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# Handbook of Cleaning for Semiconductor Manufacturing

## Fundamentals and Applications

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# Introduction

Semiconductor manufacturing continuously faces the most demanding technical challenges of any industry. As features have scaled, one of the most problematic areas of fabrication has been cleaning. Over the last few decades, the art of cleaning has turned into the science of surface preparation, critical cleaning, post-etch residue removal, and particle removal. Years ago the integrated circuit industry "borrowed" techniques from other industries – now the microelectronic engineers and scientists are the technology drivers. They work with the most advanced technology in the world making affordable microprocessors, controllers, and memory devices, so everyone can afford the newest electronic gadgets. These engineers work on devices that have minute features, rare materials, intricate equipment, and specialized processes. They help develop high-yielding, easily manufactured processes for the most sophisticated devices at the minimal cost and with the lowest environmental impact. This handbook celebrates these individuals – those who develop processes that are not physically present on a finished device. The chemicals used are all washed away, along with the contaminating metals, organics, and particles, yielding a pristine surface.

We have assembled authors with specific expertise to provide a thorough and thoughtful look at key range of cleaning topics in this field. The work is divided into three sections. The first six chapters address fundamental processes in chemical cleaning. Chapter 1 examines surface and colloid chemistry in cleaning, and Chapters 2 and 3 describe the chemistries of cleaning and etching processes. Chapter 4 details the surface phenomenon of cleaning. While chapters 5 and 6 discuss the design, delivery, and recycling of chemical formulations used in cleans. The second section (Chapters 7–14) covers a range of cleaning applications. Chapters 7, 8, 9, and 10 discuss cleaning and stripping of front end and back end of the line structures, Chapters 11 and 12 examine passivation and corrosion of copper and passivation of silicon and germanium. Wafer reclamation and wafer bonding preparation processes are discussed in Chapters 13 and 14. The last section of the book offers insight into the trends in cleans technologies. Chapter 15 details novel methods for evaluating the surface cleanliness and condition. The strip and cleans methods needed for the newest photolithography applications are discussed in Chapter 16.

Our book is dedicated to all the engineers past, present, and future that have and still toil feverishly and relentlessly to develop and utilize proven cleaning processes, and invent new ways to solve these crucial issues.

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November 2010.

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# Contents

**Foreword** xvii

**Introduction** xxi

## Part 1: Fundamentals

**1. Surface and Colloidal Chemical Aspects of Wet Cleaning** 3
*Srini Raghavan, Manish Keswani, and Nandini Venkataraman*
1.1 Introduction to Surface Chemical Aspects of Cleaning 3
1.2 Chemistry of Solid-Water Interface 4
1.2.1 Surface Charging of Oxide Films in Aqueous Solutions 4
1.2.2 Surface Charging of Silicon Nitride Films in Aqueous Solutions 6
1.2.3 Electrified Interfaces: The Double Layer and Zeta Potential 6
1.2.3.1 Oxide Films and Particles 7
1.2.3.2 Nitride Films and Particles 10
1.3 Particulate Contamination: Theory and Measurements 11
1.3.1 Effect of the Electric Double Layer Formation on Particulate Contamination 11
1.3.2 Direct Measurement of Interaction Forces between Particles and Surfaces 13
1.4 Influence of Surface Electrical Charges on Metal Ion Adsorption 17
1.5 Wettability of Surfaces 22
1.5.1 Surface Tension and Surface Energy 22
1.5.2 Adsorption Characteristics and Wettability Modification 22
1.6 High Aspect Ratio Cleaning: Narrow Structures 26
1.6.1 Rate of Liquid Penetration into Narrow Structures 27
1.6.2 Enhancement of Liquid Penetration into Narrow Structures 30
1.7 Surface Tension Gradient: Application to Drying 30
1.7.1 Isopropyl Alcohol Surface Tension Gradient Drying 31
1.7.2 Water Layer After Drying 31
1.7.3 Alternate Chemicals for Drying 32
1.8 Summary 35
References 35

**2. The Chemistry of Wet Cleaning** 39
*D. Martin Knotter*
2.1 Introduction to Aqueous Cleaning 39
2.1.1 Background of Aqueous Cleaning Chemistry 39

2.2 Overview of Aqueous Cleaning Processes 41
2.2.1 RCA Cleaning 41
2.2.2 Modified RCA Processes 41
2.2.3 Other Cleaning Processes 41
2.3 The SC-1 Clean or APM 42
2.3.1 Electrochemistry of SC-1 43
2.3.2 Molecular Mechanism 46
2.3.3 Etching Rate in APM 48
2.3.4 Concentration Variations 49
2.3.5 Concentration Monitoring and Control 53
2.3.6 APM-related Surface Roughening 55
2.3.6.1 Vapor Etching 55
2.3.6.2 Galvanic Etching and Masking 57
2.3.6.3 Catalyzed $H_2O_2$ Depletion 61
2.3.7 Metal-ion Contamination and Complexing Agents 63
2.3.8 Diluted APM 66
2.4 The SC-2 clean or HPM 67
2.4.1 Particle Deposition 68
2.4.2 Hydrogen Peroxide Decomposition in SC-2 68
2.4.3 Hydrochloric Acid Fumes 70
2.4.4 Diluted HCl 70
2.5 Sulfuric Acid-Hydrogen Peroxide Mixture 71
2.5.1 Stripping and Cleaning Mechanism 73
2.5.1.1 Dissolution Reaction 73
2.5.1.2 Discoloration Reaction 74
2.5.2 Particulate and Sulfate Contamination 76
2.5.3 Alternatives 79
2.5.3.1 Modification of SPM 79
2.5.3.2 Sulfur Trioxide 79
2.6 Hydrofluoric Acid 80
2.6.1 Hydrogen Passivation 80
2.6.2 Etching Rate Control 85
2.6.3 Bath Monitoring 86
2.6.3.1 Conductivity 86
2.6.3.2 Near Infrared 88
2.6.4 Contamination 89
Acknowledgments 91
References 91

**3. The Chemistry of Wet Etching 95**
*D. Martin Knotter*
3.1 Introduction and Overview 95
3.1.1 Definition of Etching 96
3.1.2 The Physics of Wet Etching 96
3.1.2.1 Difference in Bond Strength 98
3.1.2.2 Absence of the Proper Reactant 99
3.1.2.3 Formation of Inhibiting Coatings 99

3.2 Silicon Dioxide Etching 99
3.2.1 Hydrofluoric Acid Etching 100
3.2.2 Water-based Etching 109
3.3 Silicon Etching 111
3.3.1 Hydrofluoric Acid and Nitric Acid Mixture 113
3.3.2 Potassium Hydroxide and Alcohol Mixtures 116
3.3.3 Tetramethyl Ammonium Hydroxide Etching 120
3.4 Silicon Nitride Etching 122
3.4.1 Hydrofluoric Acid-based Etching Solutions 123
3.4.2 Hot Phosphoric Acid Etching 127
3.4.3 Water Etching 138
Acknowledgements 139
References 139

**4. Surface Phenomena: Rinsing and Drying 143**
***Karen A. Reinhardt, Richard F. Reidy, and John A. Marsella***
4.1 The Surface Phenomena of Rinsing and Drying 143
4.1.1 Introduction to Surface Phenomena in Rinsing 144
4.1.2 Introduction to Surface Phenomena in Drying 144
4.2 Overview of Rinsing 144
4.2.1 Wafer Charging 145
4.2.1.1 Charging from Immersion in Water 145
4.2.1.2 Wafer Charging During Spinning 146
4.2.2 Wetting a Surface 148
4.2.2.1 Surface Energy and Surface Tension 148
4.2.2.2 Wetting and Rinsing Small Features 150
4.2.2.3 Wetting Rough Surfaces 151
4.2.3 Silica in Water 154
4.2.3.1 Oxidation of Silicon in Water 155
4.2.3.2 Precipitation of Silica in Water 157
4.3 Overview of Drying 158
4.3.1 The Chemistry and Physics of Watermarks 158
4.3.1.1 Watermarks Formation 158
4.3.1.2 Watermarks on Wafers Caused by Cleaning 161
4.3.1.3 Watermarks on Wafers Caused by Immersion Lithography 162
4.3.2 Drying High Aspect Ratio Features and Stiction 162
4.3.3 Adhesion of Particles during Rinsing and Drying 164
Acknowledgements 166
References 166

**5. Fundamental Design of Chemical Formulations 169**
***Robert J. Rovito, Michael B. Korzenski, Ping Jiang, and Karen A. Reinhardt***
5.1 Introduction and Overview 169

5.2 Historical Development of Formulations for the Integrated Circuit Industry 170
5.2.1 Chemical Formulation Generations 170
5.2.2 First Generation Oxidizing Chemicals 171
5.2.3 Second Generation Solvent-based Formulations 172
5.2.4 Third Generation Amine-based Formulations 173
5.2.5 Hydroxylamine Photoresist Residue Removers 173
5.2.6 Fluoride-containing Strippers and Post-etch Residue Removers 174
5.2.7 Amine Post-etch Residue Removers for Copper 174
5.3 Mechanism of Stripping, Cleaning, and Particle Removal 175
5.4 Components and Additives in Chemical Formulations 177
5.4.1 Base Chemical and Active Ingredient 177
5.4.2 Buffering Agents 177
5.4.3 Surfactants 178
5.4.4 Chelating Agents 180
5.4.5 Oxygen Scavenging or Passivating Agent 180
5.5 Creating Chemical Formulations 180
5.5.1 Overview of Techniques Used in Creating Chemical Formulations 181
5.5.2 Formulation Design Models and Parameters 181
5.5.2.1 Solubility Parameters 182
5.5.2.2 Selective Solvency 184
5.5.2.3 Kinetic Salt Effects 185
5.5.3 Practical Considerations 185
5.5.3.1 Bath Life and Bath Life Extension 185
5.5.3.2 Materials Compatibility 187
5.5.3.3 Tool Configuration – Single Wafer vs. Batch Processing 188
5.5.3.4 Rinsability 188
5.5.3.5 Shipping and Shelf Life 188
5.5.3.6 Purity Level 188
5.6 Environmental, Safety, and Health Aspects 188
Acknowledgments 190
References 190

**6. Filtering, Recirculating, Reuse, and Recycling of Chemicals 193**
***Barry Gotlinsky, Kevin T. Pate, and Donald C. Grant***
6.1 Overview of Wet Chemical Contamination Control 193
6.1.1 Contamination Control Challenges Relating to Chemical Distribution 194
6.1.2 Use of Filtration to Control Particle Contamination 194
6.1.3 Metrology Techniques for Particles 194
6.1.4 Metrology Techniques for Dissolved Contaminants 195
6.2 Bulk Chemical Distribution for Wet Cleaning Tools 195
6.2.1 Bulk Chemical Delivery Systems 195
6.2.2 Bulk Chemical Delivery System Design 196

6.2.3 Particulate Purity Control for Bulk Chemical Delivery Systems 197
6.2.4 Metallic Ion Purity Control for Bulk Chemical Delivery Systems 200
6.2.5 Organic Purity Control for Bulk Chemical Delivery Systems 201
6.2.6 Chemical Delivery Sub-systems 202
6.3 Chemical Distribution, Filtering, and Recirculation Requirements for Wet Cleaning Tools 202
6.3.1 Recirculating Immersion Tools 202
6.3.2 Single Wafer Tools 204
6.3.3 Wafer Drying 206
6.4 Contamination Control Metrology 206
6.4.1 Particle Measurement for Chemical Fluids 206
6.4.1.1 Particle Measurement Methods 206
6.4.1.2 Particle Sampling Locations 210
6.4.2 Chemical Purity of Chemical Fluids 210
6.4.2.1 Inorganic Contaminant Measurement Methods 211
6.4.2.2 Inorganic Contaminant Sampling 212
6.4.3 Chemical Handling System Component Purity 212
6.5 Effects of Contamination 213
6.5.1 Particulate Contamination 213
6.5.2 Ionic and Metallic Contamination 215
6.5.3 Organic Contamination 215
6.6 Filtration 217
6.6.1 Filtration Mechanisms 217
6.6.2 Filtration Design and Materials 220
6.6.3 Characterization of Filter Performance 225
6.6.4 Filtration for Bulk Chemical Delivery Systems and Wet Clean Tools 229
6.7 Chemical Blending, Recycling, and Reuse 230
6.7.1 Chemical Blending 230
6.7.1.1 On-site blending case – 50:1 diluted HF from 49 wt% HF: 231
6.7.2 Reprocessing and On-site Waste Treatment 232
6.7.3 On-site Treatment of Waste Streams 233
6.7.4 Deionized Water Reuse and Reclamation 234
6.8 Summary 234
References 235

## Part 2: Applications

**7. Cleaning Challenges of High-κ/Metal Gate Structures 239**
*Muhammad M. Hussain, Denis Shamiryan, Vasile Paraschiv, Kenichi Sano, and Karen A. Reinhardt*
7.1 Introduction and Overview of High-κ/Metal Gate Surface Preparation 239
7.1.1 High-κ Dielectric Evolution 240

7.1.2 Metal Gate Evolution 241
7.1.3 High-κ/Metal Gate Integration and Structures 243
7.1.3.1 Gate-First Process 243
7.1.3.2 Gate-Last Process 245
7.1.3.3 Comparison between Gate-First and Gate-Last Scheme 248
7.1.3.4 Fully Silicided Process 251
7.2 Surface Preparation and Cleaning 253
7.2.1 Surface Cleaning Challenges Prior to High-κ Deposition 253
7.2.2 Pre-interfacial Oxide Formation Cleaning 253
7.2.3 Interfacial Oxide Formation 254
7.2.3.1 Hydroxyl-terminated Surface 254
7.2.3.2 Interfacial Oxide Formation 255
7.2.3.3 Thermal Oxidation 258
7.2.3.4 Nitrided Surfaces 259
7.2.3.5 Hydrogen-terminated Surface 259
7.2.4 High-κ Deposition on Germanium 260
7.3 Wet Film Removal 261
7.3.1 First Metal Gate Removal 262
7.3.2 Replacement Gate Removal 264
7.4 High-κ Removal 264
7.4.1 Challenges of Removing High-κ Material after Etching 264
7.4.2 Removal of High-κ Dielectric 265
7.4.3 Dry Removal 266
7.4.4 Wet Removal 269
7.4.5 Corrosion 272
7.4.6 Combination of Wet and Dry Removal 272
7.5 Resist Stripping and Residue Removal 273
7.5.1 Plasma Stripping 274
7.5.2 Wet Stripping 276
7.5.3 Cleanliness Prior to Anneal 278
Acknowledgments 278
References 278

**8. High Dose Implant Stripping 285**
*Karen A. Reinhardt and Michael B. Korzenski*
8.1 Introduction and Overview of High Dose Implant Stripping 285
8.1.1 High Dose Implant 286
8.1.2 Photoresist Modifications Due to Implant 288
8.1.3 Post-photoresist Removal Residue 292
8.1.4 Silicon Loss and Silicon Dioxide Formation and Loss 295
8.1.5 Dopant Deactivation 298
8.2 High Dose Implant Cleaning and Stripping Processes 299
8.2.1 Process Requirements 299
8.2.2 Process Comparison: Wet and Dry 300
8.3 Plasma Processing 301
8.3.1 Photoresist Popping 301

8.3.2 Plasma-induced Damage 304
8.3.2.1 Charging Damage 304
8.3.2.2 Physical Damage 305
8.3.3 Stripping Process Chemistry 305
8.4 Wet Processing 307
8.4.1 Wet Processing after Plasma Processing 308
8.4.2 Wet-only Processing Background 308
8.4.3 Aqueous Wet-only Processing 309
8.4.4 Semi-aqueous and Solvent Processes 312
8.4.4.1 Selective Passivation 313
8.4.4.2 Corrosion-free Compositions 315
8.4.4.3 Crust Dissolution 316
8.4.4.4 Corrosion Inhibitors 316
8.5 Other Processing 317
8.5.1 Water-assisted and Solvent-based Crust Removal 317
8.5.2 Supercritical Processing 317
8.5.3 High-pressure Processing 320
8.5.4 Cryoaerosol Process 320
Acknowledgments 322
References 322

**9. Aluminum Interconnect Cleaning and Drying 327**
*David J. Maloney*
9.1 Introduction to Aluminum Interconnect Cleaning 327
9.2 Source of Post-Etch Residues Requiring Wet Cleaning 329
9.2.1 Post-tungsten Plug Etchback Cleaning 330
9.2.2 Post-aluminum Line Etch Cleaning 331
9.2.3 Post-via Etch Cleaning 336
9.3 Chemistry Considerations for Cleans Following Etching 338
9.3.1 Fluoride-based Cleaning Formulations 340
9.3.1.1 Applications 342
9.3.1.2 Process Conditions 343
9.3.2 Cleaning with Hydroxylamine 344
9.3.2.1 Applications 346
9.3.2.2 Process Conditions 346
9.4 Rinsing/Drying and Equipment Considerations 347
9.4.1 Rinsing/Drying 347
9.4.2 Equipment 349
9.5 Alternative and Emerging Cleaning Technologies 350
Acknowledgements 351
References 351

**10. Low-κ/Cu Cleaning and Drying 355**
*Karen A. Reinhardt, Richard F. Reidy, and Jerome Daviot*
10.1 Introduction and Overview 355
10.1.1 Copper Interconnects: Background and Applications 356

10.1.2 Low-κ Dielectrics: Background and Applications 356
10.1.3 Copper and Low-κ Integration 357
10.2 Stripping and Post-etch Residue Removal 359
10.2.1 Plasma Post-etch Stripping, Cleaning, Residue Removal, and Passivation 362
10.2.2 Wet Post-etch Cleaning and Residue Removal and Drying 365
10.2.2.1 Dilute Hydrofluoric Acid 365
10.2.2.2 Semi-aqueous and Solvent Cleaning 366
10.2.2.3 Fluoride-containing Aqueous Formulations 367
10.2.2.4 Acidic Aqueous Formulations 367
10.2.2.5 Semi-aqueous Alkaline Formulations 367
10.2.2.6 Near-neutral Aqueous Formulations 368
10.3 Pore Sealing and Plasma Damage Repair 368
10.3.1 Pore Sealing 368
10.3.1.1 Plasma Treatments 369
10.3.1.2 Thin Sealing Layers 370
10.3.1.3 Graded Pores 370
10.3.1.4 Chemical Modification 370
10.3.1.5 Determination of Pore Sealing Effectiveness 371
10.3.2 Plasma Damage Repair 372
10.4 Post-chemical Mechanical Polishing Cleaning 373
10.4.1 Post-CMP Cleaning Defectivity Challenges 373
10.4.1.1 Corrosion 373
10.4.1.2 Particulate Contamination Defectivity 376
10.4.1.3 Metallic Contaminants 377
10.4.1.4 Watermarks and Stains 378
10.4.1.5 Detrimental Effects on Low-k Dielectric: Cracks and Delamination 379
10.4.1.6 Surface Conditioning and Material Integrity 380
10.4.2 Post-CMP Cleaning: Processes and Formulations 380
10.4.1.7 Particle Removal 381
10.4.1.8 Megasonic 385
10.4.1.9 Brush Scrubbing 386
10.4.1.10 Corrosion Prevention 387
10.4.3 Cost Effectiveness and Environmentally Friendly Processing 389
References 389

**11. Corrosion and Passivation of Copper 395**
*Darryl W. Peters*
11.1 Introduction and Overview 395
11.2 Copper Corrosion 396
11.2.1 Pourbaix and Stability Diagrams 396
11.2.2 Copper Corrosion and Oxidation 399
11.2.2.1 Oxidation and Corrosion with Respect to pH 399

11.2.2.2 Galvanic and Photo-induced Corrosion 400
11.2.2.3 Examples of Corrosion – Post-etch and Post-CMP 402
11.2.3 Corrosion Inhibitor Efficiency 402
11.3 Copper Corrosion Inhibitors 403
11.3.1 Azole Corrosion Inhibitors 404
11.3.1.1 Benzotriazole 404
11.3.1.2 Carboxybenzotriazol 406
11.3.1.3 5-aminotetrazole 406
11.3.1.4 1,2,4-triazole 406
11.3.1.5 Influence of Solution pH 407
11.3.1.6 Process Results of Azole Cleaning Solutions 412
11.3.2 Oxygen Scavengers 414
11.3.3 Diols, Triols, and Carboxylic Acids 415
11.3.3.1 Corrosion Inhibition Efficiency 415
11.3.4 Mercaptans 420
11.4 Copper Cleaning Formulations 420
11.4.1 Post-etch Cleaners 421
11.4.2 Post-CMP Cleaners 423
Acknowledgments 425
References 425

**12. Germanium Surface Conditioning and Passivation 429**
***Sonja Sioncke, Yves J. Chabal, and Martin M. Frank***
12.1 Introduction 429
12.1.1 Germanium Use in Integrated Circuit Transistors 429
12.1.2 Gate Stack Interface Preparation and Passivation 430
12.1.3 Need for Passivation 430
12.2 Germanium Cleaning 431
12.2.1 Wet Chemical Compatibility and Etching Rates: A Historical Perspective 431
12.2.2 Wet Chemical Compatibility and Etching Rates: Recent Results 433
12.2.3 Metal Deposition on Germanium 434
12.2.4 Metal Removal from Germanium 437
12.2.5 Particle Deposition on Germanium 439
12.2.6 Particle Removal from Germanium 441
12.3 Surface Passivation and Gate Stack Interface Preparation 442
12.3.1 Thermodynamic Stability of Native Oxides 442
12.3.2 Oxidation 443
12.3.2.1 Gate Stacks on Oxidized Germanium 447
12.3.3 Nitridation and Oxynitridation 448
12.3.3.1 Gate Stacks on Nitrided or Oxynitrided Germanium 452
12.3.4 Hydrogenation 453
12.3.4.1 Hydrogenation in Ultra High Vacuum 453

12.3.4.2 Wet Chemical Treatment of Flat Single Crystal Germanium Surfaces 454
12.3.4.3 Electrochemistry on Flat Single Crystal Germanium Surfaces 460
12.3.4.4 Hydrofluoric Acid-treated Germanium Gate Stacks 460
12.3.5 Chlorine Passivation 462
12.3.5.1 Gate Stacks on HCl-treated Germanium 463
12.3.6 Sulfur Passivation 464
12.3.7 Silicon Passivation 467
References 468

**13. Wafer Reclaim 473**
*Michael B. Korzenski and Ping Jiang*
13.1 Introduction to Wafer Reclaim 473
13.2 Introduction to Silicon Manufacturing for Semiconductor Applications 474
13.3 Energy Requirements for Silicon Wafer Manufacturing 478
13.4 Test Wafer Usage and Wafer Reclaim 479
13.4.1 Silicon Material Flow in a Wafer Fab 479
13.4.2 Economics of Reclaiming Wafers 480
13.5 Requirements for Wafer Reclaim and Recycle 482
13.5.1 Reclaim Wafer Metrics 482
13.5.2 Techniques for Measuring Wafer Reclaim Specs 483
13.6 Wafer Reclaim Options 484
13.6.1 External Reclaim 485
13.6.2 Internal Wafer Reclaim Programs 487
13.7 Types of Wafer Reclaim Processes 488
13.7.1 Conventional Reclaim Processes 488
13.7.2 Non-metal Reclaim Processes 488
13.7.3 Metal Reclaim Processes 492
13.7.4 Metal Contamination 494
13.8 Formulated Reclaim Solutions 498
Acknowledgements 498
References 499

**14. Direct Wafer Bonding Surface Conditioning 501**
*Hubert Moriceau, Yannick C. Le Tiec, Frank Fournel, Ludovic F. L. Ecarnot, Sébastien L. E. Kerdilès, Daniel Delprat, and Christophe Maleville*
14.1 Introduction and Overview of Bonding 501
14.1.1 Wafer Bonding for Semiconductor Applications 503
14.1.1.1 Silicon and Silica Direct Bonding 503
14.1.1.2 Silicon-on-insulator Structures 504
14.1.1.3 3D Integration Wafer Level Packaging 504
14.1.1.4 Diverse Material Stacking 505

14.1.1.5 Patterned Silicon-on-insulator Wafers 506
14.1.1.6 Germanium-on-insulator Wafers 506
14.1.2 Wafer Bonding Surface Conditioning 507
14.2 Planarization and Smoothing Prior to Bonding 507
14.2.1 Chemical Mechanical Planarization 507
14.2.2 Surface Smoothing 509
14.3 Wet Cleaning and Surface Conditioning Processing 511
14.3.1 Process Flow 512
14.3.2 Sulfuric Acid-Hydrogen Peroxide Mixture 513
14.3.3 Deionized Water/Ozone Cleaning 513
14.3.4 Standard Clean-1 Surface Conditioning 514
14.3.5 Standard Clean-2 Cleaning 515
14.3.6 Wafer Brush Scrubbing 515
14.3.7 Wafer Drying 516
14.3.7.1 Equipment 516
14.3.7.2 Analysis 517
14.4 Dry Surface Conditioning Processing 519
14.4.1 Process Flow 519
14.4.2 Plasma Activation 520
14.4.2.1 Background of Plasma Processing 520
14.2.2.2 Plasma Activation Mechanism 521
14.2.2.3 Plasma Subsurface Impact 524
14.4.3 Ultraviolet-Ozone Cleaning 526
14.4.3.1 Carbon Contamination 526
14.4.3.2 Ultraviolet-Ozone Cleaning 527
14.4.3.3 Oxidation by Ultraviolet-Ozone Processing 528
14.4.3.4 Surface Hydrophilicity 528
14.4.3.5 Ultraviolet-Ozone Defect Densities 529
14.5 Thermal Treatments and Annealing 529
14.5.1 Pre-bonding Annealing 530
14.5.2 Post-bond Annealing 532
14.5.2.1 Degassing Species Limitation 532
14.5.2.2 Effect of Interfacial Oxide Thickness on Bonding Defect Densities 533
14.6 Conductive Bonding 534
References 537

## Part 3: New Directions

**15. Novel Analytical Methods for Cleaning Evaluation** **545**
*Chris M. Sparks and Alain C. Diebold*
15.1 Introduction 545
15.2 Novel Analytical Methods 546
15.3 Recent Advances in Total Reflection X-ray Fluorescence Spectroscopy Analysis 547
15.3.1 Alternative X-ray Sources for TXRF 547

15.3.2 Surface Coverage of the Wafer 549
15.3.3 Edge Contamination Monitoring of the Wafer 551
15.3.4 Front and Back Surface Monitoring of the Wafer 552
15.3.5 Contamination Analysis on New Materials 553
15.4 Advances in Vapor Phase Analysis 553
15.5 Trace Metal Contamination on the Edge and Bevel of a Wafer 555
15.6 Kelvin Probe Technologies 556
15.7 Novel Applications of Electron Spectroscopy Techniques 558
15.8 Novel X-ray Spectroscopy Techniques 561
15.9 Electrochemical Sensors 561
15.10 Summary 561
Acknowledgments 561
References 561

**16. Stripping and Cleaning for Advanced Photolithography Applications 565**
***John A. Marsella, Dana L. Durham, and Leslie D. Molnar***
16.1 Introduction to Advance Stripping Applications 565
16.2 Historical Background 566
16.2.1 Solvent-Based Strippers 566
16.2.2 Hydroxylamine Photoresist Residue Removers 568
16.2.3 Fluoride-containing Strippers 568
16.3 Recent Trends for Photoresist Stripping and Post-etch Residue Removal 569
16.3.1 New Materials and Compatibility Issues 569
16.3.2 Germanium 569
16.3.3 Phase-change Memory Material 569
16.3.4 Porous Low-κ Materials 570
16.3.5 High-κ Materials 570
16.3.6 High Dose Ion Implanted Photoresist 571
16.4 Single Wafer Tools 572
16.4.1 Back End of the Line Processing 573
16.4.2 Front End of the Line Processing 574
16.4.3 Photoresist Rework 575
16.5 Wetting in Small Dimensions and Cleaning Challenges 576
16.6 Environmental Health and Safety 579
16.6.1 Challenges to the Semiconductor Industry 579
16.6.2 Solvents 580
16.7 The Future of Advanced Photoresist Stripping and Cleaning 581
Acknowledgements 581
References 581

**Index 585**

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# PART 1
# FUNDAMENTALS

# 1

# Surface and Colloidal Chemical Aspects of Wet Cleaning

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*Abstract*

Surface and colloidal chemicals aspects relevant to wet chemical cleaning and drying of semiconductor surfaces are reviewed. Specific areas discussed in this chapter include surface charging of metal oxide and nitride films, development of an electrical double layer, zeta potential of electrified interfaces and its effect on particulate contamination, adsorption of surfactants and metal ions on insulating surfaces, principles of surface tension gradient drying, and wetting and penetration of high aspect ratio features.

*Key words:* interfacial phenomena, wet cleaning, surface charging of metal oxide and nitride, electrical double layer, metal adsorption, high aspect ratio cleaning, surface tension gradient drying

## 1.1 Introduction to Surface Chemical Aspects of Cleaning

The fabrication of integrated circuits requires a myriad of liquid-based etching and cleaning processes that are followed by rinsing and drying steps. Interfacial phenomena such as wetting, spreading, adsorption, adhesion, and surface charge play a critical role in determining the feasibility and efficiency of a liquid-based process step. The objective of this chapter is to discuss the fundamental science of the key interfacial phenomena relevant to wafer etching, cleaning, and drying. Specific areas discussed in this chapter include:

1. Surface charging of materials in aqueous cleaning and rinsing solutions – understanding of the physical phenomena related to the adhesion and removal of particulate contaminants and metal ions.
2. High aspect ratio cleaning – understanding the physical limitations induced by surface wetting and capillary forces for processes that require liquid penetration into narrow features.

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3. Drying methods – understanding the physics of creating a surface tension gradient at the water/vapor interface through interfacial adsorption.

The aforementioned concepts should be considered in unison to understand and explain cleaning processes and to control contamination. For example, to remove metallic and particulate contamination, the cleaning chemical must wet the surface, desorb, and preferably complex the metal ion and create a surface which bears a charge of the same sign as that on the contaminant particles to prevent re-deposition.

## 1.2 Chemistry of Solid-Water Interface

Successful removal of colloidal particles from surfaces requires an understanding of the repulsive and attractive forces between the particle and the surface. The repulsive forces arise mainly from the interaction of charged double layer at the particle/solution and the wafer/solution interface. The degree of surface hydroxylation and acid-base characteristics of these hydroxyl groups impact the charging of a surface. Sections 1.2.1 and 1.2.2 describe the surface charging of silicon dioxide and silicon nitride in aqueous media.

### 1.2.1 Surface Charging of Oxide Films in Aqueous Solutions

The surface of a semi-metal oxide film is terminated with hydroxyl (–OH) groups. A comprehensive discussion of hydroxylation of an oxide surface is provided by Yopps *et al.* [1]. The density of these hydroxyl groups is roughly two to three per square nm [2]. When this oxide surface is immersed in an aqueous solution, the hydroxyl groups react with $H^+$ and $OH^-$ ions. These interactions are represented using the following equilibrium equations [3]:

$$\mathrm{MOH} + \mathrm{H}^+ \leftrightarrow \mathrm{MOH}_2^+ \qquad K_1 \tag{1.1}$$

$$\mathrm{MOH} \leftrightarrow \mathrm{MO}^- + \mathrm{H}^+ \qquad K_2 \tag{1.2}$$

where $M$ is a metal atom or an element such as Si.

Using the equilibrium constants ($K_1$ and $K_2$) for the reactions of the protonation (Eq. 1.1) and deprotonation (Eq. 1.2) of SiOH sites, the fraction of sites with positive, negative and zero charge, viz, $\theta_+$, $\theta_-$ and $\theta_o$ on $SiO_2$ can be calculated as a function of solution pH. The result of such a calculation is shown in Figure 1.1 for $SiO_2$ using $K_1$ and $K_2$ values of $10^{0.7}$ and $10^{-3.9}$ respectively [4]. The surface charge density (coulombs per square meter), $\sigma_{surf}$, at any particular pH is given by the expression:

$$\sigma_{surf} = N_s q(\theta_+ - \theta_-) \tag{1.3}$$

where $N_s$ represents the total number of surface sites per square meter, and $q$ is the fundamental electronic charge (coulombs).

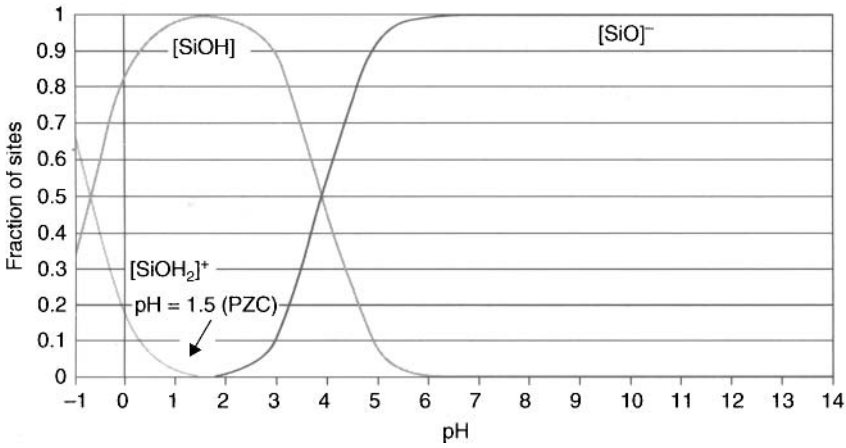



**Figure 1.1.** Fraction of positive, negative, and neutral sites on a $SiO_2$ surface immersed in water at various pH values calculated using $K_1 = 10^{0.7}$ and $K_2 = 10^{-3.9}$. Used with permission of the authors.

Figure 1.1 shows that the surface of $SiO_2$ is positively charged at low pH and negatively charged at high pH. At a pH of ~1.5, the fraction of positive sites is equal to the fraction of negative sites. This pH is called the point of zero charge (PZC) [5]. It is worth noting that at the PZC while the fractions of positively charged and negatively charged sites may be equal, each fraction may not be 0.5. The PZC value is roughly equal to the average of $pK_1$ and $pK_2$. Reference [6] outlines surface charging theory with respect to wafer cleaning.

Oxides may be classified as acidic, basic, or amphoteric [7]. Acidic oxides are generally oxides of non-metals (*e.g.* $SiO_2$, $As_2O_3$) that are dissolved by bases. By contrast, basic oxides (*e.g.* alkaline earth oxides such as MgO, FeO) are oxides of metals that are dissolved by acids. Oxides that show both acidic and basic properties are referred to as amphoteric oxides (*e.g.* $Al_2O_3$, SnO). Acidic oxides exhibit a low PZC while basic oxides exhibit higher PZC. For example, $SiO_2$, an acidic material, exhibits a PZC close to a pH of 2 while $Al_2O_3$, a basic material, exhibits a PZC close to a pH of 9. Table 1.1 lists PZC of materials of interest to semiconductor processing.

An acid- base mass titration technique is typically used to determine the PZC of materials. In this technique demonstrated by Schwarz, a suspension of oxide particles in an electrolyte is titrated with a standard acid/base solution [14]. The protonation/deprotonation of the oxide surface causes the solution pH to increase/decrease from the original pH value. A mass balance from the added $H^+/OH^-$ ions is then made to obtain the extent of adsorption of $H^+$ and $OH^-$. The surface charge density, $\sigma_{surf}$ is given by:

$$\sigma_{surf} = F \times (\Gamma_{H^+} - \Gamma_{OH^-}) \tag{1.4}$$

where $\Gamma_{H^+}$ and $\Gamma_{OH^-}$ are adsorption densities (moles per square meter) of $H^+$ and $OH^-$, respectively, and $F$ is the Faraday constant (96500 coulombs/gram equivalent).

The use of this technique is described in many papers [15–18] and only works well for samples with large surface areas such as particles. For materials with low surface areas such as oxide films, the pH change due to adsorption/desorption is too small to be accurately measured causing large errors in mass balance [19].

**Table 1.1.** Point of zero charge of materials of interest to wafer cleaning

| Material | PZC at pH of | Type | Reference |
|---|---|---|---|
| $SiO_2$ | 2–4 | Acidic | [8] [9] |
| $Si_3N_4$ | 3–5.5 | Depends on relative proportion of $NH_2$ and OH groups | [8] [9] |
| $TiO_2$ | 5–6 | Weakly acidic | [10] |
| $Al_2O_3$ | 8–9 | Amphoteric/mildly basic | [11] [12] |
| Si | 3–4 | Acidic | [8] |
| PSL | No PZC (negative charge at all pH values) | Not applicable (organic) | [13] |

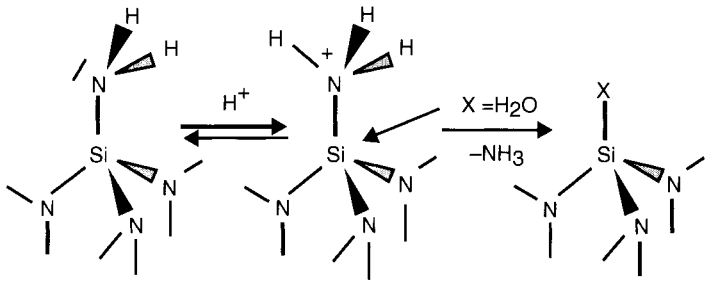



**Figure 1.2.** Charging of silicon nitride films in water; protonation of amine terminated surface sites leading to formation of positively charged sites that may react with water to form silanol groups [20]. Used with permission from Martin Knotter, NXP.

### 1.2.2 Surface Charging of Silicon Nitride Films in Aqueous Solutions

Silicon nitride films are most commonly deposited using a chemical vapor deposition (CVD) technique in which silane ($SiH_4$) reacts with ammonia ($NH_3$). Plasma-enhanced CVD (PECVD) forms $SiN_x$ and low pressure CVD (LPCVD) forms $Si_3N_4$. Consequently, silicon nitride films may contain up to 5–6 atomic % hydrogen, especially those formed with PECVD. As shown in Figure 1.2, these films typically have amine ($-NH_2$) surface groups, which depending on their $pK_a$ value can be protonated leading to the formation of positively charged sites [20]. The negative sites on the surface of nitride films have been postulated [21, 22] to be created by the reaction of surface amine groups with water forming silanol (Si-OH) followed by deprotonation to form negatively charged $SiO^-$ sites. The isoelectric point (defined in Section 1.2.3) of nitride films can vary widely depending on the hydrolytic strength of $-NH_2$ groups, which in turn will depend on the solution pH, ionic strength, and temperature.

### 1.2.3 Electrified Interfaces: The Double Layer and Zeta Potential

A solid immersed in an aqueous solution produces a region of electrical inhomogeneity at the solid-solution interface. An excess charge at the solid-solution

interface is balanced by a diffuse region of equal but opposite charge on the liquid side. Composed of surface charge and its counter ions, this region is called the electrical double layer. Helmholtz was amongst the first to present a simple capacitor model for an electrical double layer [23]. Following this, a diffuse model of a double layer where the potential decreases exponentially from the surface into the bulk of the solution was put forth by Gouy and Chapman [24, 25]. Stern combined the capacitor model with the diffuse model and suggested that the double layer consists of two parts – an internal Stern layer and outer diffuse layer [26]. A more comprehensive review of recent theoretical models that seek to overcome the limitations of the Gouy-Chapman-Stern model is given in reference [27]. The following section provides a general discussion on selected phenomenological aspects of electrical double layers for oxide films that in principle can be applied to nitride films as well.

### 1.2.3.1 *Oxide Films and Particles*

The development of charge on the surface of oxides in contact with an aqueous solution results in an electrified interface. Hydrogen and hydroxyl ions that cause the development of surface charge are referred to as potential determining ions (PDI) [5] [28]. Figure 1.3 is a schematic sketch of the interface between $SiO_2$ and

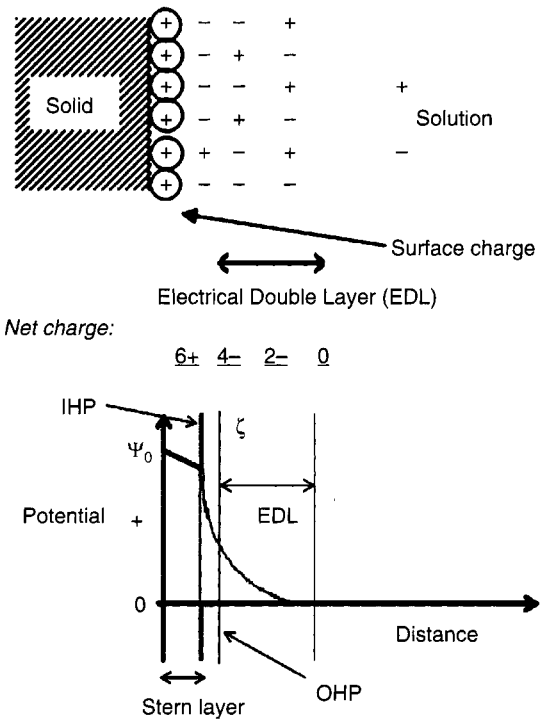



**Figure 1.3.** Schematic diagram of electrical double layer structure at the $SiO_2$/aqueous solution interface at a pH where the surface is positively charged. Used with permission from the authors.

$H_2O$ at a pH value such that the surface has a positive charge. The six positive charges on the oxide surface are balanced by an equal number of negative charges in the surrounding liquid layers (net negative charges of 4 and 2 in the subsequent 1st and 2nd liquid layers from the surface) that line up close to the interface. Due to thermal motion of water molecules and ions, the charge balancing "counter ions" may be distributed in a few layers from the surface. The layer of positive charge and the "effective" layer of negative counter ions, shown in Figure 1.3, is referred to as the electrical double layer. This separation of charge at the interface leads to a surface potential, $\psi_0$. Experimentally it is not possible to measure $\psi_0$ for dielectric materials, but it can be calculated using a Nernst equation. For a metal immersed in a solution containing ions of its own kind, the classical Nernst equation is used for calculating the surface potential. However, if the potential determining ions are $H^+$ and $OH^-$, this equation converts to the following equation [28]:

$$\frac{\Psi_0 = \frac{RT}{F} \ln a_{H^+}}{(a_{H^+})_{PZC}} \tag{1.5}$$

where $a_{H^+}$ is the activity of the hydrogen ion in the solution, $(a_{H^+})_{PZC}$ is the activity of the hydrogen ion at the pH value corresponding to point of zero charge (PZC) of the solid surface, $F$ is the Faraday constant, and $T$ is the temperature of the solution.

Rearranging Equation 1.5 and substituting the values of constants the following is obtained:

$$\psi_0(V) = 0.059(pH - PZC) \qquad \text{at } 25°C \tag{1.6}$$

According to Equation 1.6, the potential of an oxide surface should change by 59 mV at 25°C for a ten-fold change in $H^+$ ion concentration in solution. This same potential change is predicted by the classical Nernst equation (with $H^+$ replaced by the metal ion $M^+$) for a ten-fold change in univalent metal ion concentration.

The interfacial potential decreases from a value of $\psi_0$ on the surface to a value of zero in the bulk of the solution. The profile of potential decay with distance into the solution is schematically illustrated in the lower half of Figure 1.3. The profile of this decay has been discussed in many textbooks dealing with the electrical double layer phenomenon [29, 30]. The surface potential decays in a linear fashion from the surface to a location called the outer Helmholtz plane (OHP) which represents the closest distance of approach of electrostatically attracted counter ions. Beyond the OHP, the potential decays exponentially following a Boltzmann type distribution into solution. The potential of the double layer just outside the outer Helmholtz plane is known as zeta potential (ZP) indicated by $\zeta$ in Figure 1.3. Similar to the surface charge, ZP also varies with pH. The pH value at which the ZP of a material is zero is known as the isoelectric point (IEP) [28].

The zeta potential value depends on the profile of the decrease of the interfacial potential with distance from the surface. In solutions of high ionic strength, the surface charge is mostly balanced by counter ions in the OHP resulting in low values of ZP. For example, in a 1 M ionic strength solution, most of the potential drop would occur within a distance of 0.3 nm from the surface. This means that while the surface charge may be either positive or negative, ZP would be close to zero

in such solutions. In most of the cleaning solutions used in semiconductor manufacturing, such as SPM (sulfuric acid hydrogen peroxide mixture), BHF (buffered hydrofluoric acid), APM (ammonium hydroxide hydrogen peroxide mixture), and HPM (hydrochloric acid hydrogen peroxide mixture), the ionic strength is so high that the ZP of materials is likely to be close to zero. Because of this issue, cleaned wafers are typically re-immersed in dilute electrolyte solutions to measure the effect of cleaning treatments on the ZP of films. If the adsorption of ions causes the sign of zeta potential to be opposite to that of the surface charge, it is an indication that adsorption involves other forces in addition to electrostatic forces [5]. These ions, called specifically adsorbing ions, typically reside in the inner Helmholtz plane (IHP) and are much closer to the surface. For example, the adsorption of long chain cationic surfactants at an oxide/solution interface can change the ZP of a negatively charged surface from an initial negative value to a positive value [31].

The measurement of ZP is carried out using electrokinetic techniques. Two techniques are widely used for determining ZP during wafer cleaning. For colloidal particles, the technique of microelectrophoresis is used [29] [32]. In this technique, mobility of charged particles is measured in an applied electric field (*e.g.* using the Doppler effect). This mobility is then converted to ZP using Henry's equation given below [30].

$$\zeta = \frac{3\mu_E \eta}{2\varepsilon_r \varepsilon_0 f_1(\kappa a)} \tag{1.7}$$

where $\mu_E$, $\varepsilon_r$, $\varepsilon_0$, $\eta$, $\kappa$ and $a$ are electrophoretic mobility, relative permittivity of solution, permittivity of vacuum, viscosity of solution, Debye-Huckel Parameter (inverse of Debye length), and radius of particle, respectively. The term $f_1(\kappa a)$ is a monotonically varying function that increases from 1.0 at $\kappa a = 0$ to 1.5 at $\kappa a = \infty$, in which case Equation 1.7 becomes the Smoluchowski equation.

The streaming potential technique is used for the ZP characterization of wafer surfaces [22]. Streaming potential arises when an ionic solution driven by a pressure gradient comes in contact with a charged stationary surface. When the solution flows, a part of the double layer charge is sheared and carried with the flowing solution giving rise to what is termed as streaming current. Streaming current/potential is measured by placing two identical reversible electrodes at the two ends of the channel formed between two wafer surfaces [22, 33]. Zeta potential can be calculated from the gradient of measured streaming potential with respect to pressure drop across the channel using Equation 1.8 [30].

$$\zeta = \frac{\Delta E}{\Delta p} \frac{\eta K_e}{\varepsilon_r \varepsilon_0} \tag{1.8}$$

where $\Delta E$ and $\Delta p$ are the potential difference and pressure drop across the two ends of a capillary/channel, and $K_e$ is the electrolyte conductivity.

Using a streaming potential technique, there have been several reports of measurements of ZP of oxide, silicon, and nitride wafers [34, 35]. Strictly speaking, ZP exists only for surfaces that are insulating in nature. It is not meaningful to describe ZP for conductive metallic surfaces (*e.g.* gold particles, chromium coated quartz mask surface) without an insulating layer because charges are immediately

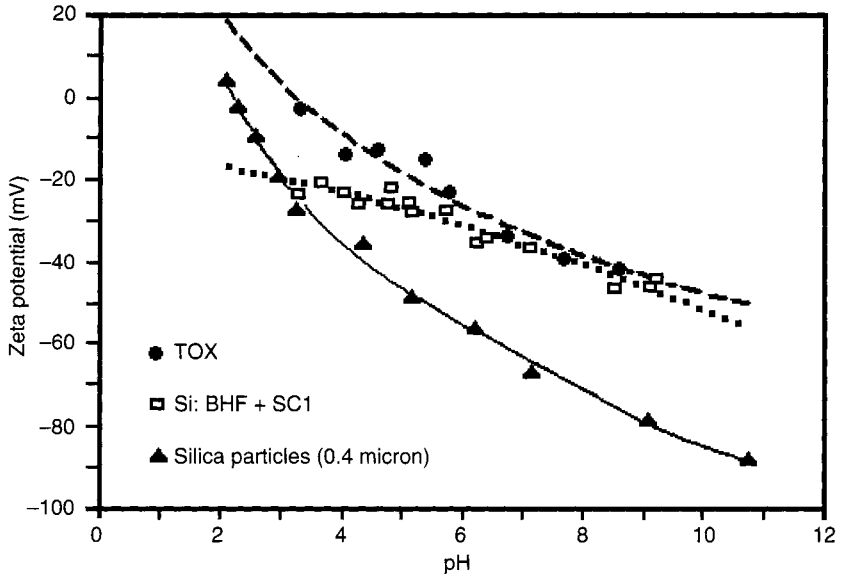



**Figure 1.4.** Comparison of zeta potential of silicon dioxide surfaces subjected to different surface treatments [33]. Used with permission of Raghunath Chilkunda.

conducted into the bulk of the metal. Data for ZP of metallic surfaces quoted in the literature could have only been obtained for metallic surfaces with an insulating surface layer [36, 37]. The zeta potentials of materials are known to be strongly dependent on surface preparation or synthesis procedure. For example, $TiO_2$ particles synthesized in a chloride-based medium may have a very different IEP than particles synthesized from a sulfate-based solution. An example of the effect of surface treatment on ZP of films is shown in Figure 1.4 [33]. In this figure, the measured ZP of thermal silicon dioxide (TOX) films and silicon subjected to BHF treatment followed by SC-1 (standard clean-1 or APM) leading to formation of a chemical oxide are shown. For comparison purposes, the ZP of colloidal silica particles (0.4 μm) is also shown. It may be discerned that the TOX films have an isoelectric point (IEP) close to a pH of 4 whereas colloidal silica particles have an IEP close to pH of 3. However, silicon coated with a chemical oxide film formed in the SC-1 solution does not exhibit an IEP in the pH range of 2 to 10 [33]. Even though all the films have a negative ZP in the pH range of 5 to 10, the value of IEP is dependent on the type of surface treatment.

### *1.2.3.2 Nitride Films and Particles*

As in the case of oxide surfaces, the IEP of nitride surfaces is also sensitive to preparation procedures. Results from a study investigating the effect of different pretreatments on the IEP of nitride films is shown in Figure 1.5 [22]. Removal of surface oxide by BHF treatment yields a film with an IEP of approximately 5.3. Oxidizing pretreatments such as SPM and APM shift the isoelectric point to lower pH values. Silicon nitride particles are commonly used as model contaminant particles in wafer cleaning studies. The IEP of silicon nitride particles is a strong function of the method of preparation and the aging process, and thus can vary from a pH of 2.5 to 6.2 [38, 39].

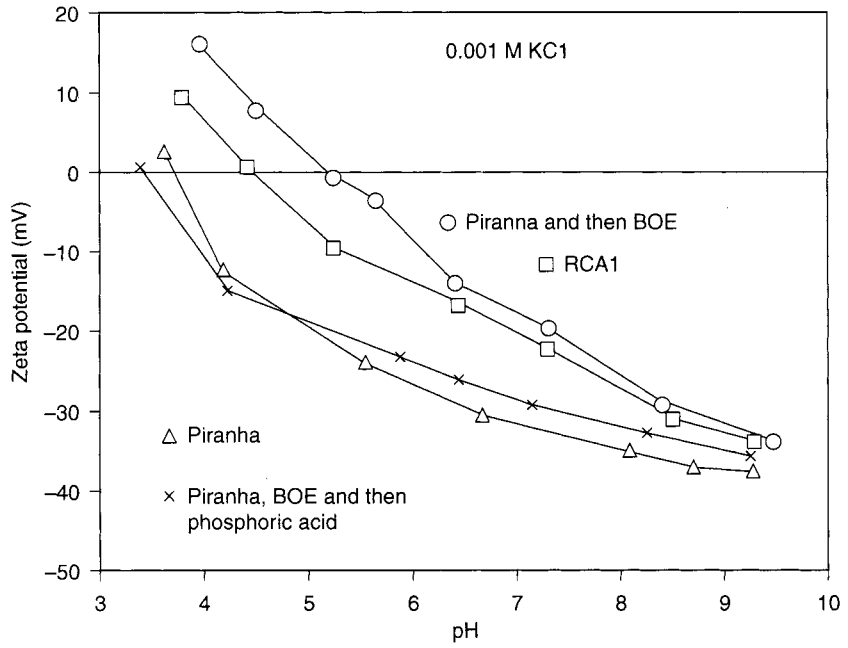



**Figure 1.5.** Effect of different surface treatments on the zeta potential of LPCVD silicon nitride films measured by streaming potential method [22]. Reproduced with permission of ECS – The Electrochemical Society from Jan, D. and Raghavan, S., *Journal of the Electrochemical Society.*

## 1.3 Particulate Contamination: Theory and Measurements

### 1.3.1 Effect of Electric Double Layer Formation on Particulate Contamination

The electric charge developed by particles affects contamination of the wafer surfaces during cleaning. If the charges on the contaminant particles and the wafer surface in a given liquid medium are opposite in sign, then electrostatic attraction between the particle and the surface is favorable. In the DLVO (Derjaguin and Landau, Verwey, and Overbeek) theory [40–42], the potential energy of interaction between two materials is considered to consist of two components, namely van der Waals and electrical double layer. The van der Waals (VDW) interaction energy, $E_{VDW}$ is almost always attractive, and for the interaction between a spherical particle and a flat plate, it is given by the following equation:

$$E_{VDW} = -\frac{A_{132} \cdot a}{6D} \tag{1.9}$$

In Equation 1.9, $A_{132}$ is the effective Hamaker constant between particle 1 and surface 2 immersed in medium 3, $a$ is the radius of particle, and $D$ is the closest distance of separation between particle and surface. The negative sign indicates that VDW interaction energy is attractive. The effective Hamaker constant between particle 1 and surface 2 immersed in a medium 3 can be calculated from the individual Hamaker constants of the three materials, $A_{11}$, $A_{22}$, and $A_{33}$, according to the following equation.

$$A_{132} = \left(\sqrt{A_{11}} - \sqrt{A_{33}}\right)\left(\sqrt{A_{22}} - \sqrt{A_{33}}\right) \tag{1.10}$$

The Hamaker constant of materials lies in the range of $10^{-19}$ to $10^{-20}$ J.

The electrostatic energy of interaction between the particle and the surface depends on the surface potential of the particle and the wafer ($\psi_{01}$ and $\psi_{02}$, respectively), the closest distance of separation between the surface of the particle and the wafer ($D$), diameter of the particle ($d$), and the Debye length ($\kappa$) in the liquid medium. The Debye length is a function of the ionic strength of the medium and is given by:

$$\kappa = \left[ \frac{1000 q^2 N_A}{\varepsilon_r \varepsilon_0 k_B T} \sum_i z_i^2 M_i \right]^{0.5} \tag{1.11}$$

where $q$ is the fundamental electronic charge, $N_A$ is Avogadro's number, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $z_i$ is the charge on the $i^{th}$ ion, $M_i$ is the molar concentration of $i^{th}$ ion, $\varepsilon_0$ is the permittivity of free space, and $\varepsilon_r$ *is the* relative permittivity of the material with respect to vacuum. For surface potential values less than 50 mV, the expression for electrostatic interaction energy, $E_{EDL}$, is given by:

$$E_{EDL} = \pi \varepsilon d \left( \Psi_{01}^2 + \Psi_{02}^2 \right) \left\{ \frac{2\Psi_{01}\Psi_{02}}{\Psi_{01}^2 + \Psi_{02}^2} \ln \frac{1 + e^{-\kappa D}}{1 - e^{-\kappa D}} + \ln \left[ 1 - e^{-2\kappa D} \right] \right\} \tag{1.12}$$

Replacement of surface potential by zeta potential in the above equation introduces minimal error if the surface potential values are small (<50 mV).

Several key comments may be made about this expression:

1. The electrostatic energy of interaction is proportional to the product of the surface potential of materials 1 and 2. Consequently, if the surface and the particle have surface potentials of the same sign, the electrostatic interaction energy will be positive or repulsive. Alternatively, if the surface or zeta potentials are of opposite signs, $E_{EDL}$ will be negative or attractive.
2. Higher ionic strength solutions result in larger values of k that will significantly reduce the magnitude of $E_{EDL}$. For a very large value of k, $E_{EDL}$ will be close to zero.
3. In low dielectric constant solutions such as organic liquids, $E_{EDL}$ will be quite small.

Figure 1.6 is a schematic illustration of van der Waals interaction energy, electrostatic interaction energy and sum of the two components as a function of distance of separation between a particle and a surface. In the figure, attractive energy is denoted by a negative sign whereas repulsive energy is denoted by a positive sign. As may be seen, the total energy of interaction exhibits a maximum at a certain distance from the surface. This maximum represents a barrier for particle deposition on the surface. The height of the barrier would decrease with an increase in ionic strength of the solution. Reduction in barrier height would favor particle deposition.

The importance of ionic strength of solutions on particle contamination was elegantly demonstrated by Riley and Carbonell using silica particles [43]. They investigated the contamination of cleaned silicon wafers in solutions of different ionic

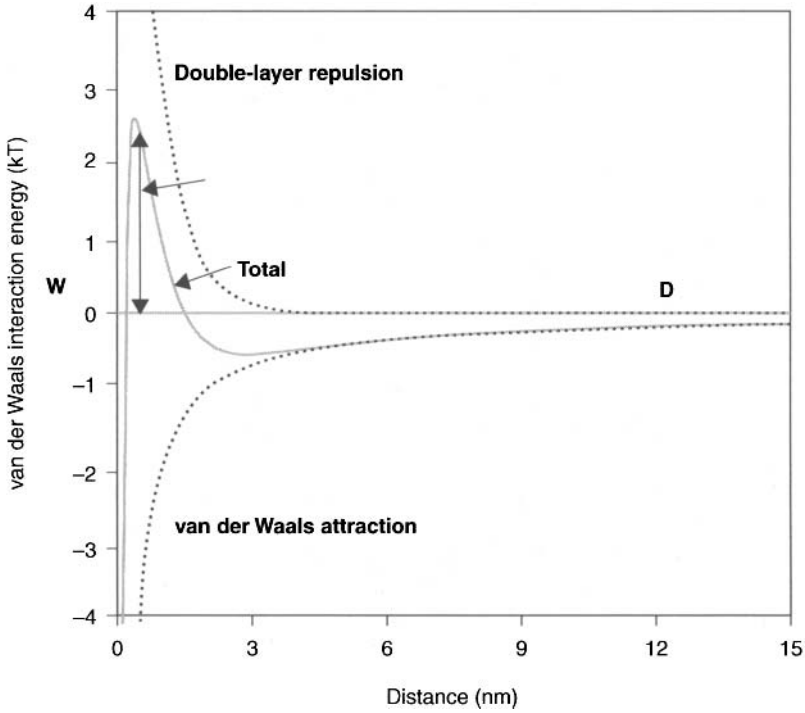



**Figure 1.6.** Schematic plots of van der Waals interaction energy, electrostatic interaction energy, and the sum of the two energies against distance of separation between a particle and a surface. Used with permission from the authors.

strength containing mono-sized silica particles at pH values where the zeta potential of wafer and particles are both negative. The results of their study are plotted as normalized surface coverage as a function of ionic strength in Figure 1.7. Normalized surface coverage is defined as the ratio of the number of particles deposited on wafers submerged into contaminated solution for 5 min to that deposited on wafers dipped for a few seconds. The results indicate that particle deposition on wafers increases sharply at an electrolyte concentration of 0.01 M. The $\kappa$ value at this electrolyte concentration is reasonably large (0.33 $nm^{-1}$); consequently, the electrostatic repulsion between particle and wafer is significantly reduced. Sulfuric acid hydrogen peroxide mixture, HPM, and BHF solutions have ionic strengths in excess of 1 M and, thus, provide conditions conducive to particulate contamination. Even though the ionic strength of 5:1:1 ($H_2O$:$H_2O_2$:$NH_4OH$) SC-1 solution is in excess of 1 M, deposited particles, if any, are continuously removed due to silicon etching [44].

### 1.3.2 Direct Measurement of Interaction Forces between Particles and Surfaces

Atomic force microscopy (AFM) has emerged as a very useful tool for directly measuring interaction forces between surfaces in air and liquid media [45]. A technique known as the colloidal probe method has been developed to measure interaction forces between particles and surfaces [45–47] and reviewed in [6]. In this technique, a single particle (1–50 μm) is attached to the end of an AFM

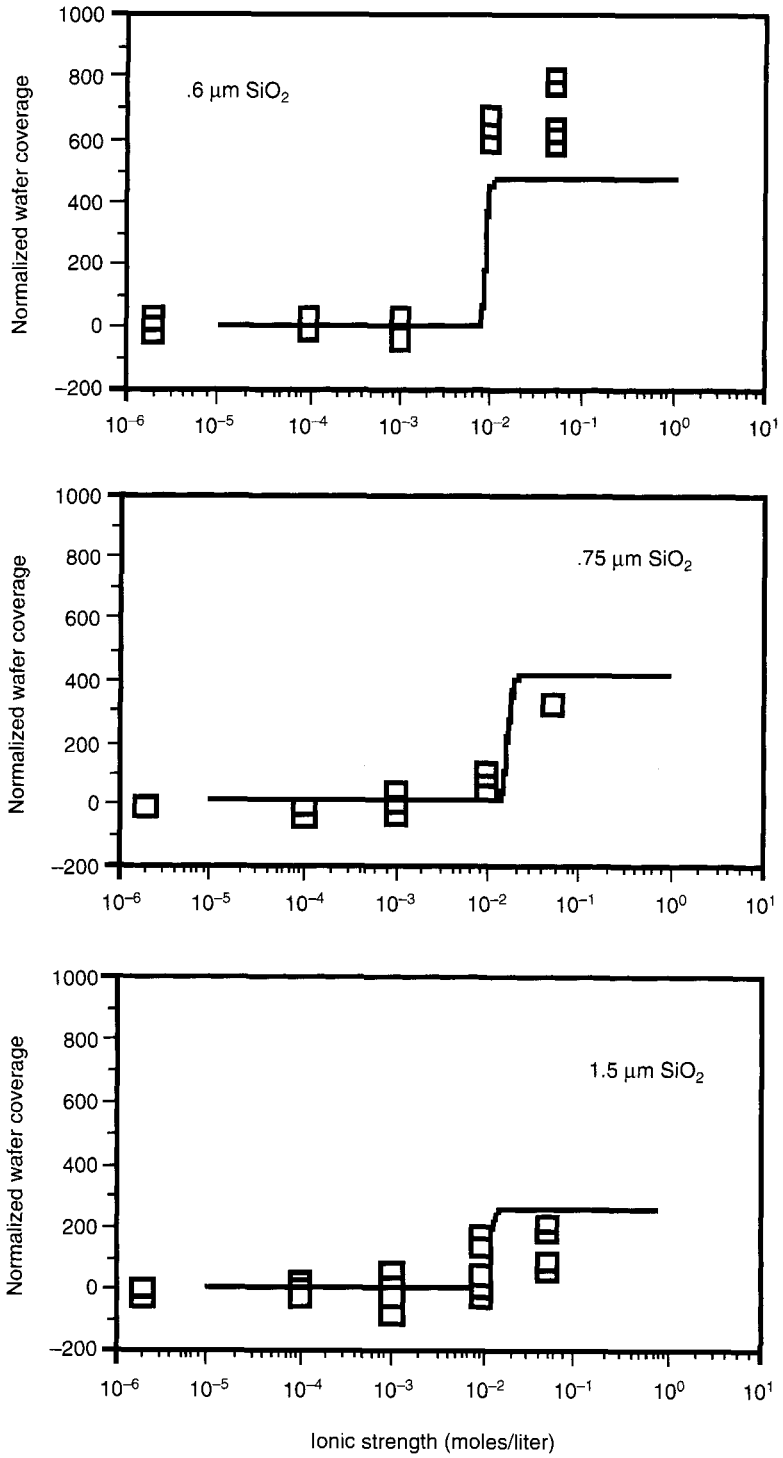



**Figure 1.7.** Normalized coverage of silicon wafers by 0.6, 0.75, and 1.5-μm sized silica particles as a function of ionic strength of solution [43]. Reprinted from *Journal of Colloid and Interface Science*, 158(2), Riley, D. J and Carbonell, R. G., "Mechanisms of Particle Deposition from Ultrapure Chemicals onto Semiconductor Wafers: Deposition from Bulk Liquid during Wafer Submersion", page 259. Copyright (1993) with permission from Elsevier.

cantilever, and the instrument measures the interaction forces during the particle approach towards and retraction from a surface. The adhesion can be quantified from the force measured during retraction.

An example of the measured force between a silicon dioxide surface and a silica particle (5 μm) in deionized water (DIW) is shown in Figure 1.8. A long-range repulsive force is observed starting at a separation distance of 40 nm. This repulsive force is due to the interaction between the electrical double layers on the negatively charged surfaces. The magnitude of the repulsive electrical double layer force continues to increase as the tip and the surface approach each other. When the tip-cantilever assembly is retracted from the surface, the force-distance curve closely follows the curve obtained during approach.

The interaction force between a hydrogen terminated silicon surface and hydrogen terminated silicon tip as a function of separation distance after time of immersion of 2, 10 and 60 min is shown in Figure 1.9. In this case, during approach (Figure 1.9a) only attractive forces exist between the surface and the tip after 2 and 10 min. The tip jump onto Si surface occurs at distances of 4.9 and 2.8 nm after 2 and 10 min, respectively, as indicated by down arrows. When the immersion time was increased to 60 min, a weak repulsive force was measured starting at a distance of ~ 15 nm. However, ultimately the force becomes attractive and the tip suddenly jumps onto the surface at a distance of ~ 2.0 nm. It has been reported in literature that the hydrogen terminated surface requires hours of immersion in aerated water to be transformed to a hydrophilic state. Therefore, it can be expected that the hydrophobic Si-H sites are not likely to be replaced by hydrophilic Si-OH sites after 2 and 10 min of immersion times. Therefore, only attractive forces were

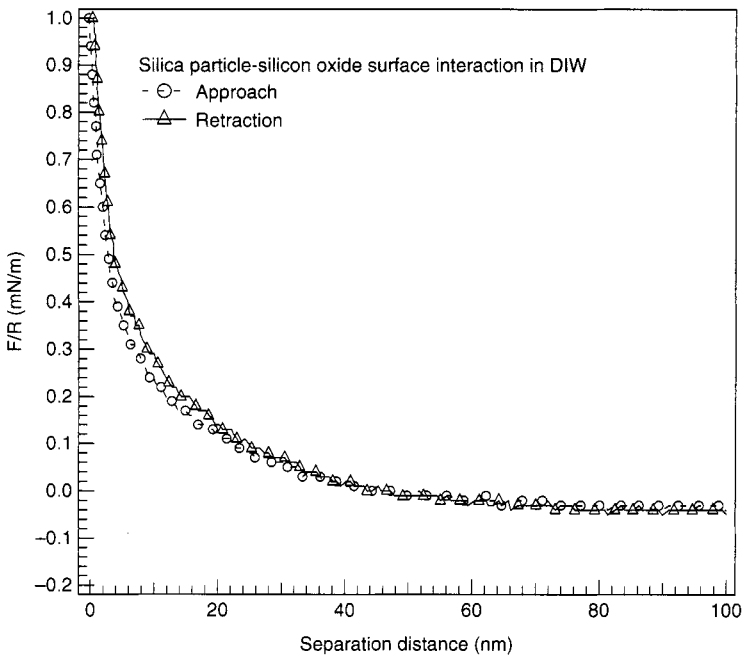



**Figure 1.8.** Normalized force as a function of separation distance between a silica particle and silicon oxide surface in DIW. Used with permission from the authors.

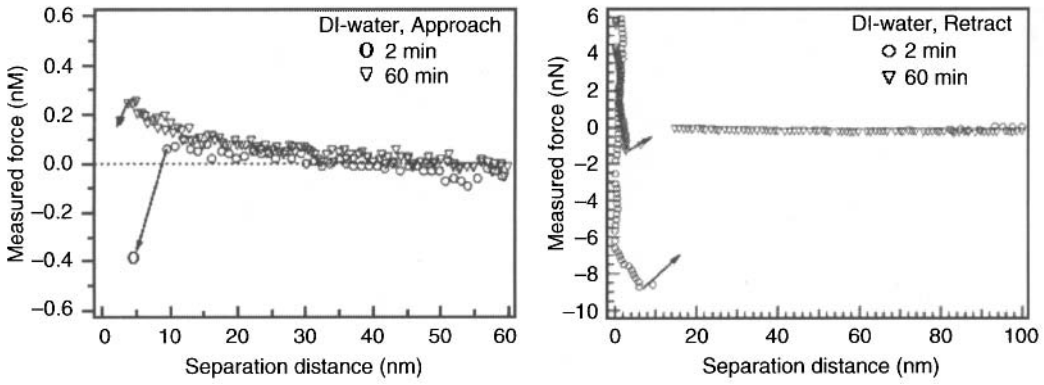



**Figure 1.9.** Force measured as a function of separation distance for interaction between a hydrophobic silicon tip and hydrophobic silicon surface in DIW: a) approach curve and b) retraction curve. Used with permission from the authors.

measured during approach between the silicon surface and the silicon tip. After 60 min of immersion time, the native oxide film that is formed would acquire a negative charge by dissociation of silanol groups (Si-OH) to $SiO^-$ and $H^+$. The measured repulsive force is a consequence of the establishment of negative charges of the surface and the tip.

The adhesion forces between silicon surface and silicon tip in DI-water can be measured from the retraction curves as shown in Figure 1.9b. It can be seen from this figure that a strong adhesion force of 10.5 nN exists after a short immersion time of 2 min. The results also show that as the immersion time increased from 2 to 10 and 60 min, the adhesion force decreased from 10.5 nN to 3.0 nN and 1.2 nN, respectively.

In an effort to understand particle deposition on silicon after processing in HF solutions, Chen and Singh [45] measured interaction forces between a HF-cleaned silicon nitride tip (representing nitride particles commonly used for contamination experiments) and a hydrogen terminated silicon surface in an acidic solution at pH = 1.88. The solution contained 0.1 wt% HF to prevent oxidation of surfaces. The results shown in Figure 1.10 reveal attraction between surfaces during approach as well as retraction indicating the dominant role of van der Waals forces. Addition of an anionic surfactant at ~1 wt% eliminated this attractive force.

Cooper *et al.* measured interaction forces between polystyrene latex (PSL) particles (5 μm) and silicon dioxide ($SiO_2$) surfaces in 0.03 M $KNO_3$ solution with pH ranging from 2 to 10 [48]. The results show a strong effect of pH on the force between the particle and the surface. A strong adhesion force of 127 nN was measured in an acidic solution with a pH of 3. This adhesion force is attributed to the van der Waals force that exists between the particle and the surface. Force measurements at a pH greater than 5 show a significant decrease in adhesion force ranging from 0 to 12 nN, as shown in Figure 1.11. Increasing the pH of the solution also resulted in a higher surface roughness due to etching of the oxide film in a basic solution. It was concluded that this increase in surface roughness causes the particle to interact mainly with the asperities and not the flat surface beneath, thereby reducing the interaction volume between particle and substrate. This results in the decrease of adhesion force between two surfaces. The measured adhesion force was compared with theoretically calculated forces using an adhesion force model that models

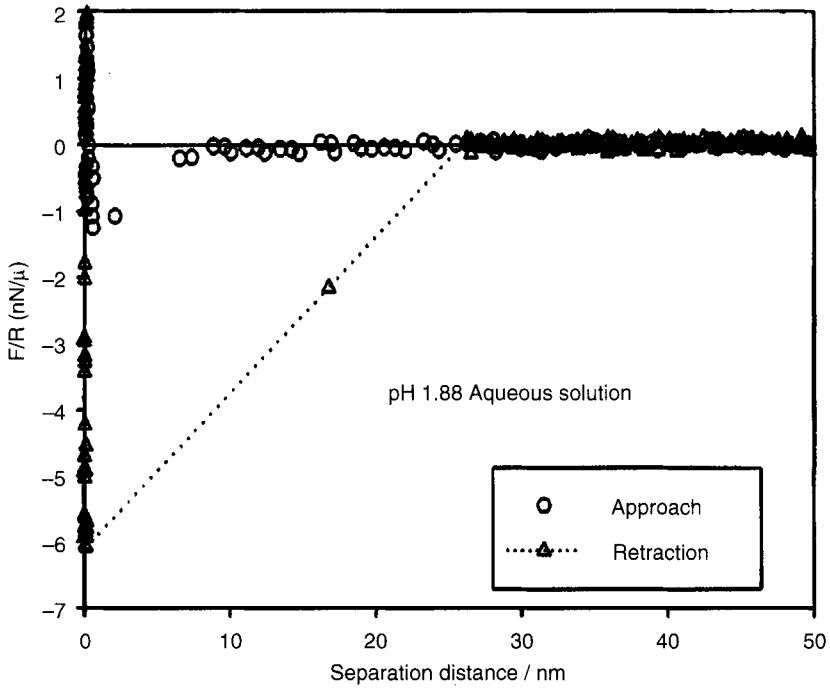



**Figure 1.10.** The normalized force as a function of separation distance between a silicon nitride tip and a silicon surface in an aqueous solution of pH 1.88 containing 0.1 wt% HF [45]. Reproduced with permission of ECS – The Electrochemical Society from Chen, Z. and Singh, R. K., *Journal of the Electrochemical Society*.

hemispherical asperities to represent surface roughness. Theoretically calculated adhesion force correlated well with experimentally measured force between PSL particles and $SiO_2$ surface in both acidic and basic solutions.

## 1.4 Influence of Surface Electrical Charges on Metal Ion Adsorption

Metal ion contamination on silicon oxide or nitride wafers typically occurs by adsorption and/or ion exchange. The extent of contamination is affected by charges developed on the surfaces and the nature of the metal ions (*i.e.* bare, hydrolyzed, cationic, anionic).

The adsorption of metal ions from solutions onto oxide and nitride films causes metallic contamination during wafer processing. According to Loewenstein et al., the adsorption of metal ions on silicon or silicon dioxide occurs by replacement of a hydrogen ion from a hydroxyl group by a metal ion [49]. The adsorption of metal ions can be modeled using basic surface chemical principles [50]. In order to elucidate the adsorption of metal ions onto oxides, it is very important to understand the aqueous chemistry of metal ions in solutions at different pH values. Multivalent bare metal ions such as $Cu^{+2}$ and $Fe^{+3}$ do not exhibit a tendency for adsorption, but the hydrolyzed forms (*e.g.* $Cu_2(OH)_2^{+2}$, $Cu(OH)^+$, $Cu(OH)_2$, $Cu(OH)^{-3}$, $Cu(OH)_4^{-2}$) adsorb strongly at the oxide/water interface. Hence aqueous speciation calculations are critical for modeling metal ion adsorption [51, 52].

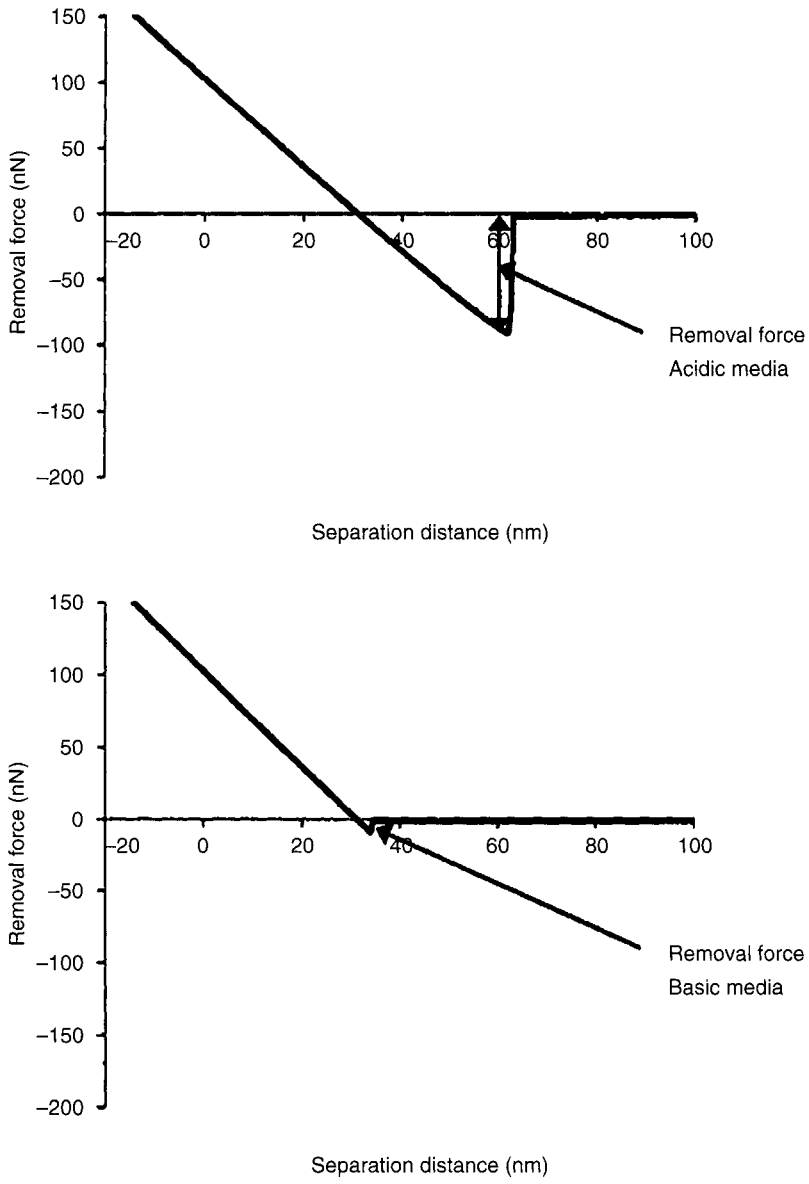



**Figure 1.11.** Interaction forces measured between a polystyrene latex particle and a silicon oxide surface. The upper curve represents the force *vs.* distance curve under acidic conditions. The lower curve is for the same system under basic conditions [48]. Reprinted from *Journal of Colloid and Interface Science*, 228(2), Cooper, K., Gupta A., and Beaudoin, S., "*Substrate Morphology and Particle Adhesion in Reacting Systems*", page 213. Copyright (2000) with permission from Elsevier.

An example of a speciation calculation using commercially available software [53] to obtain the total copper concentration of a 10-ppb solution, is shown in Figure 1.12a. At pH values less than 6, copper is predominantly in the form of the cupric cation ($Cu^{+2}$). Around pH of 6, copper ions begin to hydrolyze and, in the pH range 6–8, they predominantly exist as singly charged $CuOH^{+}$ and neutral $Cu(OH)_2$ species. The precipitation of insoluble CuO begins to occur at a pH of 7.5. In the pH range 8–10, 70% of copper is likely to be insoluble CuO and 30% as soluble $Cu(OH)_2$

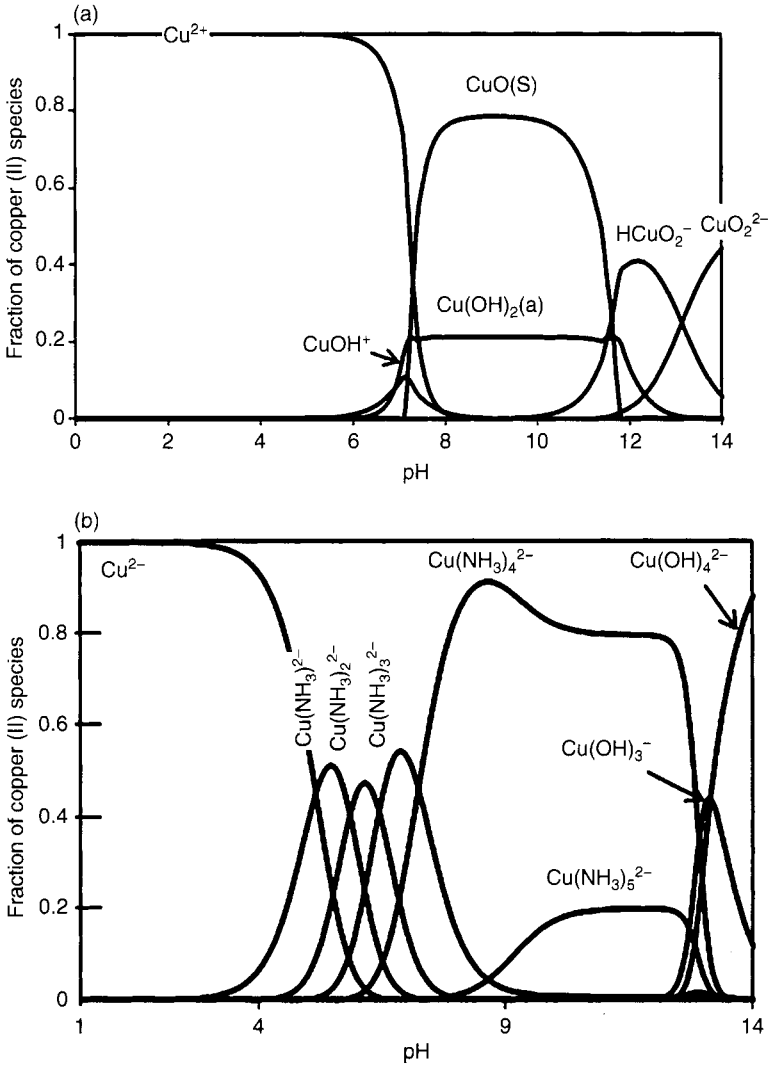



**Figure 1.12.** Speciation of copper in an aqueous solution a) without and b) with 1 M total ammonia, as a function of pH, for a total copper concentration of 10 ppb. Used with permission from the authors.

species. At alkaline values above pH of 11, the copper oxide begins to redissolve forming anionic copper hydroxide species.

The presence of complexing species such as $NH_3$ (*i.e.*, in APM solution) can greatly alter the speciation. Figure 1.12b shows the results of speciation calculations carried out for an aqueous solution containing 10-ppb copper and 1 M ammonia. In the presence of ammonia, a number of soluble Cu-$NH_3$ complexes form. At pH values between 9 and 13, $Cu(NH_3)_4^{+2}$ is the predominant species. Ammonium hydroxide/hydrogen peroxide solutions typically have a pH of ~11 and can induce adsorption of copper in the form of $Cu(NH_3)_4^{+2}$ on a negatively charged chemical silicon oxide film. Similar speciation diagrams for Cu(I) and Cu(II) in ammonium chloride solutions predict the formation of $Cu(NH_3)_3Cl^+$, $Cu(NH_3)_4^{+2}$ and $Cu(NH_3)_5^{+2}$ complexes in alkaline solutions [54].

The adsorption of metal ions can occur by an ion exchange mechanism where the metal ions exchange with hydrogen ions in the surface hydroxyl groups. For adsorption of a metal ion $M^+$ on $SiO_2$, the exchange process can be represented as follows:

$$SiOH(s)+M^+(aq) \leftrightarrow SiOM(s)+H^+(aq) \tag{1.13}$$

The equilibrium constant for the reaction, $K_{exc}$, can be written as:

$$K_{exc} = \frac{\theta_M[H^+]}{\theta_0[M^+]} \tag{1.14}$$

where $\theta_M$ is the fraction of surface sites occupied by the metal ion and $\theta_0$ is the fraction of surface sites in the neutral hydroxylated form. Since the sum of $\theta_0$ and $\theta_M$ equals one, the above equation can be rearranged to:

$$\theta_M = \frac{K_{exc}[M^+]}{[H^+]+K_{exc}[M^+]} \tag{1.15}$$

If the initial number density (number/$m^2$) of hydroxyl groups is denoted as $N$, then the surface concentration of metal ions, $\sigma_m$, is:

$$\sigma_M = N\theta_M \tag{1.16}$$

Using literature $K_{exc}$ values for the interaction of copper ions with silica gels, Lee *et al.*, have modeled the copper ion uptake by chemical silicon oxide wafers at different pH values [55]. The researchers also carried out calculations for copper using ion exchange data for SiOH groups given in Table 1.2. It may be noted that copper can bind with the –SiOH groups to form 1:1 ($SiOCu^+$) or 1:2 ($(SiO)_2Cu$) surface species (complexes). The results obtained for a solution with copper ion

**Table 1.2.** Equilibrium data for ion exchange reactions involving SiOH groups and $Cu^{+2}$ [55]. Used with permission from Material Research Society, reprinted from Lee, W., Torek, K. J., Palsulich, D. A., and Weston, L., *Science and Technology of Semiconductor Surface Preparation, Mat. Res. Soc. Symp. Proc.*, Volume 477(1977) page 57.

| Equilibrium reaction | Log k |
|---|---|
| $SiOH + H^+ \rightarrow SiOH_2^+$ | 0.7 |
| $SiOH \rightarrow SiO^- + H^+$ | –3.9 |
| $SiOH + Cu^{+2} \rightarrow SiOCu^+ + H^+$ | –5.52 |
| $2\,SiOH + Cu^{+2} \rightarrow (SiO)_2Cu + 2H^+$ | –11.19 |

concentration of 10 ppb are shown in Figure 1.13. The results of the computation show:

1. The highest level of copper uptake occurs in the pH range of ~ 5.5 to ~9.5.
2. In the same pH range, the (surface) concentration of copper occupied sites is very small compared to the concentration of negative sites.

In two seminal papers, James and Healy provided excellent discussions of the adsorption of hydrolyzable metal ions on oxide surfaces [56, 57]. They measured the adsorption behavior of cations ($Ca^{+2}$, $Co^{+2}$, $Fe^{+3}$, $La^{+3}$ and $Th^{+4}$) on silica. The effects of the adsorbed ions on the zeta potential of silica were also determined. For each metal ion, there was a critical pH where adsorption increased steeply over a very narrow pH range. This critical pH is usually just below the pH of the formation of bulk hydrolysis products. In the case of some metal ions, three isoelectric points were measured.

A multicomponent Langmuir model has been used to model competitive adsorption of metal ions and hydrogen ions onto oxidized silicon surfaces [49]. Representing the interaction constant of ions of type '*i*' by $K_i$, the fraction of surface covered by ions of type '*i*' is given by:

$$\theta_i = \frac{K_i[M^{i+}]}{1+\Sigma_i K_i[M^{i+}]} \tag{1.17}$$

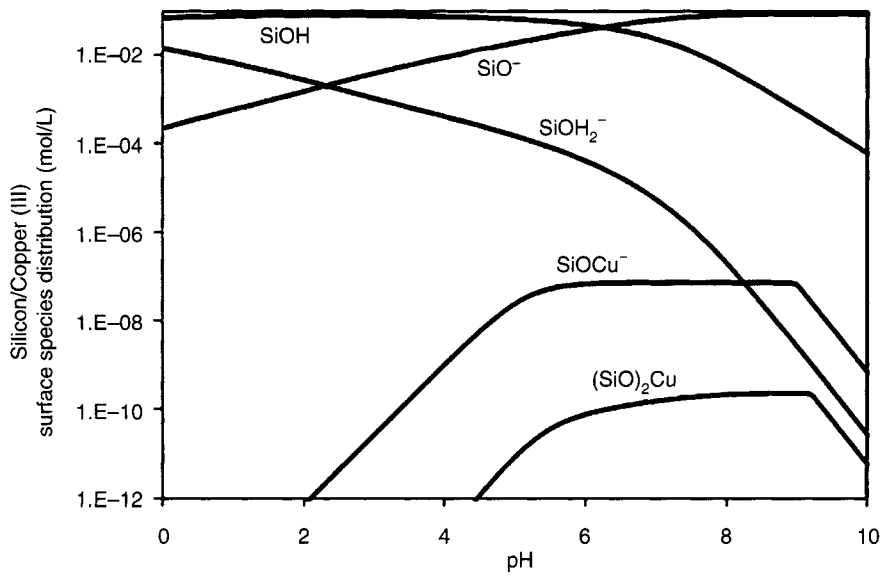



**Figure 1.13.** Distribution of surface species as a function of pH when copper adsorbs on silica. For [Cu] = 10 ppb, $SiO_2$ = 1 M, surface area = 9613 $cm^2$ and 0.0871 M surface sites. Used with permission from the authors.

Unfortunately, pH-dependent speciation of the adsorbing metal ions has not been considered in this work. As pointed out earlier, hydrolysis of metal ions is pH dependent, and hydrolyzed metal ions exhibit much stronger adsorption on surfaces.

## 1.5 Wettability of Surfaces

### 1.5.1 Surface Tension and Surface Energy

Films that are cleaned and dried may be either high energy surfaces such as oxides, nitrides, and metals or low energy surfaces such as hydrogen terminated silicon, photoresists, and low-κ (low dielectric constant) materials or a combination of both types of surfaces. In some unique situations such as the etching of silicon by hydrofluoric acid, the high energy surface of silicon could be rendered into a low energy surface by hydrogen termination. Most liquid chemical formulations used in wet processing are aqueous solutions with surface tension of less than 72 mN/m (water has a surface tension of 73 mN/m [dyne/cm] at 20°C). However, buffered hydrogen fluoride solutions may have surface tension as high as 90 mN/m. Since more than one type of film may be exposed during a cleaning step, chemical formulations must be tailored to wet all of the surfaces that are involved. One of the film characteristics that aids in the choice of chemical formulations is the critical surface tension of wetting, $\gamma_c$. Liquid chemicals that have a surface tension equal to or less than $\gamma_c$ will completely wet the solid. The determination of $\gamma_c$ is typically done by the Zisman method [58]. In this method, contact angle ($\theta$) of liquids or liquid mixtures of different surface tension on the surface of interest are measured, and a plot of cos $\theta$ versus surface tension is made. The surface tension of the liquid that gives a value of 1 for cos $\theta$ is designated as the $\gamma_c$ of that surface.

The critical surface tension of wetting of an HF-etched silicon surface has been reported [59]. In this study, methanol/water solutions of different compositions containing 1 wt% HF with surface tensions in the range of 72–23 mN/m were used, and the surface tension results are shown in Figure 1.14. Using the Zisman method, the critical surface tension of wetting has been determined to be approximately 27 mN/m.

### 1.5.2 Adsorption Characteristics and Wettability Modification

Surface active agents or surfactants are added to cleaning formulations for a variety of reasons including reduction of surface tension for modification of wettability of surfaces, and prevention of particle deposition as well as plating of metal ions. Typically, these agents are organic chemicals with a hydrophobic tail and a hydrophilic head. For surfactants that are used in wafer cleaning, the hydrophobic part of the molecule typically contains alkyl and/or phenol groups along with hydrophilic groups such as polyethylene oxide or polyglycidol to control the hydrophilic-lipophilic balance (HLB). The hydrophilic head is either a neutral hydroxyl (–OH) functionality or anionic carboxyl group. Cationic surfactants are not used in wafer cleaning since they tend to adsorb on almost all polymeric surfaces such as cassettes. Surfactants that cause significant foaming can leave stains on the wafer surface if not removed properly after wafer cleaning [60]. To reduce or eliminate foaming, defoamers may

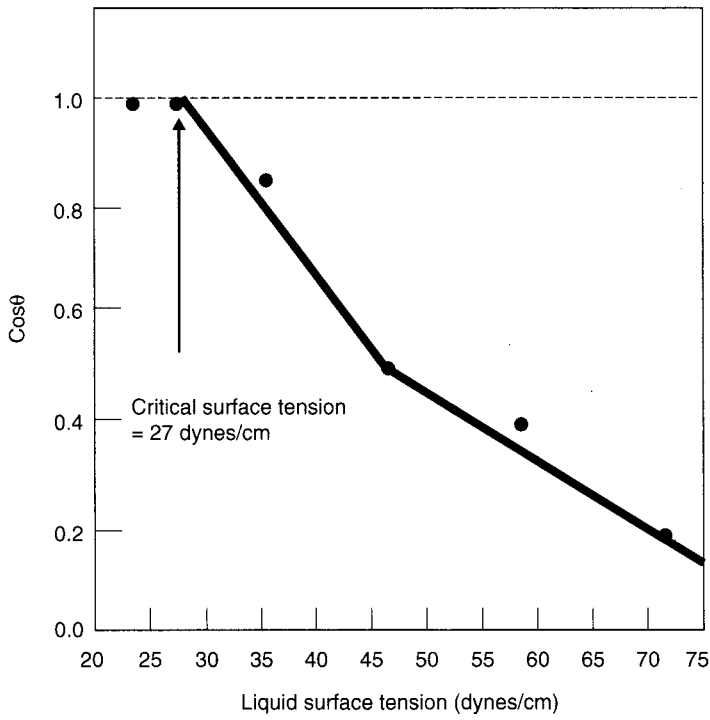


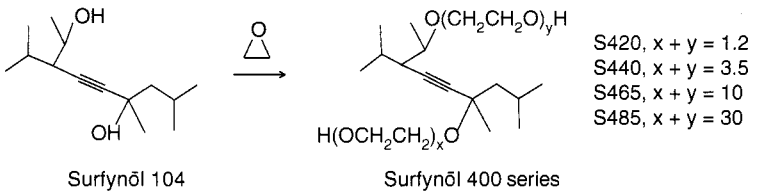

**Figure 1.14.** Zisman plot for methanol-water solutions on a silicon substrate. Plot gives $\gamma_c$ = 27 dyne/cm [59]. Redrawn with permission of ECS – The Electrochemical Society from Gould, G. and Irene, E. A., *Journal of the Electrochemical Society.*

be added. Hydrofluoric acid-based etching or cleaning solutions may contain anionic or non-ionic surfactants for improving wettability of silicon [61] and a hydrophobic base to enhance penetration of trenches. Block copolymers containing polyethylene oxide (PEO) and polypropylene oxide (PPO) groups can also be used as surfactants. Chapter 4 discusses the uses of surfactants in cleaning solutions. Some generic structures of surfactants of interest to wafer cleaning are listed in Table 1.3.

Surfactants have a tendency to adsorb at solution/air and solid/liquid interfaces resulting in the reduction of interfacial tension [62] [63]. In Figure 1.15, the surface tension of 1 wt% HF solution is shown as a function of the concentration of a polyglycidol based nonionic surfactant (Arch Chemicals Inc.OHS®) [64]. The graph shows that by adding a surfactant the surface tension of HF can be significantly reduced even at very low (tens of ppm) concentrations. The critical micelle concentration (CMC) may be estimated to be roughly 90 ppm. Increasing the ionic strength of a cleaning solution will decrease the CMC of the surfactant [65]. The CMC value of a given surfactant would be lower in BHF solutions that have much higher ionic strengths than an HF solution without another component.

Surfactant adsorption at a solid/liquid interface can modify the wettability of the surface. Dynamic contact angle measurements carried out using a Wilhelmy plate technique on hydrogen-terminated silicon show a broad hysteresis loop in deionized water – the advancing and receding angles are 87° and 61°, respectively, as shown in Figure 1.16a [64]. The contact angles in 100:1 HF solution have

**Table 1.3.** Generic structures of some surfactants of interest to wafer cleaning.

| Surfactant | Generic Structure |
|---|---|
| *Non ionic* | |
| Alkyl phenoxy polyglycidol (OHS®) | R-Ph-O-$(CH_2CH(OH)CH_2O)_n$-H |
| Acetylenic alcohols (Surfynol) |  |
| Alkyl phenoxy polyethylene alcohols (NCW) | $RO(CH_2CH_2O)_l(CH(CH_3)CH_2O)_m(CH_2CH_2O)_nH$<br>$R = C_{12}H_{25}/C_{14}H_{29}$, l + n = 10, m = 4.5 |
| *Anionic* | |
| Low chain carboxylates | R-COO- M+, where R = hydrocarbon or a fluorocarbon |

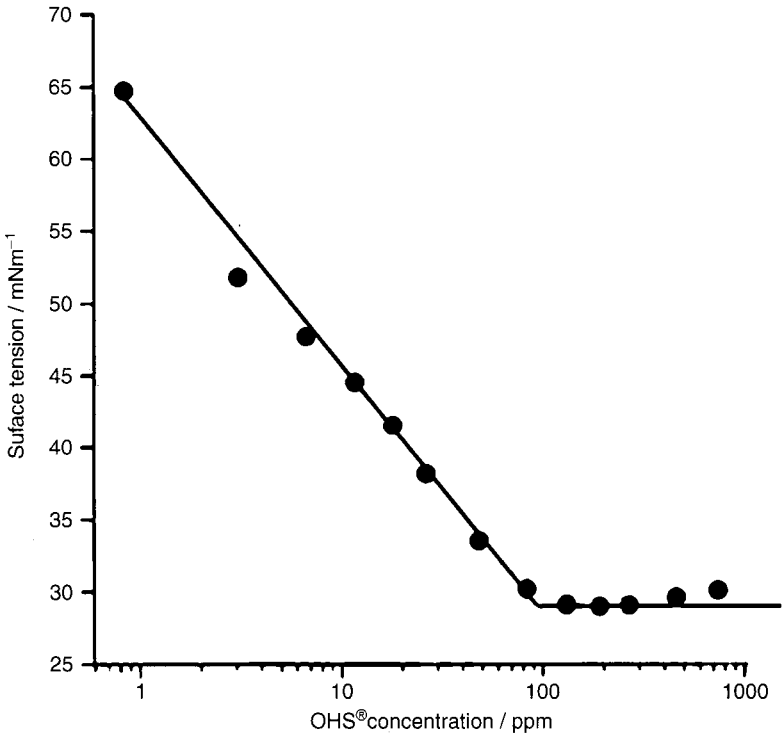



**Figure 1.15.** Surface tension *vs.* concentration of a nonionic surfactant in 1 wt% HF solution [64]. Reproduced with permission of ECS – The Electrochemical Society from Haworth, P., Kovach, M., Sperline, R., and Raghavan, S., *Journal of the Electrochemical Society*.

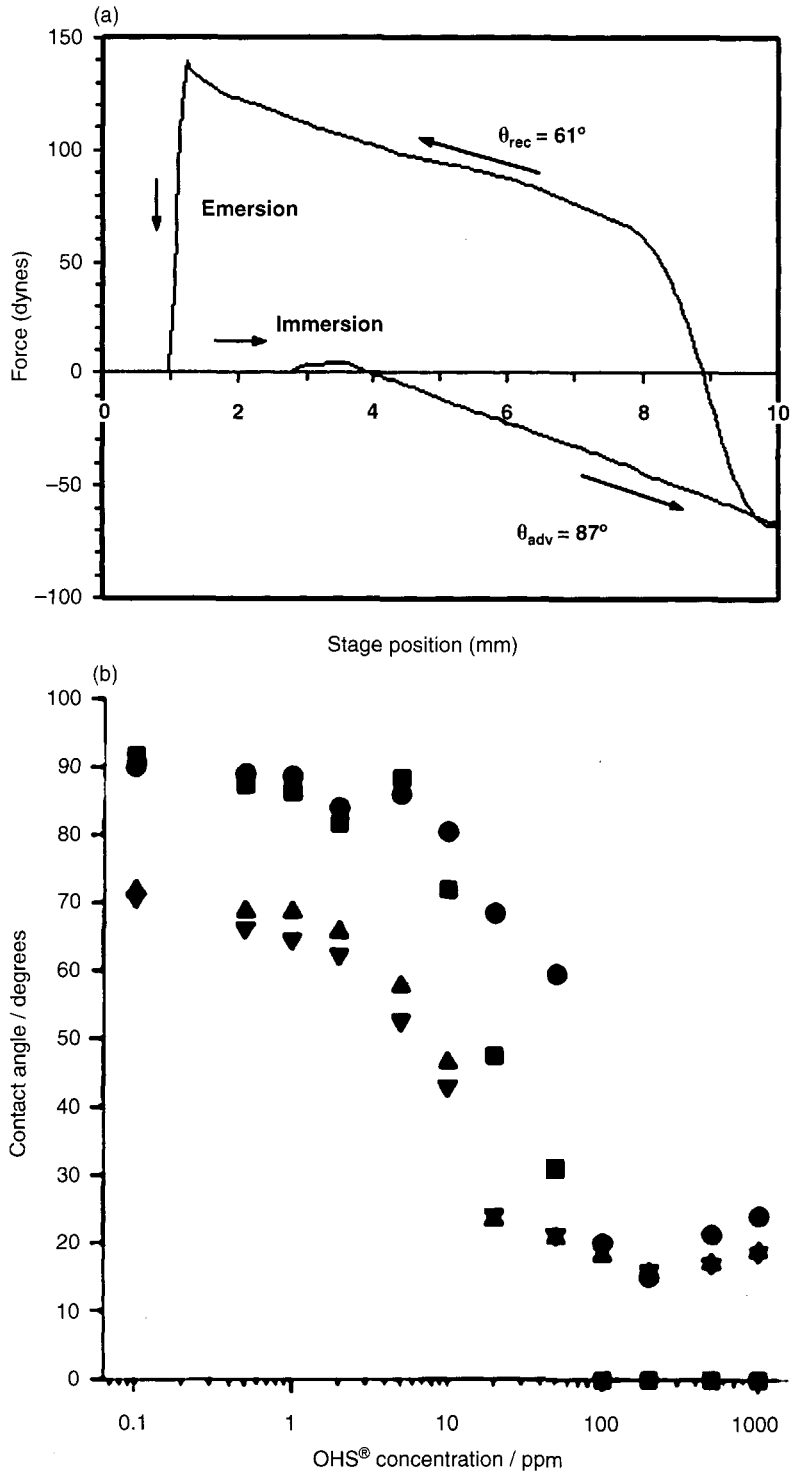



**Figure 1.16.** Advancing and receding contact angles of a) DIW on hydrogen terminated silicon, and b) 100:1 HF on silicon as a function of OHS® concentration (●) cycle 1 advancing, (■) cycle 2 advancing, (▲) cycle 1 receding, (▼) cycle 2 receding [64]. a) Used with permission from authors. b) Reproduced with permission of ECS – The Electrochemical Society from Haworth, P., Kovach, M., Sperline, R., and Raghavan, S., *Journal of the Electrochemical Society.*

been measured to be approximately the same. When 10 ppm of OHS® surfactant is added to a 100:1 HF solution, the advancing and receding angles decrease to 74° and 44°, respectively, clearly confirming enhanced wettability (as shown in Figure 1.16b). At a value close to the CMC of the surfactant, the surface becomes highly wettable with solution contact angles less than 20°. Interestingly, when two immersion cycles are used, the advancing contact angle becomes zero during the second cycle (the square data points in Figure 1.16b).

The adsorption/desorption characteristics of surfactants on silicon has been investigated [66, 67] using attenuated total reflection-Fourier transform infrared spectroscopy (ATR-FTIR) [68, 69]. Interaction of hydrocarbon surfactants such as poly(ethylene oxide alcohol) and polyglycidol-type surfactant (OHS®) with hydrofluoric acid can be followed by monitoring the intensity of –C-H peaks in the 2800–3000 $cm^{-1}$ range. In BHF solutions, absorption due to –N-H groups from $NH_4^+$ ions in solution strongly interferes with the –C-H peaks in adsorbed surfactant species. The N-H stretching is lowered from 3200 $cm^{-1}$ to 2850 $cm^{-1}$ due to hydrogen bonding [70, 71]. A technique based on replacement of the ammonium ions close to the silicon surface by alkali cations has been demonstrated to overcome the interference due to the large number of $NH_4^+$ ions in solution [67]. A comparison of adsorption density of OHS® onto silicon from 7:1 BHF solution (7 parts of $NH_4F$ [40 wt%] and 1 part of HF [49 wt%]) with that from 50:1 HF solutions for various OHS® concentrations is shown in Table 1.4. The adsorption from BHF solution is approximately 20% higher than that from dilute HF solutions.

## 1.6 High Aspect Ratio Cleaning: Narrow Structures

Wet chemical cleaning of narrow vias and trenches requires efficient, complete, and fast penetration of cleaning chemicals. Thus, both thermodynamic and kinetic factors are important. Liquid penetration by capillary effect primarily

**Table 1.4.** Comparison of OHS® equilibrium adsorption densities onto silicon from 50:1 HF solutions and 7:1 BHF solutions [67]. Reprinted with permission from Almanza-Workman, A., Raghavan, S., and Sperline, R., *Langmuir*, 16(6):3636. Copyright 2000 American Chemical Society.

| Surfactant (OHS®) concentration (ppm) | Equilibrium adsorption onto silicon $\Gamma_{OHS}$® (mol/cm²) | |
|---|---|---|
| | 50:1 HF (I ~ 1.4 M) | 7:1 BHF (I ~ 12 M) |
| 5 | $9.13 \times 10^{-11} \pm 0.5 \times 10^{-11}$ | $1.15 \times 10^{-10}$ (using KF/HF, I ~ 8 M)<br>$1.17 \times 10^{-10}$ (using CsF/HF, I ~ 12 M) |
| 100 | $1.59 \times 10^{-10} \pm 0.1 \times 10^{-10}$ | $1.93 \times 10^{-10}$ (using KF/HF, I ~ 8 M)<br>$1.91 \times 10^{-10}$ (using CsF/HF, I ~ 12 M) |
| 500 | $2.93 \times 10^{-10} \pm 0.2 \times 10^{-10}$ | $3.66 \times 10^{-10}$ (using KF/HF, I ~ 8 M)<br>$3.58 \times 10^{-10}$ (using CsF/HF, I ~ 12 M) |

I = calculated ionic strength in solution

depends upon the contact angle of the liquid on the walls of the vias/trenches, which should be as small as possible. It is also important for the liquid surface tension to be roughly the same as the critical surface tension of wetting of the via/trench material. The rate of penetration is controlled by contact angle, feature dimensions, and viscosity of the liquid. Narrower and deeper trenches can be expected to have lower rates of liquid penetration making cleaning of high aspect ratio features difficult.

### 1.6.1 Rate of Liquid Penetration into Narrow Structures

The rate of advance of liquid into an air-filled via, theoretically of any width, can be calculated using Rideal-Washburn equation [72, 73]:

$$\frac{dl}{dt} = \frac{r\gamma cos\theta}{4\eta l} \tag{1.18}$$

where $r$, $\gamma$, $h$, $l$, $\theta$ refer to the radius of the via, the surface tension of the liquid, the viscosity of the liquid, length of the via and contact angle of the liquid on the solid, respectively. This equation can be easily derived from Poiseuille's equation of flow through a capillary tube assuming that the driving pressure is due to positive Laplace pressure (= 2 $\gamma$ $cos\theta$/ $r$), and the liquid-vapor meniscus is hemispherical. Equation 1.18 can be integrated and rearranged to calculate time for complete penetration into the via as follows:

$$t = \frac{2\eta l^2}{r\gamma cos\theta} \tag{1.19}$$

As evident from the above equation, smaller values of $\gamma$ $cos\theta$ increase the time required for filling of hydrophilic vias (for hydrophobic [$\theta > 90°$] vias, Laplace pressure is negative) .

Olim derived an expression for filling of hydrophilic trenches (of width $w$) closed at one end [74]. His derivation is based on the fact that hydrophilic walls of the feature create a concave surface at the gas/liquid interface and the resulting Laplace pressure increases the pressure in the gas trapped in the feature. The pressurized gas dissolves into the liquid, thus, allowing the liquid to fill the feature.

To estimate the upper bound of the time required to fill the feature, Olim made the following assumptions:

1. The gas/liquid interface is saturated.
2. The process is isothermal.
3. There is no change in curvature of liquid/vapor interface.
4. The rate of gas diffusion from the interface into the liquid is proportional to the concentration gradient at the interface, $dC/dn$ where $C$ is the molar concentration of the dissolved gas and $n$ is distance normal to the interface.

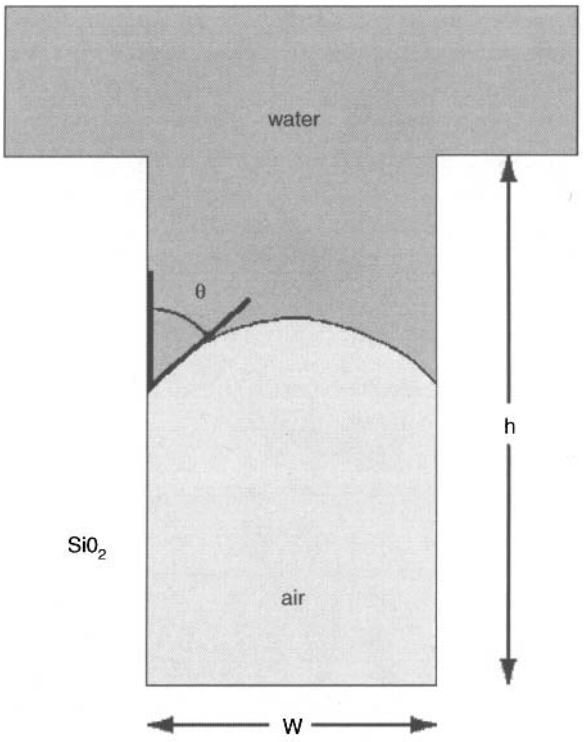



**Figure 1.17.** Schematic showing feature wetting of a high aspect ratio via or contact [74]. Where $w$ is the width, $h$ is the height and θ is the contact angle. This shows a low surface energy solution with a convex angle indicating a hydrophilic surface. Reproduced with permission of ECS – The Electrochemical Society from Olim, M., *Journal of the Electrochemical Society*.

The conditions at which this gradient is minimized yields the slowest diffusion rate and that in turn yields an upper limit on the value of the time interval required for the liquid to fill the feature, $\Delta t_{fill,max}$, which is given by [74]:

$$\Delta t_{fill,max} = \frac{k}{DRT}\left[1+\frac{P_h}{\Delta P}\right]h^2 \tag{1.20}$$

where $k$, $D$, $R$, $T$, $P_h$, $\Delta P$, *and* $h$ are Henry's constant, diffusion coefficient of the gas in the liquid, universal gas constant, gas temperature, atmospheric pressure, pressure difference across the liquid gas interface, and feature depth, respectively.

Replacing $\Delta P$ by $2\gamma cos\theta/w$, Eq. 1.20 becomes:

$$[\![\Delta t]\!]_{(fill,max)} = k/DRT[1+(P_{hw})/2(cos\theta)h^2 \tag{1.21}$$

It may be noticed from Eq.1.21 that maximum filling time is a function of feature dimensions $h$ and $w$, surface tension of the liquid filling the feature $\gamma$, contact angle at the liquid- vapor interface $\theta$, Henry's constant $k$, diffusion coefficient, $D$, of gas in

liquid and temperature of liquid. The equation predicts a filling time of ~1 sec for water at 300 K in trenches 0.5 μm wide and 4 μm deep. The filling time increases for narrower and deeper trenches and can go up to ~10 sec for features 1 μm wide and 10 μm deep.

Ota *et al.* predicted the liquid infiltration rate into wettable and non-wettable 2-μm deep trenches/microholes in the size range of 0.2 to 1.6 μm [75]. The model for infiltration rate was based on the overall force balance due to liquid pressure, gas pressure inside the trench prior and during the fill process, and the Laplace pressure. The overall force ($F$) balance during initial infiltration stage for non-wetting and wetting liquids is given by Eq. 1.22 and 1.23, respectively. In these equations, the first two terms on the right refer to liquid pressure, the second term to gas pressure inside the microhole, and the third term to pressure due to surface tension:

$$F = \left\{ P_0 \pi \left(\frac{d}{2}\right)^2 + s\rho g \left(\frac{d}{2}\right)^2 \right\} - P_i \pi \left(\frac{d}{2}\right)^2 - T \sin\alpha \, 2\pi \left(\frac{d}{2}\right) \tag{1.22}$$

$$F = \left\{ P_0 \pi \left(\frac{d}{2}\right)^2 + s\rho g \left(\frac{d}{2}\right)^2 \right\} - P_i \pi \left(\frac{d}{2}\right)^2 + T \cos\beta \, 2\pi \left(\frac{d}{2}\right) \tag{1.23}$$

In the above equations, $d$ is the microhole diameter, $P_0$ is the outside liquid pressure, $P_i$ is the inside gas pressure, $s$ is the liquid thickness above the microhole, $\rho$ is the liquid density, $g$ is the acceleration due to gravity, $T$ is the liquid surface tension, and $\alpha$ and $\beta$ are the contact angles of liquid on non-wettable and wettable microholes respectively.

Since, $P_0 = P_i$ initially, and assuming pressure due to liquid head ($s\rho g$) to be negligible, Eq. 1.22 and Eq. 1.23 convert to

$$F = -T \sin\alpha \, 2\pi \left(\frac{d}{2}\right) < 0 \tag{1.24}$$

$$F = +T \cos\beta \, 2\pi \left(\frac{d}{2}\right) > 0 \tag{1.25}$$

The net negative force for non-wettable surface suggests that liquid does not infiltrate into microhole of such a surface. On the other hand, net positive force for wettable surface indicates that liquid is able to penetrate into a microhole irrespective of its size.

As the liquid starts penetrating into the wettable micropore, the pressure inside the gas phase in the micropore increases and at equilibrium, the liquid penetrates to a depth $h$. The force balance in this case is:

$$F = \left\{ P_0 \pi \left(\frac{d}{2}\right)^2 + h\rho g \left(\frac{d}{2}\right)^2 \right\} - P_i \pi \left(\frac{d}{2}\right)^2 + T \cos\beta \, 2\pi \left(\frac{d}{2}\right) = 0 \tag{1.26}$$

Considering $h\rho g$ being negligible compared to other terms in the equation, Eq. 1.27 is obtained. Additionally, a force balance between pressure inside the gas phase in

the microhole and the water pressure yields Eq. 1.28, where $L$ is the total depth of the microhole and $P_{oa}$ is the initial pressure in the gas phase of the microhole:

$$\left\{(P_0 - P_i) + \frac{4T}{d}\cos\beta\right\} = 0 \tag{1.27}$$

$$P_i(L-h) = P_{oa}L \tag{1.28}$$

Combining Eq. 1.27 and Eq. 1.28, and assuming that no dissolution of gas occurs (different from Olim's approach [74]) in the liquid inside the microhole, Eq. 1.29 is obtained:

$$\frac{h}{L} = 1 - \frac{1}{\frac{P_o}{P_{oa}} + \frac{4T\cos\beta}{P_{02}d}} \tag{1.29}$$

This equation shows that the extent of liquid infiltration (which Ota and Tsutsumi describe as infiltration rate), $h/L$, depends on initial pressure in the gas phase of the microhole, liquid pressure, surface tension of the liquid, micropore size, and contact angle of liquid on the microhole surface. Conditions that will promote good penetration ($h/L$ approaching 1) include low values of $P_{oa}$, $d$, and $\beta$, and high values of $T$. The authors of [75] have shown experimentally that the extent of liquid infiltration is about 0.75 for wettable microholes (contact angle = 28°) in the size range of 0.2 to 1.0 μm. The experimentally determined infiltration values matched well to those predicted with the theoretical model.

### 1.6.2 Enhancement of Liquid Penetration into Narrow Structures

Efficient cleaning of surfaces and deep vias/trenches is critical to the semiconductor industry. Considerable work has been done to understand particle/ionic contaminant removal mechanisms in megasonic cleaning of both blanket and patterned wafers [76, 77]. It has been shown that oscillating flow (vortex oscillating mechanism) generated in a megasonic process provides a significant advantage in terms of reducing the rinsing time for patterned wafer cleaning [77].

## 1.7 Surface Tension Gradient: Application to Drying

Drying is an integral part of cleaning. Improper drying can leave watermarks on a wafer surface that can act as undesirable masks during subsequent processing, such as etching and deposition [78, 79]. Additional challenges exist in drying surfaces that consist of hydrophilic and hydrophobic regions in close proximity. Spin drying does not reduce the thickness of the water layer on a hydrophilic wafer below 0.5 μm in the typical wet processing time. Using evaporation to remove this water layer is known to leave watermarks on the surface. To reduce or prevent the formation of these watermarks, drying based on a surface tension gradient by use of isopropyl alcohol is commonly carried out as discussed in the following section.

### 1.7.1 Isopropyl Alcohol Surface Tension Gradient Drying

One of the most important steps in wet processing of wafers is drying. While the use of isopropyl alcohol (IPA) in removing water from wafer surfaces has been practiced for over three decades, the manner in which isopropyl alcohol is used has changed significantly [80]. Drying methods based on IPA to remove water from wet wafers include condensation of hot IPA on a wafer to "dissolve away" water [81], direct displacement of water by liquid IPA [82], and creation of a surface tension gradient using dilute IPA vapor at ambient temperature [83–85]. Drying by condensation of hot IPA vapor in almost pure form or of an azeotropic composition by condensing on the wafer – vapor drying, has been replaced by drying using IPA vapors, typically in an $N_2$ atmosphere, at ambient temperatures, condensing the IPA on the water surface, in which the wafers are submerged, and then slowly raising the wafers (or lowing the water). This latter drying method, known as surface tension gradient (STG) drying or Marangoni drying, is based on the ability of IPA to reduce the surface tension of water along with the creation of gradient of surface tension on a water meniscus formed on a wafer surface.

The creation of a surface tension gradient on a water meniscus (*i.e.* water/vapor interface) formed on a hydrophilic wafer is shown in Figure 1.18. Exposure of this meniscus to IPA vapor (typically diluted with nitrogen to 1–2 vol%) results in the adsorption of IPA molecules at the water/vapor interface. Since IPA is soluble in water, the adsorbed IPA molecules tend to diffuse into the bulk water. As shown in Figure 1.18, at a location far away from the wafer surface (*C*), diffusion of adsorbed IPA molecules into the water would result in a low density of molecules on the surface. In a region very close to the wafer surface (*A*), diffusion of IPA molecules is reduced due to the very thin water layer; consequently, the surface concentration of molecules is larger than that in region *C*. In the region *B*, the surface concentration of IPA molecules would be between that in region *A* and region *C*. Variation in the surface concentration of IPA molecules would result in a gradient of increasing surface tension from region *A* to *C*. In an attempt to reach equilibrium, the IPA molecules flow from region *A* towards region *C* and carry water molecules with them. This movement creates motion of a few subsurface layers dictated by the fact that the surface tension force is balanced by viscous forces. Once the water is stripped away by the surface tension effect, the IPA easily evaporates, and the wafer is rendered dry.

The surface tension of water/IPA solutions is plotted in Figure 1.19 as a function of volume percent of IPA in solution [83]. Addition of IPA in water up to 20 vol% decreases the surface tension of water steadily from 72 mN/m to roughly 32 mN/m. This is due to the population of IPA molecules at the solution/air interface. Beyond 25 vol% IPA, the change in surface tension is minimal due to progressive saturation of the interface with IPA molecules.

### 1.7.2 Water Layer After Drying

"Stripping" of layers of water by the surface tension gradient effect dries the wafer. In order to maintain the STG effect, there has to be relative motion between the wafer and the water in the rinse bath. A fluid mechanics based model relevant to

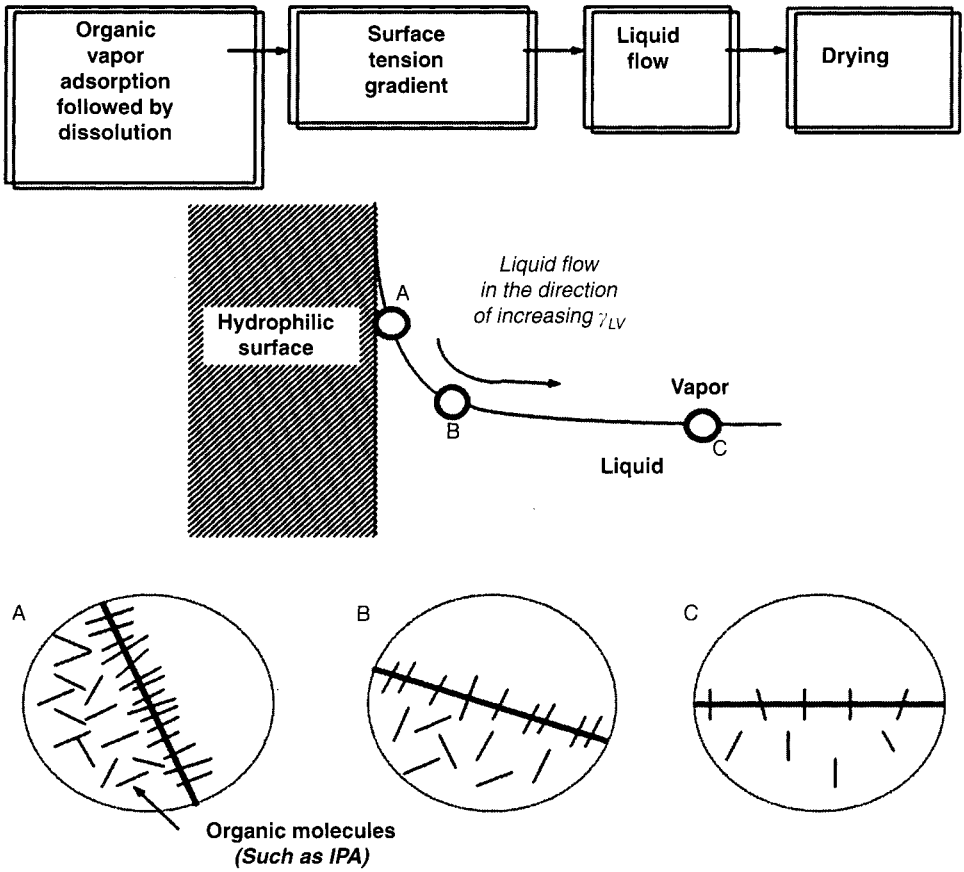



**Figure 1.18.** Schematic figure showing the surface tension gradient at the liquid-vapor interface on a hydrophilic surface. The difference in surface concentrations of IPA molecules at three locations *A, B, and C* is also illustrated. Used with permission from the authors.

Marangoni drying has been developed by Thess and Boos [85]. This model which assumes that the surface tension distribution is a known function of position and attempts to explain the movement of a thin liquid film on a flat plate that is vertically withdrawn from a large liquid reservoir in the presence of a surface tension gradient.

The beneficial effects of IPA in reducing the thickness of the evaporated water layer have been elegantly shown by researchers at FSI. Figure 1.20 clearly shows that low liquid drain rates (rate of movement of liquid/vapor interface along the wafer) of 1 to 2 mm/sec along with IPA vapor can tremendously reduce the thickness of the water layer.

### 1.7.3 Alternate Chemicals for Drying

In principle, any organic vapor that is capable of adsorbing at the water/vapor interface as well as dissolving in water could be used for STG drying. However, the work of Marra *et al* [83] showed that the efficacy of organic vapors meeting

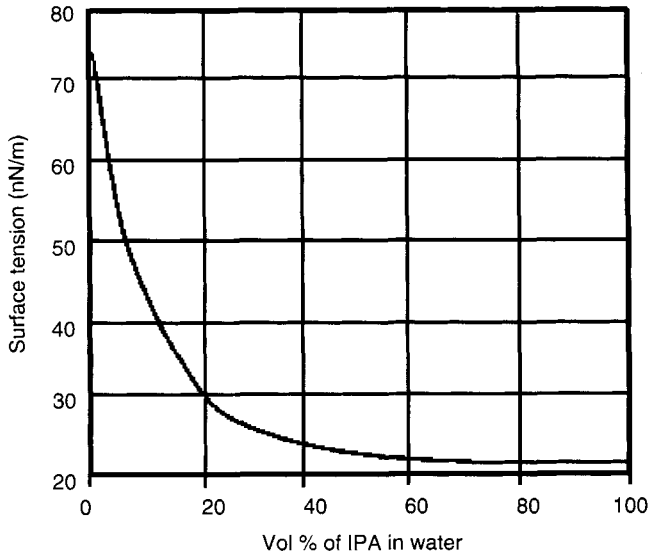



**Figure 1.19.** Surface tension of water (mN/m) as a function of volume percent of IPA in water [87]. Used with permission from Jin-Goo Park.

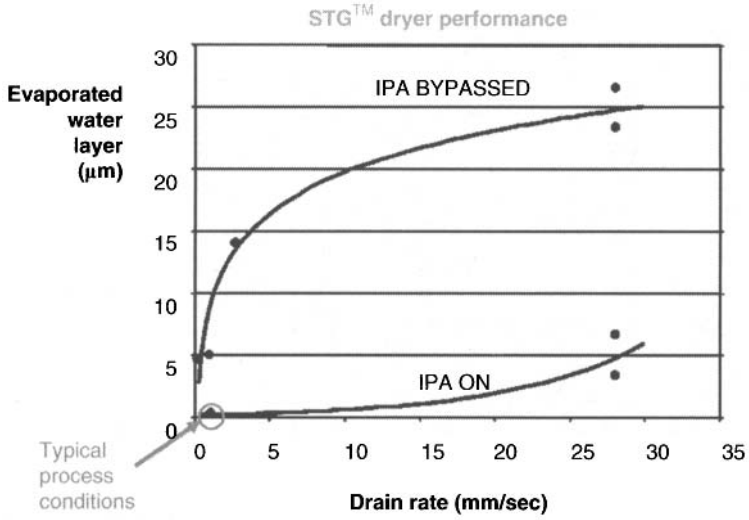



**Figure 1.20.** Effect of liquid drain rates along with IPA vapor on thickness of water layer. Courtesy of FSI International, Inc.

both of these criteria in providing drying varies widely. For example, they found acetone to be less effective than IPA. Leenaars *et al.* compared the drying performance of several organic vapors and emphasized the importance of optimum vapor pressure and water solubility of vapors in drying of wafers [88]. Table 1.5 provides selected physical constants and drying results for organic solvent investigated by these authors [88, 89]. To date, the reason for the superior

**Table 1.5.** Marangoni drying result and selected physical constants for various organic vapors. Table adapted from [88, 89].

| Solvent | Drying Result | Saturation Vapor Pressure (mbar) | Solubility (g/L of water) | Surface Tension of Solvent $mNm^{-1}$ |
|---|---|---|---|---|
| 2-Proponal | + | 43 | Complete | 20.93 |
| 1-Proponal | + | 19 | Complete | 23.32 |
| 2-Butanol | +/− | 17 | 125 | 22.54 |
| 1-Hexanol | +/− | 1 | 5.8 | 25.81 |
| 1-Heptanol | _ | 0.5–1 | <1 | 38.50 |
| 1-Octanol | _ | 0.3 | 0.54 | 27.10 |
| Hexane | _ | 160 | 0.05 | 17.89 |
| Tetrachloro-Methane | _ | 120 | 0.8 | 26.43 |
| Octane | _ | 15 | 0.1 | 21.14 |
| Diethyl Ether | _ | 587 | 12 | 16.65 |
| Ethyl Acetate | ++ | 97 | 80 | 23.39 |
| Butyl Acetate | ++ | 13 | 10 | 24.88 |
| Methyl Isobutyl Ketone | ++ | 6.7 | 19 | 25.45 |
| Acetone | + | 233 | Complete | 22.72 |
| Tetrahydrofuran | ++ | 200 | Complete | 23.97 |
| 2-Ethoxy Ethanol | ++ | 5 | Complete | 28.35 |
| Diacetone Alcohol | ++ | 1.5 | Complete | 24.88 |
| 1-Methyl -2-Pyrrolidone | + | 0.3 | Complete | 28.91 |
| Ethylene Glycol | _ | 0.06 | Complete | 47.99 |
| Nitrogen | _ | 1000 | 0.02 | – |

Vapor flow of 6 L/min, drying result: '−' = bad, '+/−' = moderate, '+' = good, '++' = excellent, solubility/vapor pressure at 20°C, surface tension at 25°C

performance of IPA in providing drying by STG effect has not been clearly established. Because of flammability issues related to IPA (flash point of IPA is ~12°C), there has been interest in replacing IPA with nonflammable liquids such as methoxy–nonafluorobutane based fluids, manufactured by 3M under the trade name Novec™.

## 1.8 Summary

In this chapter, we have reviewed some of the fundamentals of surface chemical concepts involved in wet chemical cleaning and drying of surfaces pertinent to integrated circuit fabrication. Improvement in cleaning and drying of surfaces is possible through a basic understanding of interfacial phenomena. It is pertinent to mention that much of the fundamental principles described in this chapter were known as early as the 1950's. However, due credit must be given to the semiconductor industry for taking these principles further and implementing them in wafer cleaning and drying applications.

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# 2

# The Chemistry of Wet Cleaning

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*Abstract*
Aqueous-based cleaning for microelectronics fabrication is the most prevalent process step in integrated circuit manufacturing, approximately 2–3 times per masking layer. These steps are composed of one or more cleaning processes that can be used in different order to provide different results depending on the sequence and the chemicals used. This chapter provides in depth discussions of the chemistry of the primary cleaning solutions; SC-1 (APM), SC-2 (HPM), SPM, and HF; their composition and purpose. The reaction mechanism, the chemical reactions and reactivity, and the sensitivity of chemical composition with respect to each of these processes are explained.

***Keywords:*** wet cleaning, photoresist stripping, critical cleaning, SC-1, APM, SC-2, HPM, SPM, Piranha, reaction mechanism, concentration control

## 2.1 Introduction to Aqueous Cleaning

The majority of cleaning in a microelectronics fabrication area is performed with liquids, primarily water, the most abundant molecule on the earth. On average wet cleaning and surface conditioning are used 2–3 times per masking layer. Other liquids are used for cleaning, but water surpasses all others. Chemicals, both gases and liquids, can be mixed into the water, or water added to dilute chemicals. This Chapter covers the chemistry of aqueous-based cleaning solutions. Chapter 3 covers the chemistry of aqueous-based etching solutions.

### 2.1.1 Background of Aqueous Cleaning Chemistry

Since gas is a poor medium to transport contaminants away from the wafer surface, most of the liquid use for microelectronic cleaning is water. However, other liquids are used. Organic solvents such as isopropyl alcohol (IPA) and N-methyl pyrrolidone (NMP) are employed as well as semi-aqueous chemical mixtures, as

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discussed in Chapter 4. Pure water has many advantages over any other solvent – it is cheap, easy available, non-flammable, non-toxic, safe, and can be disposed of without violating any environmental laws. Unfortunately, it is not a perfect solvent because it does not dissolve most non-polar organic compounds, it is reactive and can cause corrosion, and it is difficult to remove from high aspect ratio holes such as the dimensions used in the present integrated circuit (IC) technology. Therefore, reagents are added to give water specific functionalities.

The compatibility of water with many reagents is limited and sometimes has unwanted side effects. Sequences of different "functionalized" water are required to either remove something that could not be removed using the previous process step or recover from side effects caused by the previous step. And sometimes, different reagents cannot be mixed because they react. It is for this reason that rinsing with pure water is required between process steps.

Before discussing the specifics of reagents and cleaning steps, an overview of an ideal sequence is presented. Figure 2.1 depicts a schematic representation of a randomly-contaminated Si surface. The surface contains metal ions, particles, and organic films that can also mask the other contaminants. The organic

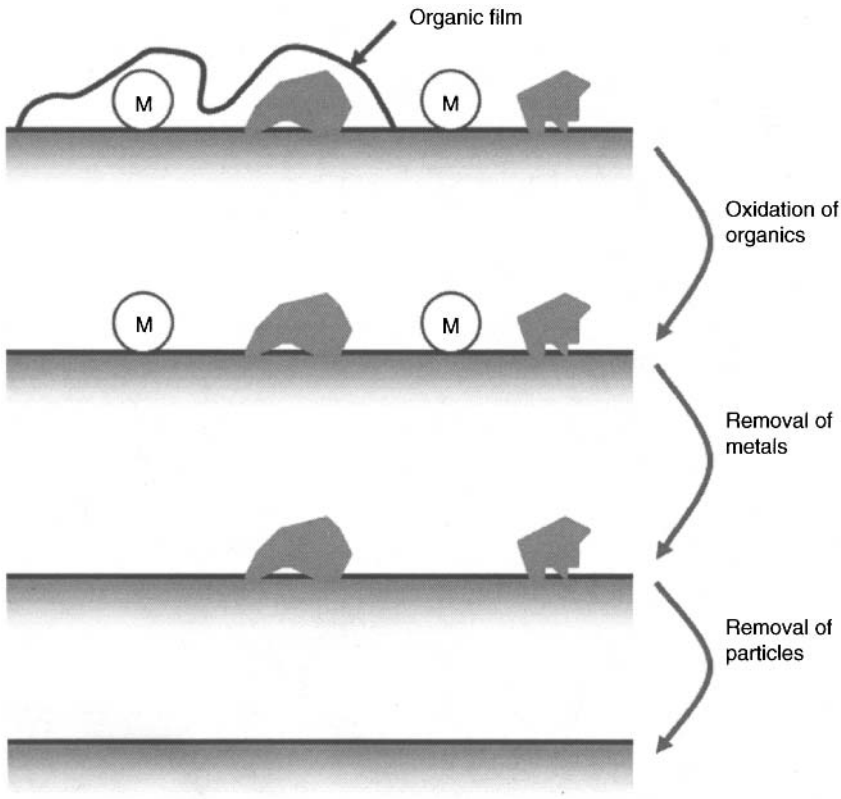



**Figure 2.1.** A surface (top) with all possible contaminants: an organic film, metal ions (M), and particles. In the lower pictures the subsequent removal of organics, metals, and particles are shown resulting in a clean surface. Used with permission of the author.

contamination has to be removed first because it can inhibit the removal of metal ions and particles that are covered by this film. Additionally, particles, those which are organic in nature, are removed in this step. The second step is the removal of metal ions because, in some cases, they can affect the homogeneity of the surface etching process required to remove the particle. Therefore, the particle removal step is the final step of an ideal cleaning process.

## 2.2 Overview of Aqueous Cleaning Processes

### 2.2.1 RCA Cleaning

Kern, while working for RCA, developed a method to clean Si wafers and first published the process in 1970 [1]. This cleaning sequence was, and still is, accepted worldwide as the standard clean for silicon wafers. The RCA cleaning method contains two steps: SC-1 (standard clean) and SC-2. These steps involve a wet-chemical oxidation of the surface by $H_2O_2$ in an alkaline and acidic environment, respectively. RCA cleaned wafers are always hydrophilic and contain a layer of chemical oxide. A chemical oxide is a silicon oxide formed by the oxidation of silicon *via* a wet-chemical reaction. Both standard cleans are discussed extensively in Sections 2.3 and 2.4.

The original RCA sequence does not start with a clean that specifically removes organic contamination; however, it does remove some organics but only those with particle behavior. It also does not specifically include an HF step to remove native or chemical oxide.

### 2.2.2 Modified RCA Processes

There are several RCA-based cleans that have been developed by adding a step or by modifying the original RCA process steps: for example, the HF-last RCA clean for creating a hydrophobic surface [2], the insertion of a preceding clean using sulfuric acid hydrogen peroxide mixture (SPM) at 90–130°C, followed by diluted HF (DHF), and finally with SC-1 and SC-2. There are many other combinations of processes that can be used. Between each of the chemical steps, a deionized water (DIW) rinse is required to remove the reagents from the wafer.

Tool suppliers that provided cleaning other than batch immersion have developed processes for spin-spay and single wafers tools because multiple chemical steps also can be accomplished using a spray processor [2].

### 2.2.3 Other Cleaning Processes

At the beginning of the 1990's IMEC (Interuniversity Micro-Electronic Center) in Leuven, Belgium, introduced a new cleaning philosophy [3] to address some of the weaknesses associated with the SC-1 step of the RCA process. IMEC determined that the cleaning power of SC-1 is due to the combined action of surface oxidation and dissolution of the oxide. In order to control metallic contaminants and also have good particle removal, IMEC suggested using a cleaning sequence in which

the oxidation and etching steps are separated. The process outline is presented in detail in [4].

The Diluted Dynamic Clean (DDC) is a process developed by LETI and is specific to the pre-gate clean [5]. It is similar to the IMEC clean; however, the cleaning initiates with the removal of the sacrificial oxide layer. Very similar to DDC is the New Wet Cleaning (NWC) introduced by Ohmi [6]. In the NWC, the procedure initiates with an IMEC-like clean, but $H_2O_2$, surfactants, and megasonics are added to the first HF step to aid particle removal. The subsequent HF and $O_3$ cycles remove the chemicals and surfactants from the previous step. Instead of a final DIW/$O_3$ rinse, the final step is an ultra pure water (UPW) step with dissolved $H_2$ gas. These processes are also outlined in detail in [4]. Other processes have been proposed including single-step processes [7], nevertheless, the RCA process and variations continue to thrive in the IC industry.

## 2.3 The SC-1 Clean or APM

For silicon-wafer cleaning technology, ammonia hydrogen peroxide mixture (APM) is known as standard clean 1 (SC-1) and is part of the RCA process. The chemical mixture is also known as AM1, Vc1, RCA-1, Super Clean 1, or Huang-1. It was developed to remove particles and organic contamination from Si surfaces [1]. The concentration of the components is given in volume mixture ratio of ammonium hydroxide (25.5–29 wt% $NH_3$ to $H_2O$; 15.2 mol/L and equals ~59.5% as $NH_4OH$), hydrogen peroxide (30–40 wt% $H_2O_2$, without stabilizers), and water, respectively. Initially, the volume ratio of 1:1:5 $NH_4OH$:$H_2O_2$:$H_2O$ was found to be the optimum for the removal of organics. In fact, Kern [1], back in the 1960's, had found this ratio to be an optimum for the removal of bee-wax from Si wafers. The temperature should be as high as possible, but not higher than 80°C. At temperatures higher than 80°C, $H_2O_2$ decomposes too fast, and the $NH_3$ evaporates too rapidly to clean effectively. The cleaning process lasts between 5 and 10 minutes and ends with a quench in cold DIW. In the original process, chemicals are used once and then disposed.

This process has evolved since its initial discovery. The bath lifetime has been extended, and the concentration of the reagents ($NH_3$ evaporates and $H_2O_2$ decomposes) is kept constant with ingenious spiking systems. However, questions arose whether the initial chemical ratios are optimum and if dilution is possible. Cost is the major driving force to reduce the amount of chemicals used. The IC industry requires process chemicals of higher purity with every new process generation, as discussed in Chapter 4. Consequently, the cost of chemicals increases. The second driver for the dilution of process chemicals is improved performance. Chemicals are a source of contamination that ends up on the wafer surface and by adding more water to the chemicals – contaminants will be more diluted. However, dilution cannot continue indefinitely; there is physical and chemical limitations to the level of dilution that is possible.

The composition of SC-1 includes hydrogen peroxide for its oxidizing power, so that it can oxidize organic materials and form water-soluble compounds (however, note that this was an incorrect assumption: the pH is too high for $H_2O_2$ to react with C-H bonds). In the 1970's, it was already in use for cleaning electron

tube components and readily available in high purity [4]. Moreover, hydrogen peroxide and its reaction products (oxygen and water) are volatile and leave no residues on the surface after evaporation. An alkaline pH was required for the cleaning action of the SC-1 solution, and thus ammonia was a logical choice as a metal-free base. Ammonia was also selected for its volatility.

Chemically, APM is one of the most interesting cleaning solutions in semiconductor cleaning. It is one of the candidates to be used for the so-called "single chemistry clean" [7] – a cleaning cycle consisting of only one chemical step followed by a rinsing step. The principle idea of the APM formulation is: hydrogen peroxide oxidizes silicon to form silicon dioxide that is subsequently dissolved in the alkaline environment (pH = ~11) created by the ammonia. Figure 2.2 depicts the mechanism. Etching of the silicon surfaces aids the release of particles by undercutting and potentially removes sub-surface metal-ion contamination that is incorporated in the oxide layer. Although contamination is removed, a caveat remains that the etching can lead to surface roughening [3]. To improve the particle removal efficiency, megasonic energy can be added to the solution [8–10]. An extra benefit of the alkaline condition in the SC-1 step is to remove particles by changing the surface potential of the silicon surface and by making the particle surface negative, depicted in Figure 2.2. Coulomb repulsion forces the particles into solution, and they remain there due to electrostatic stabilization, the double layer repulsion [11]. This is discussed in detail in reference [12].

Although the chemistry of APM appears simple, many potential pitfalls can prevent optimized cleaning. The most important are surface roughening and metal ion contamination because many metal ions are insoluble in the alkaline environment and strongly adsorb on the chemical oxide surface. To understand the roughening mechanisms, the etching mechanism of APM is explained in more detail in Section 2.3.6.

## 2.3.1 Electrochemistry of SC-1

Manufacturing of an IC device requires cleaning of various layers, thus the surface condition and composition of the silicon surface can vary considerably depending

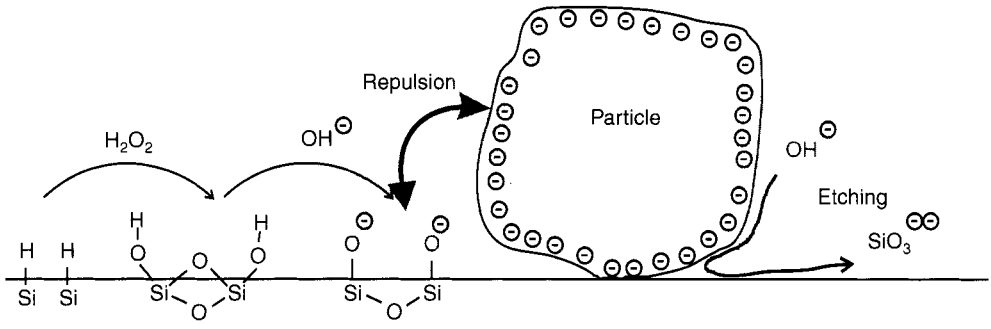



**Figure 2.2.** Schematic of the SC-1 cleaning mechanism. Silicon is oxidized by the hydrogen peroxide; accomplished by deprotonation of the silanol group, surface charging of particles, and undercutting particles by etching the silicon dioxide. Used with permission of the author.

on the manufacturing step. One of the key cleaning steps occurs prior to gate dielectric formation. The critical cleaning step is performed on a bare Si surfaces or on surfaces with a thin native oxide layer. In order to etch Si, it has to be oxidized, thus the etching mechanism can be described electrochemically by two half reactions. Equations 2.1 to 2.4 define the possible anodic and the cathodic half reactions from which the minimal potential required for the reaction can be calculated as a function of reactants and pH. If a potential exceeds this value, the reaction rate and thus the current density will increase. This is schematically represented in an I-E curve depicted in Figure 2.3. In this figure, the current density of the cathodic and anodic reactions are plotted as function of the potential. For corrosion/electrochemically etching, the anodic and the cathodic current must be equal which means that the length of the arrow above the x-axis (the anonic current) is equal to the one below the x-axis (the cathodic current). This picture illustrates that the etching rate of silicon is limited by one of the two half reactions.

$$SiO_2 + 2\,H_2O + 4\,e^- \rightarrow 4\,OH^- + Si \qquad E_0 = 0.857\ V \tag{2.1}$$
$$E = 1.809 - 0.068 \times pH$$

$$SiO_3^{2-} + 3\,H_2O + 4\,e^- \rightarrow 6\,OH^- + Si \qquad E_0 = -1.697\ V \tag{2.2}$$
$$E = -0.017 + 0.017 \times \log [SiO_3^{2-}] - 0.12 \times pH$$

$$H_2O_2 + 2\,e^- \rightarrow 2\,OH^- \qquad E_0 = 1.776\ V \tag{2.3}$$
$$E = 2.728 + 0.032 \log [H_2O_2] - 0.068 \times pH$$

$$2\,H_2O + 2\,e^- \rightarrow 2\,OH^- + H_2\uparrow \qquad E_0 = -0.8277\ V \tag{2.4}$$
$$E = 0.1243 - 0.068 \times pH$$

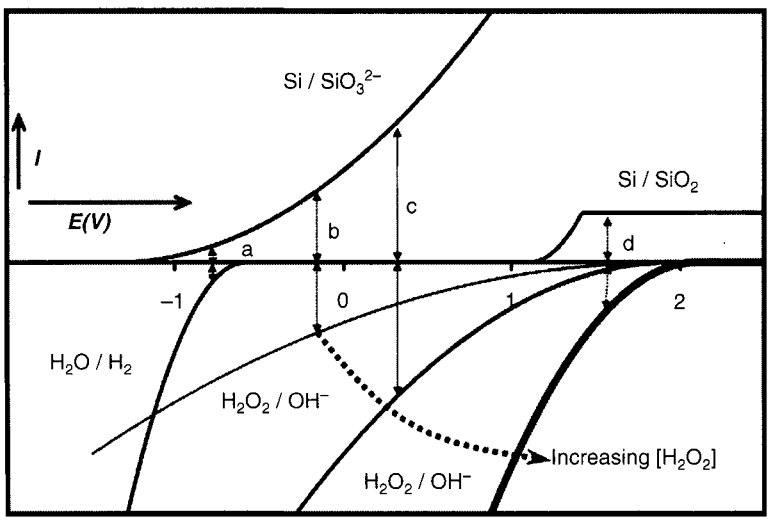



**Figure 2.3.** Model of the I-E (current-potential) curve for the etching of silicon with ammonia (pH = 10.5) and hydrogen peroxide. The relative position on the y-axis is not on scale. The vertical arrows indicate positions of possible equilibrium potentials. Used with permission of the author.

This model helps to explain the effects of variation in reactants in APM. Depending on the concentration of the reactants, $H_2O_2$ ($OH^-$) and $NH_3$, different redox half-reactions occur. At a high $OH^-$ concentration with no hydrogen peroxide, the anodic reaction proceeds as shown in Equation 2.3 and the cathodic reaction as in Equation 2.4. This will result in the net reaction given in Equation 2.5.

$$Si + H_2O + 2\ OH^- \rightarrow SiO_3^{2-} + 2\ H_2(g) \qquad (2.5)$$

Silicon will dissolve as the m-silicylic acid di-anion ($SiO_3^{2-}$) without the formation of the intermediate $SiO_2$ and with the formation of hydrogen gas as a byproduct. Alkaline solutions such as KOH are well known etchants of silicon, and they have a high selectivity towards silicon dioxide. Water (or $H^+$) is the oxidant in this reaction. In Figure 2.3, the equilibrium potential of this combination is set somewhere between the −1.3 and −0.6 Volt indicated by the arrow *a*.

If the oxidation potential of the solution is increased by adding hydrogen peroxide and the $OH^-$ concentration remains high, the cathodic reaction (the oxidation reaction) will be taken over by the hydrogen peroxide, Equation 2.3 and the anodic reaction remains as given in Equation 2.2, the net reaction result is:

$$Si + 2\ H_2O_2 + 2\ OH^- \rightarrow SiO_3^{2-} + 3\ H_2O \qquad (2.6)$$

Due to the addition of $H_2O_2$, the equilibrium potential will shift more negative (Figure 2.3 arrows *b* and *c*), the anodic current will increase, and the Si etching rate increases. This is exactly what Van den Meerakker and Van der Straaten observed [13]. In their experiments, they determined the etching rate of 1.9 M $NH_3$ solution as a function of the amount of $H_2O_2$, as shown in Figure 2.4. The etching rate of Si

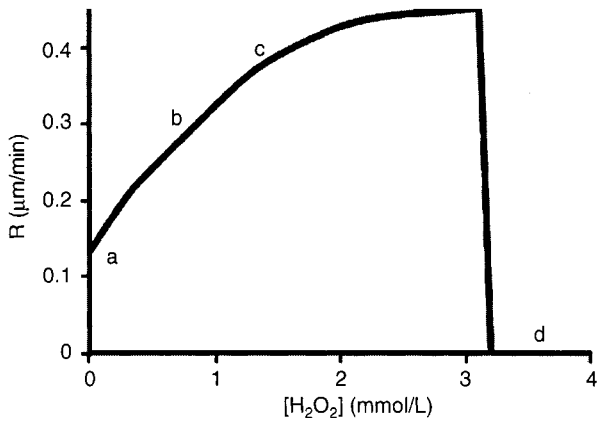



**Figure 2.4.** Etching rate (R) of Si in 1.9 M $NH_3$ (70°C) as a function of $H_2O_2$ concentration. Below 3 mM $H_2O_2$ dissolution of Si occurs and above 3 mM $H_2O_2$ dissolution of $SiO_2$ occurs, which is a slower process step. Letter marks indicate points from the I-E curve in Figure 2.3. Figure is adapted from [13]. Reproduced with permission of ECS – The Electrochemical Society from Meerakker, J. v. d. and Straaten, M. H. M. v. d., Journal of the Electrochemical Society.

in APM without $H_2O_2$ is 0.13 μm/min at 70°C and is limited by the oxidation reaction of silicon. If $H_2O_2$ (< $3 \times 10^3$ M) is added, the etching of the Si is enhanced indicating that the oxidation of the Si is still the rate limiting process step. The etching rate can be as high as 0.44 μm/min at 70°C with $3 \times 10^{-3}$ M $H_2O_2$.

A further increase of the hydrogen peroxide concentration or a reduction of the $OH^-$ concentration will result in a change of the anodic reaction compared to the one given in Equation 2.1. The cathodic reaction remains as in Equation 2.3 resulting in the net equation:

$$Si + 2\,H_2O_2 \rightarrow SiO_2 + 2\,H_2O \tag{2.7}$$

Addition of more $H_2O_2$ makes the equilibrium potential shift even more negatively (Figure 2.3 arrow *d*) where the cationic current is equal to the anionic curve of the $SiO_2$ formation curve. The current at that position is much lower than in the previous example. At this point, the dissolution of Si ceases due to the formation of poorly soluble $SiO_2$, thus the oxidation reaction is faster than the dissolution reaction. This anodic passivation occurs in 1.9 M $NH_3$ (70°C) solution at concentrations above the $3 \times 10^{-3}$ M $H_2O_2$ (Figure 2.4). The etching rate will decrease to almost zero (orders of 0.5–30 Å/min depending on type of substrate) [14–18]. In fact the etching rate is equal to that of $SiO_2$ in the absence of $H_2O_2$ at the same pH. Further increases of $H_2O_2$ do not change the etching rate of Si although the $SiO_2$ etching rate slightly decreases as a result of a decrease in pH.

## 2.3.2 Molecular Mechanism

The behavior of APM on Si and $SiO_2$ can also be understood on a molecular level. For Si to etch, like other metals and semimetals, it must be oxidized before it can be dissolved in water, as discussed in Chapter 3. Since there is etching rate selectivity between Si and $SiO_2$ the conclusion can be drawn that the oxidation reaction step is rate limited and slower than the etching step.

Figure 2.5 depicts the key reaction for the etching of Si and $SiO_2$ in a low oxidation environment. In both cases, a surface Si-OH group has to be removed by

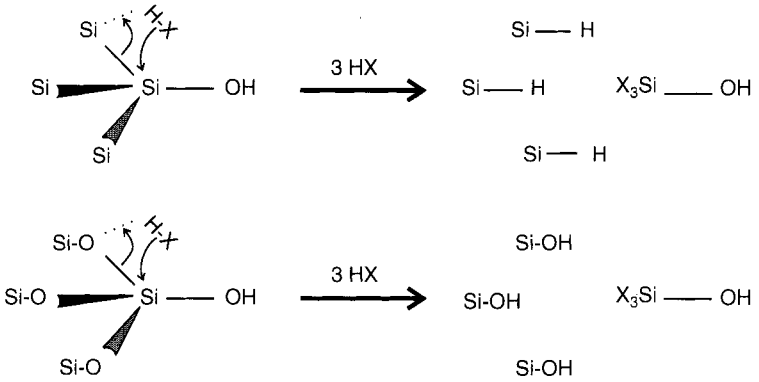



**Figure 2.5.** Similarity between etching of the ≡Si-OH unit out of a Si or $SiO_2$ matrix, where X = OH or F. Used with permission of the author.

three nucleophilic substitution reactions: for the removal of a Si-OH group from a Si matrix, three Si-Si bonds must be broken; and for the removal of Si-OH from a $SiO_2$ matrix, three Si-O bonds must be broken. The bond strengths differ – Si-Si is 327 kJ/mol while the Si-O bond is 810 kJ/mol [19–21]. The three new bonds are formed and have bond strengths of <299 kJ/mol for Si-H bonds and 428 kJ/mol for O-H bonds. The net energy balance is strongly in favor of etching Si-OH from the Si matrix, and this is independent of the etching agent (H-F or H-OH) as long as the etching rate is determined by the oxidation reaction and the newly formed Si-H bonds are reoxidized.

The reaction takes place at the surface layer of the Si proceeding by first removing the top Si atoms that are terminated with OH groups. Silicon-oxygen bonds are strongly polarized – the Si atom is positively charged and can be attacked by a nucleophile such as a hydroxyl anion. Like any nucleophilic substitution reaction, another chemical bond on the Si atom is broken when the nucleophile approaches. This is the so-called leaving group. The relative ease of this bond breaking depends on the bond strength.

Figure 2.6 shows the mechanism for forming a $SiO_2$ passivation layer, a chemical oxide in $NH_4OH$. The transition from Si etching to passivation in an ammonia solution can be understood by observing that when the hydrogen peroxide concentration is increased, even with no hydrogen peroxide present, the Si will etch faster than $SiO_2$. The Si etching rate can be further increased by adding small amounts of $H_2O_2$ because the Si-H groups on the surface will be oxidized easier. This is the regime on the electropotential diagram (Figure 2.3, points *a-c*) where Si-OH groups are removed from a Si-matrix. If the oxidation potential exceeds a certain level (>3 mmol of $H_2O_2$/L), the oxidation rate is faster than the etching rate and oxidation occurs. Above this threshold, not only is the first monolayer of silicon oxidized, but also the second layer and subsequent deeper layers. Silicon surfaces that are oxidized more than two monolayers deep behave like silicon dioxide because the SiOH unit is removed from the $SiO_2$ matrix. The etching rate of the "silicon"

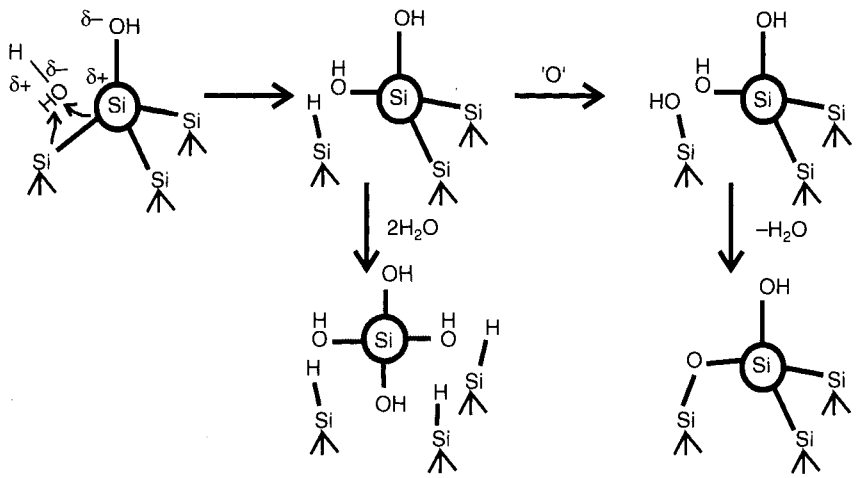



**Figure 2.6.** Etching of a monolayer of Si-OH by water and, alternatively, formation of a silicon dioxide layer. Used with permission from the author.

will become similar to that of "$SiO_2$". This is called "passivation" of silicon surface [22]. It occurs when the oxidation is fast and the dissolution of silicon dioxide is a slow process (Figure 2.3, point *d*). Chemical oxidation is a self-limiting process and when the oxide layer reaches a certain thickness it does not grow further. If no silicon dioxide is removed (at low temperatures), then the silicon-etch process will not happen. For this reason, if APM is used to re-grow a chemical oxide layer after an HF step, it preferably is done at low temperatures.

### 2.3.3 Etching Rate in APM

In most applications, the $H_2O_2$ concentration is high enough for Si to be passivated, where the etching rate of Si is approximately the same as that of $SiO_2$. Based on the reaction mechanism described in the previous paragraph, the reaction rate depends on the surface concentration of Si-OH groups and on [$OH^-$]. The number of Si-OH groups is considered to be constant (so-called steady-state concentration), and [$OH^-$] is fixed by the pH. The reaction is assumed to be first order of [$OH^-$] as it will be most difficult to break the first of the three backbone O bonds. The etching rate $dSiO_2/dt$ can be expressed as [23, 24]:

$$\frac{d\mathrm{SiO_2}}{dt} = k[\mathrm{OH^-}] = k_0 e^{-E_a/RT}[\mathrm{OH^-}] \tag{2.8}$$

In this equation, the reaction rate constant ($k$) can be further partitioned into a function according to the Arrhenius equation giving an expression where the etching rate is a function of temperature. This etching reaction has an activation energy ($E_a$) of 61 kJ/mol and a pre-exponential factor of $5.21 \times 10^{11}$ (L/mol) (nm/min). The etching rate $dSiO_2/dt$ will be expressed in nm/min. Note that the pre-exponential factor can vary depending on the type of oxide layer (*e.g.* chemical oxide, thermal oxide).

The hydroxyl concentration in APM solution depends on the amount of added ammonia ($c_{NH_4OH}$) and hydrogen peroxide ($c_{H_2O_2}$):

$$[\mathrm{OH^-}] = \sqrt{\frac{K_b K_w}{K_a}\frac{c_{\mathrm{NH_4OH}}}{c_{\mathrm{H_2O_2}}}} \tag{2.9}$$

using reference [25], approximately:

$$K_b = \frac{[\mathrm{NH_4^+}][\mathrm{OH^-}]}{[\mathrm{NH_4OH}]} = 2.41\times10^{-5} e^{-690/RT} \tag{2.10}$$

$$K_a = \frac{[\mathrm{HO_2^-}][\mathrm{H^+}]}{[\mathrm{H_2O_2}]} = 2.80\times10^{-8} e^{-22700/RT} \tag{2.11}$$

$$K_w = \frac{[\mathrm{H^+}][\mathrm{OH^-}]}{[\mathrm{H_2O}]} = 7.63\times10^{-6} e^{-50400/RT} \tag{2.12}$$

Filling Eq. 2.9 into 2.8 and using the given $K$ values, Eq. 2.13 is obtained [17]:

$$\frac{dSiO_2}{dt} = 4.22 \times 10^{10} \times \sqrt{\frac{c_{NH_4OH}}{c_{H_2O_2}}} \times e^{-75200/RT} \text{nm/min} \qquad (2.13)$$

From this equation, it can be concluded that the etching rate of APM solutions is constant for identical $NH_4OH$:$H_2O_2$ ratios. In Figure 2.7, the etching rate of some APM solutions are plotted as a function of temperature at different $NH_3$ ($NH_4OH$):$H_2O_2$ ratios. As expected, the highest etching rates are observed with the highest $NH_4OH$:$H_2O_2$ ratio (in this Figure, 4:1 ratio). As particle removal efficiency depends on the etch depth, a decrease in ammonia concentration with respect to the hydrogen peroxide concentration would result in reduced particle removal efficiency. Strangely, the trend in the industry is to reduce the ammonia concentration more than the hydrogen peroxide concentration when using diluted APM. The reason for this practice is that engineers fear that the hydrogen peroxide concentration can become too low (*e.g.* by decomposition) leading to surface roughening.

### 2.3.4 Concentration Variations

The concentrations of both the ammonia and hydrogen peroxide are critical process parameters as they impact the particle removal efficiency, the surface roughness, and the removal rate of silicon and $SiO_2$. These concentrations are subject to variations and are more critical for processes where the chemicals are reused.

Ammonia, which is a gas at room temperature (boiling point = –33°C), will easily evaporate out of the APM solution at temperatures between 50–70°C. The evaporation rate will depend on temperature, bath agitation, and exhaust. The evaporation of $NH_3$ out of an APM solution is 1st order, and the activation energy of this process is determined to be 43 kJ/mol [26].

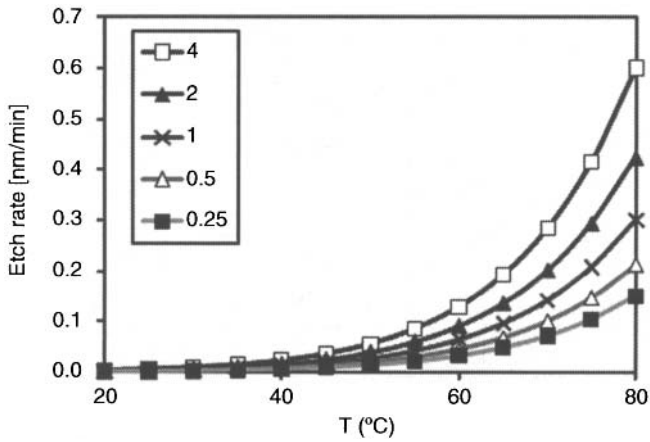



**Figure 2.7.** The $SiO_2$-etching rate of APM as function of temperature and $NH_4OH$:$H_2O_2$ ratio. Used with permission of the author.

$$NH_3(aq) \rightarrow NH_3(g) \tag{2.14a}$$

$$NH_4OH \rightarrow NH_3(g) + H_2O \tag{2.14b}$$

With the use of the Arrhenius equation, the relation between the evaporation rate and temperature is determined:

$$k = Ae^{-E_a/RT} \tag{2.15}$$

The pre-exponential factor, $A$, is an unknown parameter that is process and hardware specific and also depends on:

1. The efficiency that the $NH_3$ fumes are removed from the bath surface (*i.e.* air flow). If the exhaust is increased, $A$ will increase. This is important if maintenance has been performed on the exhaust or hood.
2. The surface area from which the $NH_3$ can evaporate, such as agitation of the liquid surface by gas bubbles of $H_2O_2$ decomposition or overflow recirculation, both of which will enhance $NH_3$ evaporation. Since the decomposition of $H_2O_2$ is temperature dependent, $A$ will slightly increase as a function of temperature when $H_2O_2$ decomposes.

In order to calculate the ammonia concentration in a process vessel at a certain time, the value of $A$ of that tank has to be resolved. This can be done by measuring the decay curve of the ammonia concentration and plot the logarithm of the ammonia concentration versus time (Eq. 2.16). The slope will yield the $-k$, and $A$ can be calculated and is equal to the determined intercept [27]:

$$k \times e^{-43000/8.317T} \tag{2.16}$$

$$\frac{d[NH_3(aq)]}{dt} = -k[NH_3(aq)] \Rightarrow \ln\frac{[NH_3(aq)]_t}{[NH_3(aq)]_0} = -kt \ln\frac{[NH_3(aq)]_t}{[NH_3(aq)]_0} = -kt \tag{2.17}$$

Hydrogen peroxide decomposes in an alkaline solution:

$$2H_2O_2 \xrightarrow{cat} 2H_2O + O_2 \tag{2.18}$$

This decomposition reaction is catalyzed by metals (*i.e.* $Fe^{+3}$, $Cu^{+2}$) or by iodine [28], and is a source of great concern. The decomposition of hydrogen peroxide has been investigated by different researchers [29, 30]. Van den Meerakker found that the decomposition rate is first order in $[H_2O_2]$ with an activation energy of 82 kJ/mol [29]. In his publication, no specification of the amount of metal contamination is given. A few years later, Schmidt [30] showed that the decomposition rate of the $H_2O_2$ is much lower if the metal concentration decreases. From the data obtained from solutions with very low metal concentrations (< 0.2 ppb) and assuming first order reaction kinetics, the activation energy is found to be 120 kJ/mol. This

implies that the metal catalyzed decomposition has a lower activation energy than the more intrinsic self-decomposition of $H_2O_2$.

All of these observations can be explained by one dominant reaction; however, there are more than one decomposition mechanisms with rates in the same range (*i.e.* a metal-ion catalyzed and a self decomposition reaction) [28]. Separating out the catalytic activity of metals in the measured decomposition-rate data, it was found that the un-catalyzed decomposition reaction was 2nd order in $[H_2O_2]$ with an activation energy of 170 kJ/mol. This finding leads to the conclusion that pure $H_2O_2$ in ammonia solution is far more stable than what was concluded on the basis of an APM solution with uncontrolled amounts of metal ion contamination.

In addition to this self decomposition pathway, there are metal catalyzed reactions as shown in Figure 2.8. There are both first order and second order reactions:

1. The first order reaction is starting from a metal ion hydroxide anion, *1*, that produces an ion exchange reaction intermediate *2* that yields *3* and *4*. In the last transition an oxygen molecule is liberated.

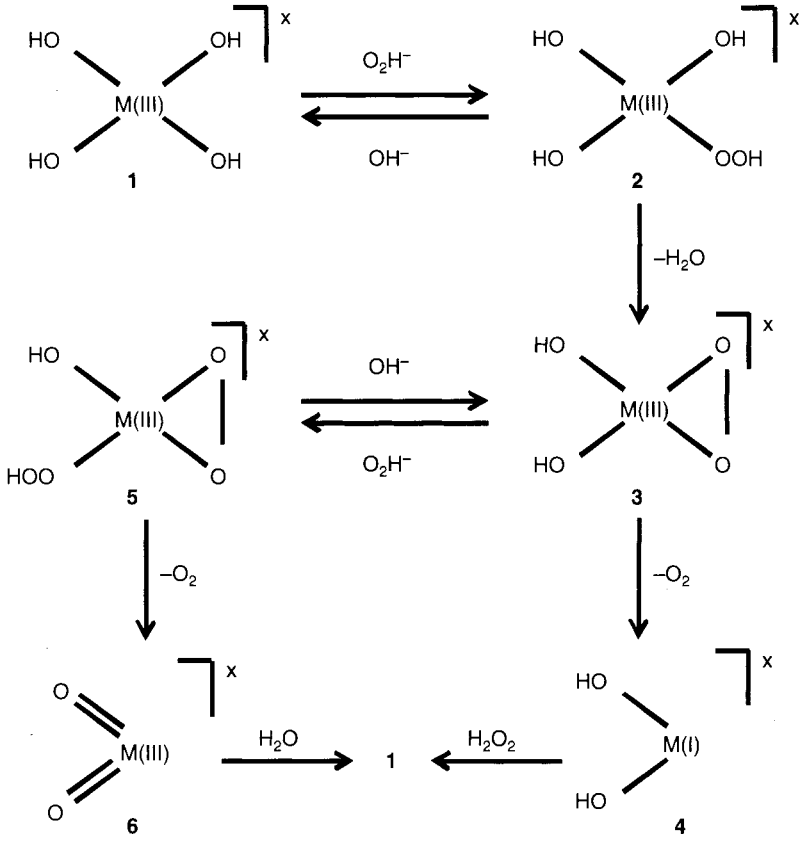



**Figure 2.8.** Proposed reaction mechanism of metal-ion catalyzed $H_2O_2$ decomposition. In this example, the metal ion has an oxidation state III, and the species has a charge of x = –1. $H_2O_2$ is represented by its $O_2H$ anion [28]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S. D., Baeyens, M., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

Intermediate *4* is a reduced metal ion that quickly re-oxidizes to reform *1*. Reactions *1* to *4* are rate limiting and are 1st order with respect to $H_2O_2$ and the metal-ion concentration. The activation energy of the rate determining step in this reaction sequence depends on the metal ion: 84 and 65 kJ/mol for Cu and Fe, respectively.

2. The second order reaction follows the same route up to intermediate *3*. A second ion exchange reaction with a hydroperoxyl anion ($HOO^-$) results into *5* that subsequently decomposes into *6* and $O_2$. The critical path now contains two $H_2O_2$ derived molecules and one metal ion. Therefore, this reaction is 2nd order with respect to $H_2O_2$. This reaction path is observed for Fe (activation energy of 71 kJ/mol) but not for Cu. Intermediate *6* is hydrolyzed back to *1*.

As an example, the rate of decomposition is illustrated by the half-life time measurements of hydrogen peroxide by Schmidt for APM solution with different concentration of metals (in his case iron ions) [30]. From these data, the reaction rate constant $k$ can be estimated and, in Figure 2.9, the natural logarithm of $k$ is plotted as a function of the metal concentration. The catalytic species is likely to be an aggregate of iron ions with one or more anions (*e.g.* $O_2^-$, $OH^-$, $NH_2^-$, $HOO^-$) [31]. Once the aggregate has a critical size, it can act as a catalytic species and behaves as a single particle.

In a fresh APM solution with a concentration of 1.4 M of hydrogen peroxide and 1 ppb of Fe ions ($10^{16}$ ions/L) at 70°C, half of the amount of $H_2O_2$ ($4.2 \times 10^{23}$ molecules/L) is decomposed within 1.7 hours. Each second, $6.8 \times 10^{19}$ molecules/L are decomposed by $10^{16}$ Fe ions or 6800 molecules $H_2O_2$ per second per Fe ion. If the catalytic active species contains at least 5 Fe ions and all Fe ions are in such a cluster, then the minimal turnover number of one catalytic species is 34000 $s^{-1}$. Furthermore, because of the fast decomposition of the $H_2O_2$, the concentration of

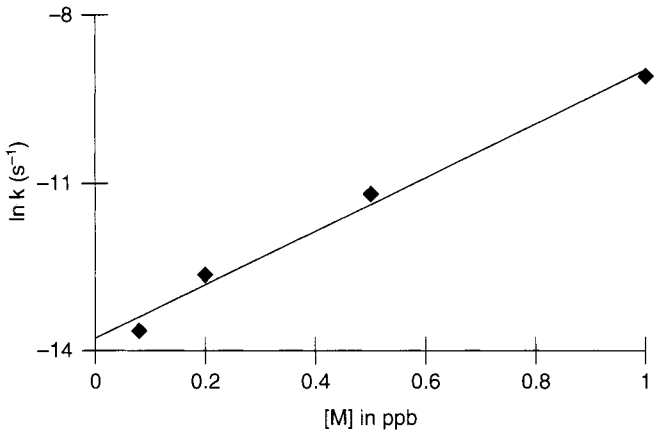



**Figure 2.9.** The ratio rate constant ($k$) of the catalytic decomposition of peroxide in APM as a function of iron concentration [28]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S. D., Baeyens, M., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

the $H_2O_2$ around the catalytic metal species will be low, and the formation of oxygen will be high. The first effect will lead to silicon surface roughening, and the latter will result in the formation of gas-bubbles at the liquid/gas interface of the catalytic metal species.

### 2.3.5 Concentration Monitoring and Control

Concentration monitoring and the subsequent spiking of chemicals is a method to extend bath lifetime. In an APM solution, both the hydrogen peroxide and the ammonia concentrations are monitored and controlled for optimum process performance. One type of monitoring can be performed by measuring parameters of the solution. Rosamilia proposed to measure the pH and conductivity, σ [32].

1. pH → $[OH^-]$: The measurement of the pH will yield the $[OH^-]$ concentration that depends (according Eq. 2.9) linearly with the square root of $[NH_3]$:$[H_2O_2]$.
2. σ $[OH_2^-]$: The conductivity is determined by all ions in the solutions, which are $H^+$, $NH_4^+$, $OH^-$, and $OH_2^-$.

For the conductivity some assumptions are made:

1. Compared to $NH_4^+$, the $H^+$ concentration is negligible.
2. In a standard APM bath, the $OH^-$ concentration can also be neglected with respect to $OH_2^-$.

There are some boundary conditions for the latter assumption. In Equation 2.19 the ratio between these two anions is given as a function of temperature and hydrogen peroxide concentration. In the standard APM the $[H_2O_2]$ is 1.4 mol/L, which means that the $[OH_2^-]/[OH^-]$ ratio at 50°C is 155 and at 70°C it is 85. In both instances the assumption that $[OH_2^-] >> [OH^-]$ is true. When APM is too diluted, this assumption may become false.

$$\frac{[HO_2^-]}{[OH^-]} = \frac{K_a[H_2O_2]}{K_w} = 3.6\times10^{-3}\times e^{\frac{3340}{T}}[H_2O_2] \qquad (2.19)$$

With these assumptions and the law of electroneutrality, $[NH_4^+]$ is equal to $[OH_2^-]$. This means that $[NH_4^+]$ in Eq. 2.10 can be replaced by $[OH_2^-]$ and by combining Eq. 2.10 with 2.11, Eq. 2.20 can be deduced [21]. By measuring the conductivity, the $OH_2^-$ concentration is obtained which in turn linearly relates with the square root of the product of the ammonia and hydrogen peroxide concentration:

$$[OH_2^-] = \sqrt{\frac{K_a K_b}{K_w} c_{NH_3} c_{H_2O_2}} \qquad (2.20)$$

Both the hydrogen peroxide (Eq. 2.21) and ammonia (Eq. 2.22) concentrations can be calculated from the pH and σ. In order to do this, the *K* values have

to be determined, and it should be noted that these values are temperature dependant (~exp ($-E_a/RT$)). In practice, the $K$ value is fixed at the moment the bath is filled and known concentrations of ammonia and hydrogen peroxide are present. Corrective actions are:

1. Addition of $H_2O_2$ when the quotient $f(\sigma)/f(pH)$ decreases.
2. Addition of $NH_3$ when the product $f(\sigma)\times f(pH)$ decreases.

$$c_{H_2O_2} = k_{H_2O_2}\frac{f(\sigma)}{f(\mathrm{pH})} \approx \frac{[OH_2^-]}{[OH^-]} \tag{2.21}$$

$$c_{NH_3} = k_{NH_3} \times f(\mathrm{pH}) \times f(\sigma) \approx [OH^-][OH_2^-] \tag{2.22}$$

If the concentration development of one of the bath constituents can be predicted, only one bath property has to be monitored. The predictable component can be added on a time-spike basis, the other one monitored by pH or σ. From the previous paragraph, it is known that a drop in hydrogen peroxide concentration is difficult to anticipate because it depends on unpredictable parameters such as the metal-ion impurity concentration. Forecasting the ammonia concentration is doable when the evaporation process is understood.

Knowing the tank specific $A$ (see Eq. 2.15), the $k$ can be calculated at any temperature. Moreover, Winters used this information to determine the spiking frequency and the amount needed to successfully maintain a constant ammonia concentration [27]. The variation of the ammonia concentration increases with the spike amount per time interval, $\beta$, ($mol^{-1}s^{-1}$) and decreases with the amount that evaporates:

$$\frac{d[NH_4OH(aq)]}{dt} = \beta - k[NH_4OH(aq)] \tag{2.23}$$

This differential equation can be rewritten and directly solved:

$$\frac{d[NH_4OH(aq)]}{k[NH_4OH(aq)]-\beta} = -dt \Rightarrow \frac{1}{k}\ln\left(k[NH_4OH(aq)]-\beta\right) = -t + C \tag{2.24}$$

With the boundary condition that at $t = 0$ the ammonia concentration is equal to the initial concentration $[NH_4OH(aq)]_0$, then $C = ln(k[NH_4OH(aq)]_0 - \beta)$. Rearranging the above equation results in:

$$[NH_4OH(aq)]_t = \frac{\beta}{k} + \left([NH_4OH(aq)]_0 - \frac{\beta}{k}\right)e^{-kt} \tag{2.25}$$

With this formula, the ammonia concentration can be calculated in an APM bath having an ammonia spiking system. Moreover, the spike amount per time interval can be calculated to keep the ammonia concentration stable with time. The

requirements are that at $t = \infty$ the ammonia concentration $[NH_3(aq)]_t$ is equal to $[NH_3(aq)]_0$. If this is inserted in into Eq. 2.25, the expected relation is found where $\beta$ is equal to the evaporation rate:

$$\beta = k\left[\mathrm{NH_4OH}(aq)\right]_0 = Ae^{-43000/8.314T}\left[\mathrm{NH_4OH}(aq)\right]_0 \tag{2.26}$$

Experiments showed that using this method the ammonia concentration can be kept constant for hours.

### 2.3.6 APM-related Surface Roughening

The disadvantage of a cleaning solution that has combined etching and oxidation properties is that the surface can be detrimentally etched in an uncontrolled bath. Etching of silicon in an APM solution is a problem when hydrogen peroxide is below a certain threshold (Figure 2.4). In alkaline solutions, silicon is known to etch differently along the different crystal planes. The etching rate of Si <111> is higher than that of the Si <100> and, consequently, etching a Si <100> surface, pits will be formed with <111> facets. If no or not enough hydrogen peroxide is present, dissolution of silicon proceeds according this mechanism, and the silicon surface will roughen [29]. Contrarily, with high hydrogen peroxide concentrations (> 3 mmol/L), the oxidation with $H_2O_2$ will dominate and yield an isotropic process. The etching, which still occurs, will become isotropic and the surface will not roughen [29]. This means that the standard 1:1:5 APM ($[H_2O_2]$ = 1.4 mol/L) does not etch the silicon significantly. From an electrochemical point of view, $H_2O_2$ can be diluted to 2500:1, without roughening silicon surfaces.

Historically, for optimizing the mixing ratio of cleaning solutions, light scatter techniques are used to count particles. These techniques do not discriminate between pits (increased surface roughness), or particles; they are all called light point defects (LPD). It is likely that the initial mixing ratios of APM were optimized for both particle removal and minimum surface roughening. There are several ways that APM solutions can increase surface roughness, and these mechanisms result in surface roughening and will be explained in more detail [34]:

1. Vapor etching.
2. Galvanic etching and masking.
3. Catalyzed $H_2O_2$ depletion.

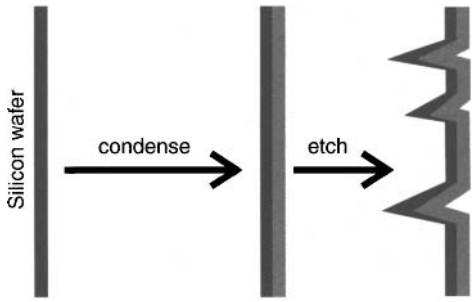
Not discussed are mechanisms of LPD creation by gas-bubbles (formed by the decomposition of $H_2O_2$). A silicon surface can roughen when gas-bubbles run continuously over the same surface area while the wafer is in the APM solution. This can also be explained by the presence of particles in the solution that are deposited by the gas bubbles that run over a surface [35].

#### *2.3.6.1 Vapor Etching*

Vapor etching occurs when APM solution is used at temperatures much higher than the boiling temperature of ammonia. The vapor arising from this APM solution

contains a high concentration of $NH_3$ gas requiring an exhaust that is adequate to remove the vapor released. Furthermore, water is vaporized at higher temperatures. Hydrogen peroxide has the highest boiling temperature of the three APM-components (150.2°C), but its relative vapor pressure is much lower than its relative concentration in the liquid. Additionally, hydrogen peroxide decomposes in an ammonia solution at high temperatures to form oxygen gas (Eq. 2.18). These gas-bubbles agitate the solution contributing additional $NH_3$ and $H_2O$ vapor.

Above an APM bath, there is hot water vapor containing a high concentration of ammonia. Bringing cold wafers into this environment, even for a short exposure, will result in condensation of a water film. These water films are saturated with ammonia and lack hydrogen peroxide, as the latter is present in low concentrations, schematically depicted in Figure 2.10. An alkaline solution without a strong oxidizing agent can result in crystal-specific etching of silicon (Eq. 2.5) and, consequently, lead to surface roughening. Wafers that lack an (chemical/native) oxide layer will be the most sensitive to this roughening mechanism because the silicon etching can immediately initiate. Immersing wafers without an oxide layer into an APM bath is not rare in semiconductor cleaning as some cleaning sequences contain



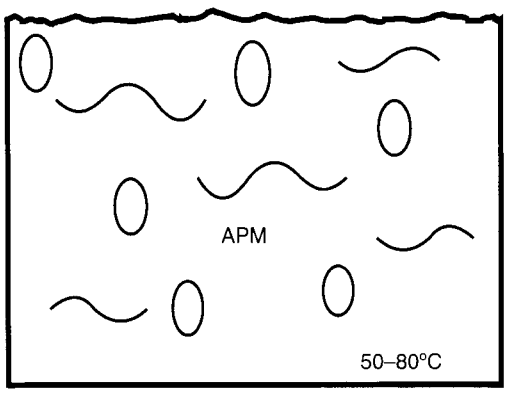




**Figure 2.10.** Surface roughening mechanism caused by condensation of ammonia. Used with permission of the author.

an HF clean prior to APM leaving a hydrogen-terminated Si surface. An image of a hydrophobic wafer exposed to APM vapor can be seen in Figure 2.11. The water that condenses on the wafer does not uniformly wet the surface and can form small droplets [36]. These droplets etch the surface and leave patterns such as those shown in Figure 2.11 on the wafer surface.

### 2.3.6.2 *Galvanic Etching and Masking*

Etching and oxidation does not necessarily take place at the same spot on the silicon surface. Electrochemical reactions can occur at separate anodes and cathodes. This means that some parts of the surface are negatively charged and act as cathodes where the oxidant, in this case $H_2O_2$ in APM, is reduced by taking electrons from silicon, as depicted in Figure 2.12. Other parts are positively charged and act as anodes where the silicon will dissolve (anodic dissolution) by reacting with OH to form $SiO_3^{2-}$, as depicted in Figure 2.13. On perfectly flat, clean, and defect-free surfaces in a homogeneous APM solution, the anodes and cathodes are indistinguishable, the regions that share anodic and cathodic behavior are too small to matter compared to the bulk silicon surface and, thus, result in homogeneous

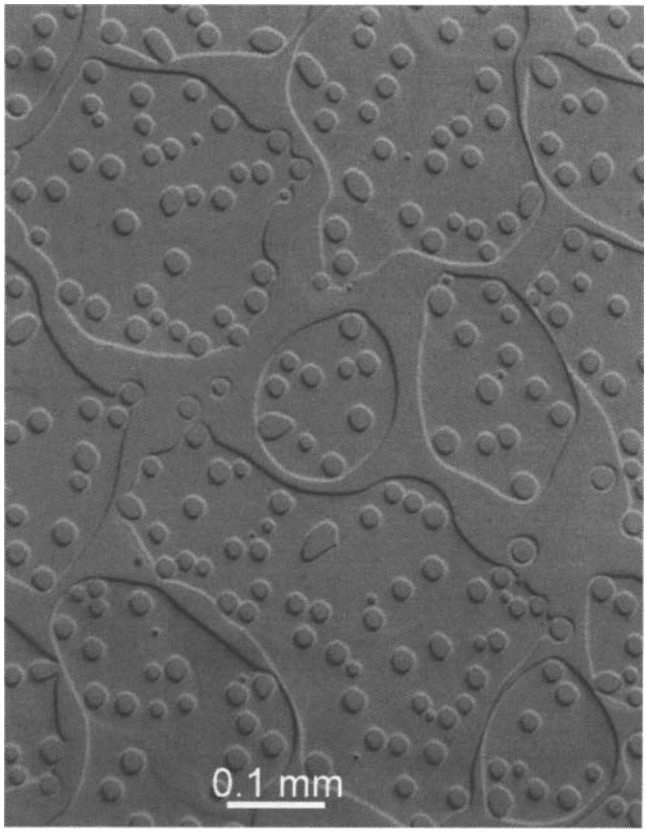



**Figure 2.11.** Micrograph of a hydrophobic silicon surface exposed to APM (70°C) vapor for 15 sec showing pattern etching. Experiment conducted and photo taken by L. Winters, NXP Semiconductors [36]. Used with permission of Léon Winters (NXP).

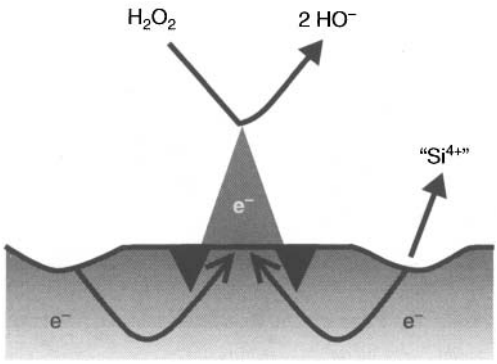



**Figure 2.12.** A local corrosion cell formed by the galvanic coupling of a metal (or also n-doped silicon) to a silicon surface [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society.*

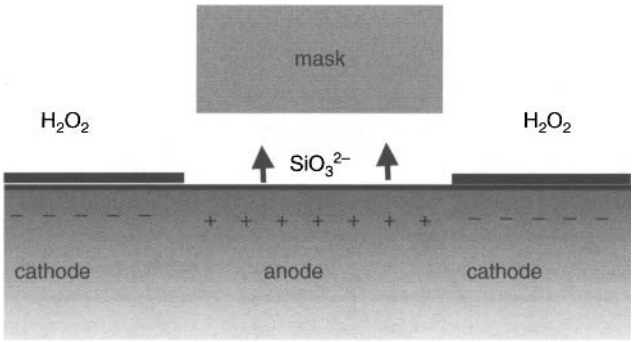



**Figure 2.13.** Crevice corrosion in APM – $H_2O_2$ becomes depleted under the mask and silicon dissolves anodically. The mask can be a particle, bubble, or photoresist residue. Used with permission of the author.

etching. Problems occur when the situation is inhomogeneous resulting in separation of larger cathodic and anodic areas. Consequently, the surface will be unequally etched which in many cases results in surface roughening at the local anode. Examples of phenomena that cause unequal distribution of the anode/cathodes are particles, gas-bubbles, metal-precipitates, pits, and doping profiles.

Galvanic corrosion of silicon explains many of the roughening problems as well as the excellent particle removal capability of an APM solution. For example, treating the etching of silicon as a corrosion process indicates that an inhomogeneous distribution of the oxidant ($H_2O_2$) will distribute the anodes and cathodes non-uniformly over the surface. Areas with low concentration of hydrogen peroxide will become the anode and areas with high concentrations the cathode. Reasons for a heterogeneous distribution of oxidant are usually diffusion limitations induced by masking (particles) or the existence of pits on the substrate. The first reason is known in literature as crevice corrosion (silicon dissolves under the particle) [37], and the second one is so-called pitting corrosion (silicon dissolves in the pit) [38]. Describing APM chemistry as a corrosion process helps explains why APM is

effective at particle removal. The liquid under the particle is poorly refreshed, and the concentration of $H_2O_2$ is lower under the particle than in the surrounding area and becomes anodic. The silicon under the particle will dissolve faster and thereby lift the particle off the surface if it is small enough. This suggests that the average etch-depth, which is usually measured, is not an important metric for the particle removal efficiency (PRE), it only gives an indication of PRE because the localized etching beneath the particle is the reason it is removed – by lift-off.

Larger particles or other obstructions such as gas-bubbles or photoresist residues can act as masks. These obstructions are more difficult to remove; consequently, the resulting crevice corrosion can become more serious leading to surface damage. Naturally occurring pits are probably not deep enough to limit diffusion of $H_2O_2$ to the bottom of the pit. However, intentionally applied pits, such as trenches, can result in pitting corrosion as the $H_2O_2$ concentration in the bottom of the pit will be lower with respect to the surface.

Metal deposits on silicon wafers can induce local silicon roughening. This is more acute with metals that are more noble than the silicon in the local environment. If such a metal deposit is galvanically coupled with the silicon substrate, then a galvanic cell is formed and produces a local corrosion cell. The more noble metal acts as the cathode while the surrounding silicon will anodically corrode. Figure 2.14 shows an atomic force microscopy image of copper contaminated silicon after cleaning with APM [34]. Surface roughening can occur due to the dissolution of the silicon around the metal contaminant resulting in a surface asperity with a metallic cap or by crystal

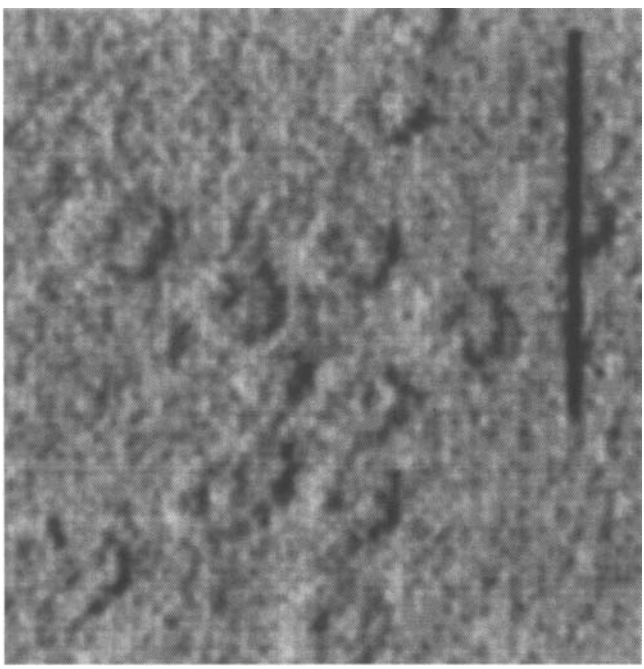


**Figure 2.14.** Atomic force microscopy plot of Cu generated APM haze (black bar has length of 10 μm) [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

specific dissolution of silicon as found in alkaline water [39, 40]. Furthermore, local $H_2O_2$ decomposition will induce local $H_2O_2$ concentration differences resulting in an enhanced effect on the surface roughening of the silicon.

In a HF solution, copper plates out onto bare silicon. Teerlinck and coworkers determined that when copper plates out it forms very small metallic nuclei [41]. They found the reaction to be activated by visible light. In another experiment, researchers placed wafers in a carrier into a tank filled with 0.5 %HF and 10 ppb of Cu for 5 minutes followed by a water rinse and drying step, the surface roughness of the wafers did not increase as observed with a light-scattering technique [34]. After immersion of these same wafers into a clean APM solution (5 minutes) and a subsequent water rinse and drying step, the surface roughness increased. In Figure 2.15 the light-scattering plot of the LPD distribution is shown. High concentration of surface roughness (haze) is observed at the top portion of the wafer as positioned in the carrier, and some rough areas are on the side. This pattern is reproducible and correlates with the position of the wafer in the Cu-spiked HF tank. It is concluded that this pattern is caused by the light intensity distribution pattern on the wafer while it was immersed in the Cu-spiked HF. On regions that had high light intensity, more copper is plated than those with lower light intensities. For this reason, the left, right, and bottom of the wafer are not roughened because the wafer carrier and tank masked the wafer. The LPD created in these process are magnified in Figure 2.16, and it can be seen that these LPD are circularly symmetric as expected from Figure 2.11.

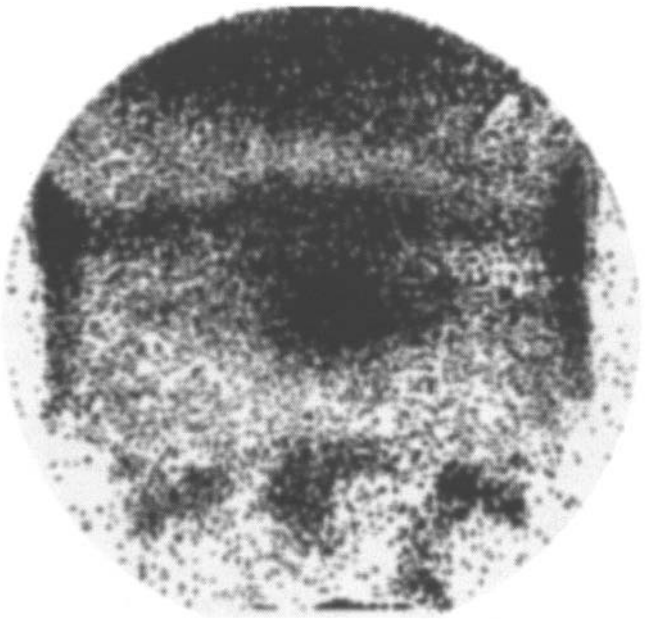


**Figure 2.15.** Light point defect distribution on a bare silicon wafer after dipping in Cu-spiked HF followed by a clean APM step [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns., M. M., *Journal of the Electrochemical Society*.

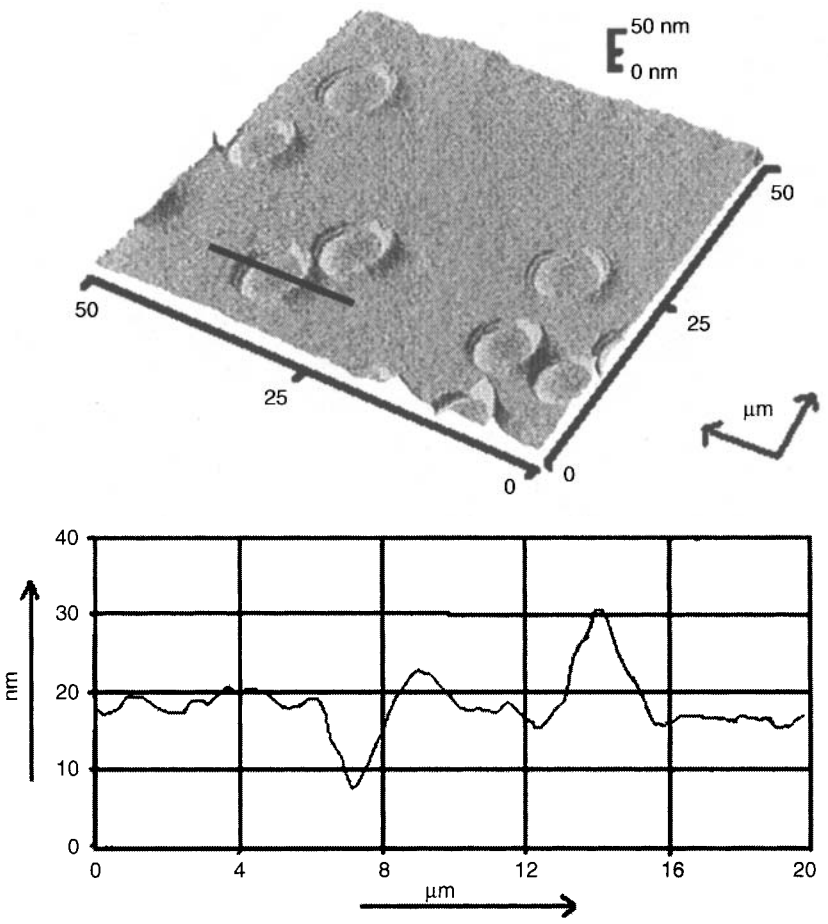



**Figure 2.16.** Atomic force microscopy picture of defects formed in Fe-contaminated APM [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

### 2.3.6.3 *Catalyzed $H_2O_2$ Depletion*

Clustered LPD is specific for APM [30]. Roughening of the surface does not occur in isolated spots on the wafer – surface asperities are clustered and distributed randomly. The roughening and clustered-LPD formation is related to the decomposition of the peroxide in the APM. Surface roughening of silicon only occurs when wafers, and in particular hydrophobic wafers, are immersed in a metal-contaminated APM solution. In the case of iron contamination, roughening only occurs in places where the peroxide is visually decomposing. In addition, this process depends on the iron concentration and appears after a certain period of exposure. The result of this type of micro-roughness is poor gate-oxide integrity (GOI). It has been found that there is a direct correlation between breakdown and clustered LPD [30]. However, the poor GOI is not specifically due to the roughness of the silicon surface. If the iron is thoroughly removed, the GOI is not affected by the roughness left on the surface [42]. The local high iron concentration can also be

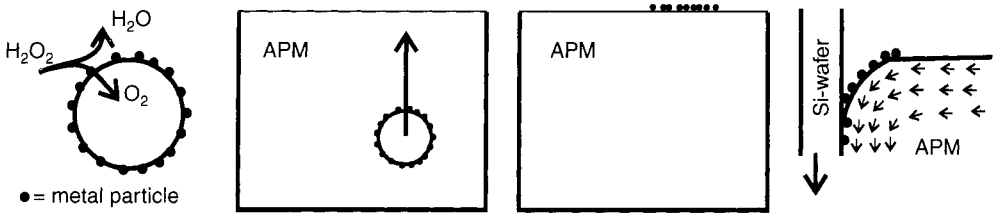



**Figure 2.17.** Schematic of the mechanism of cluster-LPD formation in Fe-contaminated APM. From left to right. Metal-oxide particles catalyze the decomposition of $H_2O_2$ thereby forming gas-bubbles. These bubbles grow and transfer metal oxide aggregates on the gas-liquid interface to the liquid surface (middle two pictures). When wafers are immersed, these aggregates are smeared over the surface as a cluster [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

visualized by a mapping of the minority carrier lifetime (MCLT) that is lower in places where the clustered LPD are found.

This phenomenon is explained by a sequence of events (Figure 2.17) that start with deposition of iron oxide aggregates on the surface and subsequent selective etching of the silicon surface. Iron (III) is poorly soluble in APM solution and will aggregate into small particles. These aggregates prefer to be located at gas-liquid interfaces. An example of an identical phenomenon in daily life is the oily substance floating on the surface when tea is prepared with Ca-rich water. Ultra-small $CaCO_3$ particles float on the surface and form a film that appears oily. In the case of APM, these particles are transferred to the surface. These particles, or iron-oxide aggregates, are catalysts for the decomposition of $H_2O_2$ to oxygen. The iron oxide aggregates are located at the gas-liquid interface of the $O_2$ bubble. When the bubble is large enough, it will emerge on the surface leaving a cluster of particles. At the moment a dry wafer is immersed in the Fe-contaminated APM bath full of oxygen bubbles, these clusters of particles will deposit at the gas/liquid/solid interface (*i.e.* where the wafer surface makes first contact with the liquid). Particle deposition will be enhanced by the convection of the liquid which is perpendicular to and in the direction of the substrate surface [43]. As particles cluster at the surface they will be smeared over the silicon surface resulting in lines of clustered LPD parallel to the immersion direction. This explains the initial LPD formation and why they are clustered. However, these particles are too small to be seen with light scattering techniques.

Iron oxide aggregates are extremely effective in decomposing $H_2O_2$; it is therefore expected that $H_2O_2$ becomes depleted close to the particle. Due to this absence, the silicon close to the iron oxide aggregate will be etched. The etching rate depends on the $H_2O_2$ concentration (Figure 2.4). Near the iron-oxide aggregate, the etching rate will be low and further away from the iron oxide aggregate the $H_2O_2$ concentration will increase, thus, the etching rate will be enhanced. At the point where the local $H_2O_2$ concentration exceeds 3 mmol/L etching suddenly will stop. This will result in an pattern in the silicon that is a circular hole with a plateau in the center – a ring is etched around the iron-oxide aggregate. The etch products, silicates, are poorly soluble and will deposit close to this hole. This phenomenon describes the results in Figure 2.16 and is depicted in Figure 2.18. The circular holes have a diameter of 2–5.5 μm, and the maximum etch depth difference between the center and the edge of the hole is 10 nm while the etch products form a wall 12 nm high.

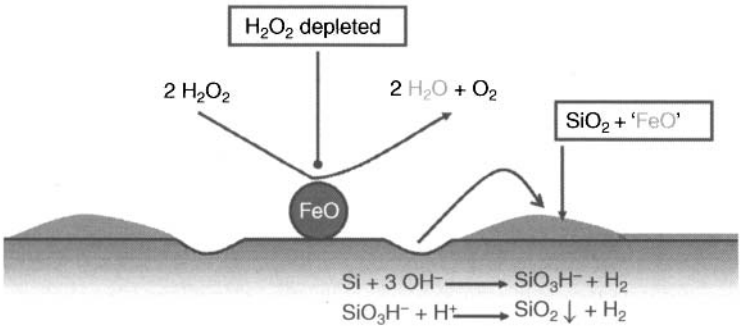



**Figure 2.18.** Schematic of hydrogen peroxide concentration profile around an Fe precipitate and the resulting etch profile. Within the circle, the $H_2O_2$ concentration is below an 3 mmol/L [34]. Reproduced with permission of ECS – The Electrochemical Society from Knotter, D. M., Gendt, S., Mertens, P. W., and Heyns, M. M., *Journal of the Electrochemical Society*.

## 2.3.7 Metal-ion Contamination and Complexing Agents

Surface roughening is not the only problem caused by metals dissolved in the APM. Metals are also problematic because they are in the chemical oxide layers. It is found that the amount of metal on a silicon surface left after an APM correlates almost linearly with the amount of metals present in the APM (Figure 2.19) [44]. If these metals are not removed thoroughly, then metals will cause weak spots in the oxide layer or diffuse into the bulk silicon. Most problems due to the incorporation of metals can be solved by a subsequent hydrochloric acid hydrogen peroxide mixture (HPM)

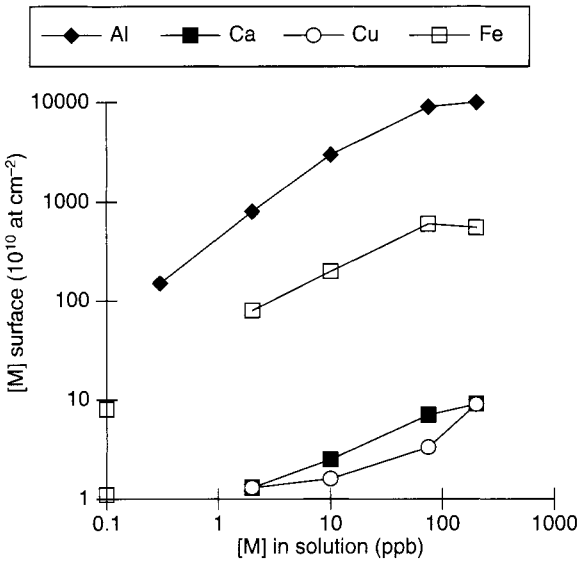


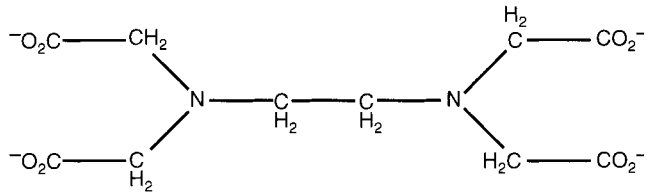

**Figure 2.19.** The amount of metal on a Si wafer after immersion in various concentrations of contaminated APM solution [44 Mouche]. Used with permission L. Mouche.

step or, more effectively, by the dissolution of the chemical oxide in HF. If the HPM particle problem or HF drying problems are under control, the purity of the APM chemicals is not critical as long as formation or deposition of catalytic-active metal particles that cause surface roughness problems can be prevented.

A method for avoiding the incorporation of metals into the chemical oxide is the addition of complexing agents to the APM solution [45]. Complexing agents are able to prevent metal ion precipitation from the APM cleaning solution onto the wafer surface [46]. They compete with the surface silanol groups to form metal-ion complexes. If the complexing agent forms a strong and stable complex with the metal ion, it will not precipitate or interact with the silanol groups. Another reason for the use of complexing agents is to stabilize the hydrogen peroxide. Metal ions complexed with these agents become de-activated with regard to the catalytic decomposition reaction.

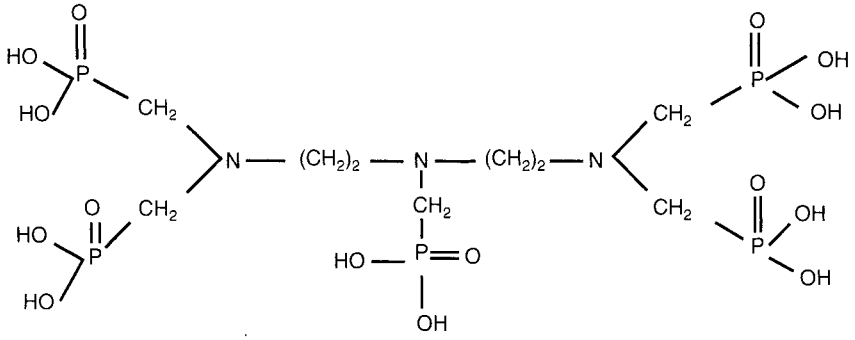
Complexing, chelating, sequestering, or coordination agents are compounds whose molecules can form several coordinate bonds to a single metal ion. Chapter 4 discusses these types of molecules. The most common and most widely used complexing agents are those that coordinate to metal ions through oxygen or nitrogen donor atoms or through both. Another large group of complexing agents is (poly) phosphate. Complexing agents are used in many fields, such as laundry, nutrition, medicine, scale prevention, chemical analysis, catalysts, *etc.* Nature cannot do without them. In hemoglobin, a porphyrin ring forms a strong complex with iron to transport oxygen. Some examples of industrial Fe (III) complexing agents are given in [47]:

***EDTA***: Ethylenediaminetetraacetic acid (EDTA) is the most common complexing agent:



The coordinating groups in EDTA are two amine groups and four carboxylic groups that are capable of wrapping around a central metal ion, such as Fe (III) and satisfy the octahedral coordination requirements of Fe (III). The effectiveness of EDTA, which is the first synthetic chelate used in nutrient solutions for hydroponics, is limited to pH 6 or lower.

***DTPMPA***: Diethylenetriamine penta(methylenephosphonic acid), DTPMPA, is an example of a phosphate. It strongly complexes Fe(III) in APM solutions.



Phosphonates reduce the metal-catalyzed decomposition of hydrogen peroxide in APM and inhibit the growth of metal aggregates [48]. Experiments with DTPMPA show that the decomposition rate of the hydrogen peroxide in "clean" APM ([M] < 0.1 ppb) is reduced by the addition of DTPMPA from a half-life of 60 to 300 hours. The ratio between complexing agent and the metal is critical. To reduce the number of added LPD and the decomposition rate of the $H_2O_2$, the molar ratio of DTPMPA to iron must be larger than 2. In fact, increased decomposition is observed for smaller ratios because DTPMPA breaks down the iron-oxide aggregates into smaller aggregates that remain catalytically active. The amount of iron that remains on the surface after a wafer dipped in a 1 ppb-Fe-spiked APM solution containing 2 equivalents (compared to Fe) of DTPMPA is below the detection limit of $2 \times 10^9$ atoms/cm$^2$. This compares very well with the same APM bath, but without DTPMPA leaving $10^{12}$ atoms/cm$^2$ on the silicon surface. However, it is expected that this compound will be less effective in removing other metal ions.

Addition of chelating agents is seen as key to the solution of an APM only cleaning scheme, the so-called "single-chemistry"clean [7]. Furthermore, replacing ammonia with tetramethyl ammonium hydroxide (TMAH) is considered to extend bath-life times. However, there are issues with this approach:

1. Replacing $NH_3$ by a quartinary ammonia species, $N(Me)_4^+$, will result in a loss of the complexing capabilities of the $NH_3$. Ammonia is known to form strong soluble coordination complexes with some metal ions, such as copper, while $N(Me)_4^+$ does not. In a standard APM solution, copper deposits relatively poorly onto the silicon surface. This loss of metal-deposition inhibition can be compensated by the addition of extra complexing agents.
2. Complexing agents do usually contain amine functionalities that are known to be unstable in hydrogen peroxide as they can be oxidized and can lead to loss of process control. In a standard APM, this is also the case with the ammonia, but it is a slow process and this amine is present in excess. Complexing agents are present in ppm amounts and if their concentration decreases below a certain limit, they can have an adverse effect on the cleaning process.
3. A mixture of chelating agents is required because formation of stable coordination complexes requires the appropriate Lewis-acid/Lewis-base combination. Hard Lewis bases, such as alkali, alkali earth, and many high-valent-transition metal ions combine well with hard Lewis acids, such as ether and carboxylic acid oxygen atoms. Soft Lewis bases, such as low-valent metal ions from group 10 and 11, form strong complexes with soft Lewis acids such as amine and phosphines.
4. If all of the previously mentioned problems are controlled, the rinse process can make matters worse. After the APM, the wafers have to be rinsed in DIW. Due to the carry-over layer and the acid-base equilibria on the silica surface, the wafer surface will be negatively charged during the first moments in the rinse water. In this period metal ion contamination from the DIW is strongly attracted to the wafer surface.

The metal performance of the clean will be dependent on the quality of the DIW. This is not necessarily stable. A final acidic rinse or treatment is still recommended.

### 2.3.8 Diluted APM

The ratio of the reactants in the APM mixture and the reaction temperature is the subject for optimization [4]. There is a trend to reduce the chemical consumption and use diluted versions of the APM clean. The chemicals ($H_2O_2$ and $NH_4OH$) are a source of contamination that can deposit on the silicon surface [49, 50] although chemical purities are improving. They contain particles and metals while the DIW is usually very clean. Dilution of the chemicals will result in cleaner solutions and, in many cases, cleaner wafers. Using fewer chemicals also has an economical benefit, but not many fabs will take advantage of saving money on chemicals at the risk of production. The drive for dilution usually is driven by process improvement.

In reducing the chemical concentration, the anticipated improvements must be compared to the metrics achieved with the conventional process:

1. Because APM is used to remove particles, the particle removal efficiency must remain constant or improve. A good assessment is to perform particle addition and removal tests, find the worst case with the process of record, and compare to the new process.
2. Since APM etches silicon, the etching rate should be the same. This is, in most cases, very critical. The etching rate of thermal oxide layers should be tested by performing the step with an increased process time as the etching rate is too slow to observe a significant decrease and also running multiple lots for assessing device performance.

There are three parameters that can tune the cleaning performance of the APM:

1. $H_2O_2$ concentration.
2. $NH_3$ concentration.
3. Temperature.

The $H_2O_2$ concentration, compared to the 1:1:5 ratio, can be reduced by a factor of ten without achieving significant surface roughening. The trouble with lowering the concentration is surface roughening, but even with high concentrations of $H_2O_2$, roughening can still occur. Roughening is due to metal impurities that are present in the $H_2O_2$; consequently, higher concentrations of $H_2O_2$ result in more metal impurities in the APM solutions [30]. The lowest limit is somewhere around 3 mmol/L, which is close to a 1:1:2500-mixture (based on a 30% w/w solution of $H_2O_2$). However, a small consumption or deviation can put wafers in jeopardy. By the aid of complexing agents, the $H_2O_2$ concentration can be kept constant and homogeneous. However, it is safer not to go to extremes. Slowly lowering the $H_2O_2$ concentration will increase the pH and, consequently the etching rate (Eq. 2.5).

The ammonia has an optimal concentration for particle removal efficiency. At high concentrations, the etching rate of silicon dioxide will increase and

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# 3

# The Chemistry of Wet Etching

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*Abstract*

Silicon-containing materials (Si, $SiO_2$, $Si_3N_4$) are etched with fluoride-based aqueous etch solutions or by water. In the latter case, acids are required to catalyze the dissolution reaction, or a base is needed to keep the reaction product, silicic acid, in solution. For the etching of silicon, an oxidation agent accelerates the reaction rate. The dissolution reaction of all the materials is described by a repetitive two-step reaction cycle:

1. The activation of the surface monomolecular layer (Si-H to Si-OH or Si-F; Si-OH to Si-F; Si-$NH_2$ to Si-OH or Si-F)
2. Dissolution of this activated layer that requires breaking Si-Si, Si-O, or Si-N bonds.

Selectivity is obtained by modifying the chemical solution and tuning the rate limiting step. Knowledge of these phenomena resulted in HF etching of $Si_3N_4$ being selective towards $SiO_2$.

***Keywords:*** Selective etching, reaction mechanism, oxidation potential, HF, water, phosphoric acid, buffered oxide etch, silicon, silicon dioxide, silicon nitride

## 3.1 Introduction and Overview

The origin of the word "etch" can be found in the Dutch word "etsen" and the German word "ätzen", both of which relate to the old high German word "azzen" that means to cause to eat. Etching is a corrosion process, in which material is slowly "eaten" away, usually in a chosen pattern. For semiconductor processing applications, wet etching is one of the oldest methods for delineation, but has been replaced by other methods in modern fabs. For the most advanced integrated circuit (IC) technology, wet processing is only used to etch unpatterned layers such as film removal from back surfaces of wafers and hard mask removal from the front surface.

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Nevertheless, etching processes are critical with respect to the desired result that must be achieved. Wet etching processes are able to achieve high selectivity with respect to the underlying layer. They also can etch material selective to the crystal structure which dry etching cannot achieve. This chapter will focus on the chemistry of wet etching for the following materials:

1. $SiO_2$
2. Si
3. $Si_3N_4$

### 3.1.1 Definition of Etching

Today, etching used for the manufacture of IC devices is performed by both dry and wet processes. Dry etching is performed using plasma in which both chemical and physical components remove material with moderate selectivity and high anisotropy due to:

1. A physical component that provides vertical directionality.
2. A chemical component that causes polymer deposition to protect the sidewall.

Due to this high anisotropy, plasma is the main etching method for delineation of critical dimension lines and spaces. Unfortunately, most wet etching processes do not preferentially remove material in specific directions as does dry etching; most wet etching processes are isotropic. There are, however, a few examples of anisotropic wet etch processes. The anisotropy is obtained by using crystal plane selectivity or controlled diffusion of reaction components. Figure 3.1 shows a comparison of an isotropic and an anisotropic etch.

Another important component of etching is selectivity – both to underlying films and also to the photoresist that protects the film from being etched. An advantage of wet etching is its high degree of selectivity for a specific material. The preferential reactions are obtained by using different materials. For etching, this requires the removal of an area of the surface film in favor of a surface region that resists the etching activity – the photoresist pattern. The resist is usually an organic polymer film and because it is activated by light is called photoresist or resist. The resist is applied on top of the substrate film, exposed to light, and then developed to leave a patterned film. Developing photoresist is also a wet etching process – the physical property of the exposed resist has changed and that enables the selective dissolution of either the exposed or unexposed areas. The following paragraph explains why different materials can be etched selectively.

### 3.1.2 The Physics of Wet Etching

The goal of an etching process is to dissolve a material. For wet etching, water is the solvent of choice. Fortunately, the materials used in IC devices are unaffected

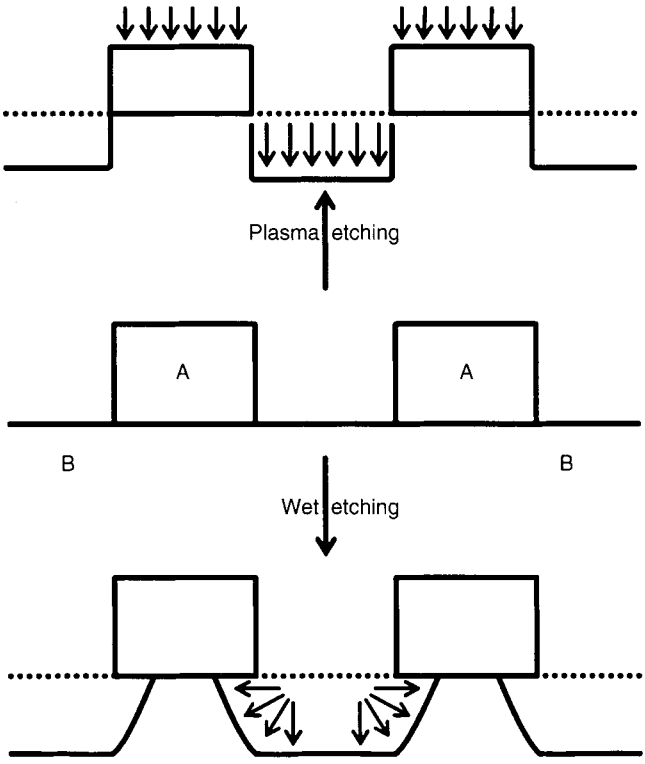


**Figure 3.1.** Difference between plasma etching (an isotropic) and wet etching (isotropic). A is the photoresist mask and B is the film to be etched. Used with permission of the author.

or dissolve very slowly in pure water. Therefore, help is required to get the material into solution. Most etching processes consist of two distinct reaction steps:

1. Activation of the surface layer.
2. Dissolution where only the activated surface layer dissolves.

In the activation step, the surface layer is transformed by one of the solution components into a product that is readily dissolved in water. Because only the top exposed layer is etched, the process proceeds iteratively in which the target material is removed molecularly layer-by-layer.

For the dissolution of metals, such as aluminum, copper, and silicon, an oxidizing agent is needed to oxidize the metal into a soluble metal salt. Other materials such as $Si_3N_4$ and $SiO_2$ need transformation at a termination group. For example for silicon nitride etching, a Si-$NH_2$ surface group is transformed into a Si-OH group. In silicon oxides, a Si-OH group reacts with HF to form a Si-F group.

The dissolution step depends on the solubility and/or diffusion coefficient of the material being etched, but also on the solvating components which are usually different from the activation reagents. These solvating components break the chemical bonds that hold the activated surface layer to the bulk material and

subsequently stabilize (solvate) the newly released ionic species. Common reactants are $OH^-$ or $H^+$ which are intrinsically present in water.

The rate determining reaction step of the etching process is either the activation or dissolution reaction. Controlling the rate determining step coupled with differences in properties of the materials in the etching environment can be exploited to specify the target material to be etched. Examples of properties that can be exploited to establish etch selectivity include:

1. Difference in bond strength.
2. Absence of the proper reactant.
3. Formation of inhibiting coatings.

### 3.1.2.1 *Difference in Bond Strength*

Since wet etching is a chemical process, etching rates are determined by the strengths of the chemical bonds that holds the material together. Breaking these bonds is the critical aspect of the etching process. For example, etching a silicon-containing material, such as silicon, silicon dioxide, or silicon nitride, are all very similar. In all three cases a Si-OH unit is etched from the matrix, as shown in Figure 3.2. The removal reaction occurs through three subsequent water addition reactions to the bond that keep the Si-OH unit in the solid matrix. If this reaction step is rate determining, etching rate selectivity for these three materials can be determined by their respective bond strengths. The Si-Si, Si-O, and Si-N bond

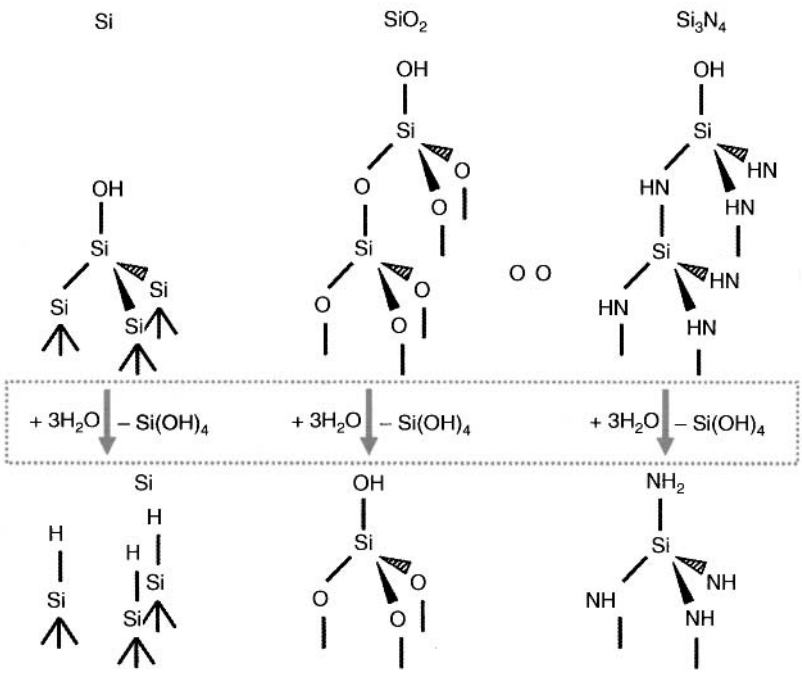


**Figure 3.2.** Etching of Si-OH in its matrix for Si, $SiO_2$, and $Si_3N_4$. Prior to the etching process, Si-H has to be oxidized to Si-OH, and the $NH_2$ group has to be substituted by OH. Used with permission of the author.

strengths are 327, 810, and 429 kJ/mol, respectively; consequently, Si will dissolve fastest, followed by $Si_3N_4$, and then $SiO_2$.

#### 3.1.2.2 *Absence of the Proper Reactant*

Another method to obtain etching selectivity is by modifying the reactants. For example, etching of silicon requires that the surface silicon atom is H-terminated for oxidation to Si-OH. This surface layer activation step requires an oxidizing agent. By decreasing the oxidation potential of the solution (*e.g.* leaving the oxidant out) the etching of silicon will cease while the etching of $SiO_2$ will continue. In the case where both exposed materials must be oxidized before being dissolved, the oxidant is at a concentration too low to oxidize one material but high enough to oxidize the targeted material, thus, in this case, tuning of the selectivity is done with the oxidation potential of the solution. An example of this method of selection is the etching of silicon in the presence of a photoresist coating. Both silicon and resist must be oxidized before dissolving into an aqueous solution. Most aqueous-based etch solutions cannot oxidize the hydrocarbons in the organic-based photoresist; however, the silicon is oxidized by water-based oxidizing agents.

#### 3.1.2.3 *Formation of Inhibiting Coatings*

During the etching process, a protective layer can form on the films, sometimes preferentially, preventing contact with the etching solution. Inhibiting coatings can be obtained by several methods:

1. One of the etching solution ingredients can form an insoluble material on top of one of the films or substrate. This can occur by a chemical reaction between the solution ingredient and the dissolving substrate material (*i.e.* $AlF_3$ in buffered HF solutions).
2. Surfactants can selectively adsorb on one of the surfaces. This weak physical interaction with the surface can inhibit the etch reaction.

## 3.2 Silicon Dioxide Etching

Etching of silicon oxide-based material is the most common etching process in IC manufacturing. Typically, these materials are used for insulation and dielectric layers and include thermally grown, chemically vapor-deposited (CVD), plasma-deposited tetraethoxyorthosilicate (TEOS), wet chemically applied silicon dioxide, and also multi-component silicate glasses, such as boron or phosphorus silicate glasses. A general name for these materials is vitreous silicon dioxide. All of these films are etched using fluoride-based chemistries. Less common etchants with low etching rates are hot acidic and hot caustic solutions. Silicon dioxide etching is also used in cleaning steps to remove native oxide or chemically grown oxide layers [1].

To remove the relatively inert silicon dioxide, this material must be transformed into a water soluble compound. In HF, the water-soluble reaction product is hexafluorosilicic acid, $H_2SiF_6$ (Eq. 3.1) and, in an alkaline solution, this is meta-silicic acid (Eq. 3.2) that will further deprotonate in the high pH solution (Eq. 3.3).

$$SiO_2 + 6\,HF \rightarrow [\,SiF_4 + 2\,H_2O + 2\,HF\,] \rightarrow H_2SiF_6 + 2\,H_2O \quad (3.1)$$

$$SiO_2(s) + OH^- \rightarrow SiO_3H^- \quad (3.2)$$

$$SiO_3H^- + OH^- \leftrightarrow SiO_3^{2-} + H_2O \quad (3.3)$$

The etching rate of silicon dioxide strongly depends on the way it has been deposited or grown – for example, the dopants present in the $SiO_2$ or the amount of damage that has been introduced by processing (*e.g.* implantation process or CMP – chemical mechanical polishing). The density, porosity, residual stress, microstructure, defect density, exact stoichiometry, and the purity of silicon dioxide films all impact etching rates [2]. There are a number of examples of etching rate differences caused by these parameters:

1. Thermally-grown or oxide layers annealed above 500°C are very dense and have a $SiO_2$ stoichiometry, thus, have low etching rates.
2. Wet chemically deposited silicon dioxide from TEOS (spin-on-glass – SOG) has a very high etching rate because it contains water and residual organics. Spin-on-glass is non-stoichiometric, has a high oxygen content, and is porous.
3. A physically damaged silicon dioxide layer etches faster than undamaged oxide. During CMP processing, slurry particles abrade the oxide surface causing a large number of defects, which cause an increase in etching rate due to more surface area and non-stoichiometric silicon dioxide.
4. Silicates that have been doped typically have high etching rates. For phosphorus doping (PSG), etching rates increase with the doping concentration because of the incorporation of $P_2O_5$ which is water soluble. However, this is not the case for $B_2O_3$ addition (BSG) – the etching rate decreases with low borate additions; however, after a threshold concentration is exceeded, the etching rate increases.
5. At the silicon/glass interface, a type of borosilicate glass is formed after the high temperature diffusion of boron from a borosilicate glass into silicon. Residues of the borosilicate glass remain in or on the silicon after the removal of the bulk BSG in HF. After an oxidation of this thin silicon layer, it dissolves in HF.
6. Silicon oxynitrides, created from the addition of $Si_3N_4$ to $SiO_2$, form films that etch slower than $SiO_2$.

### 3.2.1 Hydrofluoric Acid Etching

Hydrofluoric acid (HF) was first prepared by Scheele in 1771 as outlined in [3, 4]. Since organic polymer bottles and containers were unknown at that time, it is likely that he prepared or stored the first HF in containers made of glass. Therefore, it can be assumed that he also discovered that it etches glass. The products of this etch

reaction were analyzed by Berzelius 50 years layer who found that they were tetrafluorosilane ($SiF_4$) and water [5]. Tetrafluorosilane further reacts with HF to form the strong acid, hexafluorosilicic acid [3, 4, 6]. In the production of integrated circuits on silicon wafers, HF is the choice for etching silicon-containing material [7]. However, etching of vitreous $SiO_2$ and other silicate glasses with HF is also widely used in the glass, flint, oil recovery, and surface micromachining industries [8].

For the IC manufacturing processes, two types of HF-based etchants are commonly used for etching $SiO_2$ – dilute HF (DHF) and buffered HF (BHF) solutions. Dilute HF is prepared by diluting commercially available 49 or 50 wt% HF. Concentrations used in typical IC processing range from 0.05 to 50 wt% of HF. Hydrofluoric solutions are normally used for removal of thin layers of silicon dioxide – typically a native or chemical oxide layer. Due to selective evaporation of either HF or water, the concentration and, consequently, the etching rate of DHF are not stable over time. Alternatively, BHF, also known as buffered oxide etch (BOE), exhibits better etching rate stability over time because HF does not evaporate from these solutions. Buffered HF is used in several stages of IC manufacturing processes:

1. Backside etching.
2. Etching of contact holes.
3. Removal of sacrificial oxide layers.
4. Removal of doped oxides after diffusion.
5. Structuring oxide or nitride layers.

Commercially, BHF is sold as a mixture of 40 wt% $NH_4F$ (10.8 mol/L) and 49–50 wt% HF (27 mol/L) in an $n$:1 ratio, respectively. For example, BOE 7:1 is a mixture of 7 volume parts of the $NH_4F$ solution and 1 volume part of the HF solution. Other advantages of BHF over DHF are reduced photoresist lifting problems when etching oxide layers using an organic photoresist mask and the ability, although with a small process window, to selectively etch silicon dioxide in the presence of aluminum. Selectivity of BHF towards Al can be improved by addition of dihydroxyalcohol or glycerol. Problems with BHF include surface wetting during the etching of small structures in oxide layers and particles that precipitate out of an oversaturated ammonia fluoride solution. The wetting problems can be solved by the addition of a surfactant and maintaining the proper temperature that can prevent crystal precipitation. Crystallization of $(NH_4)HF_2$ has been observed for BOE 12:1 below 0°C and for BOE 4:1 below 24°C. Re-dissolving the crystals is a slow process, and it is recommended to dispose of the chemical.

The etching mechanism of $SiO_2$ in HF-based solutions was elucidated by several authors [9, 10, 11]. The $SiO_2$ network is stripped by removing the surface silicon, which is present as silanol groups in a repeating process as depicted in Figure 3.3. As the surface silanol group is removed, the silicon beneath the surface is released by breaking a Si-O bond and becomes a surface silanol group (Si-OH). To remove a surface silanol group, a Si-O has to be broken and replaced by a Si-F bond. Replacement of the first Si-O bond by a Si-F bond is the rate determining reaction step in the etching of $SiO_2$ in HF. Thus, the activation of the surface layer, which transformations the silanol group (Si-OH) into a surface SiF group, is a relatively slow reaction.

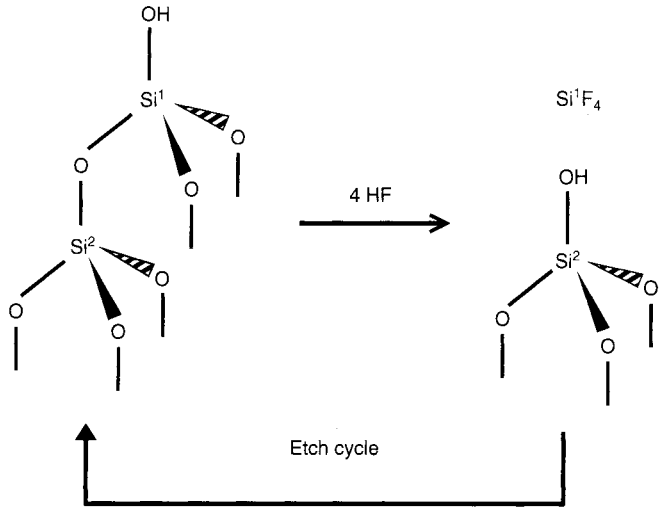


**Figure 3.3.** Depiction of layer-by-layer etching of $SiO_2$ by HF [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

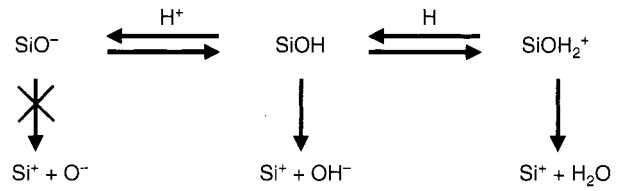


**Figure 3.4.** Acid/base equilibrium of the amphoteric surface silanol group. Used with permission of the author.

In water, surface silanol groups show amphoteric behavior, which means that they can lose or take up a proton as depicted in Figure 3.4. With respect to the reaction sequence, the relative concentration of each of the three surface groups determines the reactivity of the surface layer. If the silanol group is deprotonated, an $O^{2-}$ must be replaced although removing such groups is very difficult. Replacing $OH^-$ from the neutral silanol is possible, but it is 1000–1500 times slower that the removal of $H_2O$ from the protonated silanol, $SiOH_2^+$ [11]. The surface concentration of the three different surface groups depends on the $pK_a$ values of the protonation reactions and on the pH. Figure 3.5 shows the relative concentration of $SiO^-$, SiOH, and $SiOH_2^+$ on a $SiO_2$ surface plotted as a function of the pH. At a pH of 2 the concentrations of $SiO^-$ and $SiOH_2^+$ are equal, but very low while the net surface charge is zero. Therefore, the iso-electric point (IEP) or point of zero charge (pzc) of $SiO_2$ is at pH 2. Below pH of 2, the concentration of $SiOH_2^+$ increases and above the concentration of $SiO^-$ increases. The concentration of $SiO^-$ does not increase continuously because the more negative the surface charge becomes, the more difficult it will be to extract another positive charge, *i.e.* a proton. Similar effects are to be expected with the protonation reaction at pH values below 0, but not enough

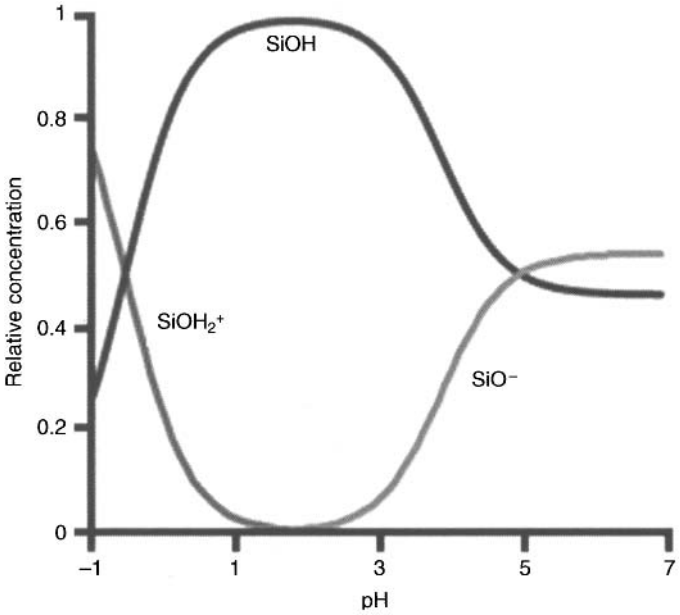


**Figure 3.5.** Relative concentrations of $SiO^-$, SiOH, and $SiOH_2^+$ on a $SiO_2$ surface in water. Based on kinetic parameters in reference [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

data points were available to quantify this process. In conclusion, the lower the pH, the easier it will be to transform a surface SiOH (or $SiOH_2^+$) group into a SiF group.

When the surface is in the proper condition for the substitution reaction, active fluorine species must be present near the reaction site. The active species in HF that dissolve the $SiO_2$ network are $HF_2^-$ and $H_2F_2$. The difluoride molecules are the active species and not the monofluoride species because the difluoride assists in the removal of the $OH^-$ (or $H_2O$) and at the same time bring a fluoride close to the $Si^+$ site, as depicted in Figure 3.6. Furthermore, the reaction with $HF_2^-$ is 2000–3000 times faster than the reaction with $H_2F_2$ because the fluorine that must be transferred in $H_2F_2$ is further away from the $Si^+$ site than it is in $HF_2^-$. In $HF_2^-$, the F-H-F bond angle is nearly 180° while the square shaped $H_2F_2$ molecule has a bond angle closer to 90°. It means that in addition to the surface composition, the configuration of the solution species determine the dissolution rate [11].

There are several fluoride species present in an aqueous solution, and these species are in equilibrium, shown in Figure 3.7. The concentration of the active fluoride species depends on the pH and the total fluoride concentration ($C_F$). The pH can be modified by addition of acids or bases. The calculation of the difluoride concentration is given by the following equations used for determining the concentrations of the species in the HF solution [12, 13]:

$$[H^+]\,[F^-] \,/\, [HF] = 6.85 \times 10^{-4}\ \text{mol/l} \tag{3.4}$$

$$[HF_2^-] \,/\, [HF]\,[F^-] = 3.963\ \text{l/mol} \tag{3.5}$$

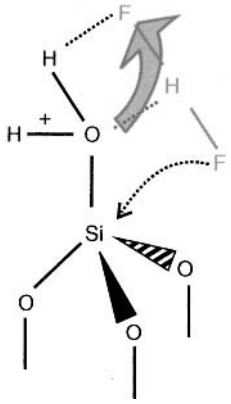


**Figure 3.6.** Difluoride ($H_2F_2$) reaction with Si showing the substitution mechanism [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

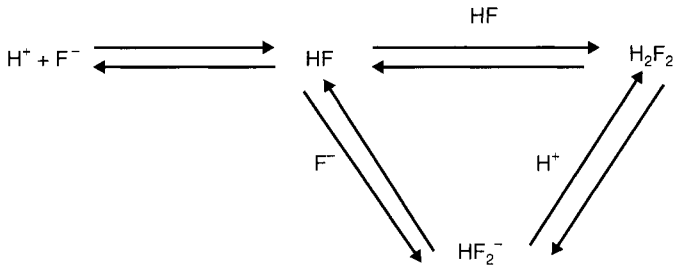


**Figure 3.7.** Equilibrium reaction between fluoride species. Used with permission of the author.

$$[H_2F_2] \,/\, [HF]^2 = 2.7\ \text{l/mol} \tag{3.6}$$

$$[H^+] + [\text{Cation}^+] = [F^-] + [HF_2^-] + [\text{Anion}^-] \tag{3.7}$$

$$C_F = [F^-] + [HF] + 2[HF_2^-] + 2[H_2F_2] \tag{3.8}$$

Where an example of a $Cation^+ = NH_4^+$ and of an $Anion^- = Cl^-$ assuming full dissociation of *Anions* and *Cations*. Since $[Cation^+]$, $[Anion^-]$, and $C_F$ are known concentrations, five unknown concentrations are left in five equations. This means that all concentrations are fixed. This calculation is a rough approximation used to estimate the respective concentrations. A calculation that includes actual ion activity was made by Kolasinski [14].

In Figure 3.8 the concentrations of the mono and difluoride species in an HF solution with a total fluoride content of 1 mol/L are plotted as a function of the pH. At very low pH, all fluorine species are neutral, and equilibrium is set between the monomer and dimer of HF. Increasing the pH results in the deprotonation of

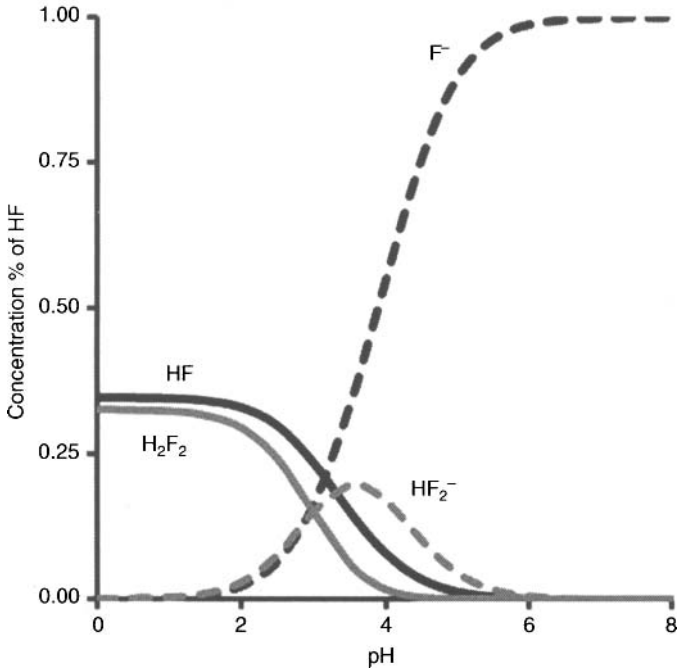


**Figure 3.8.** Concentration of F-containing species as function of pH in water with $C_t$ = 1 M (~2 wt% HF) based on reference [13]. Reproduced with permission of ECS – The Electrochemical Society from Verhaverbeke, S., Teerlinck, I., Vinckier, C., Stevens, G., Cartuyvels, R. and Heyns, M. M., *Journal of the Electrochemical Society.*

both the monomer and dimer. However, from pH 3-4 equilibria shifts completely in favor of the mono-nuclear fluoride species that does not react with $SiO_2$. The effect of the total fluoride concentration (Equation 3.8 and 3.6) on speciation is that dilution favors the monofluoride species – the concentration of monofluoride species is proportional to the square root of $C_F$ and that of the difluoride is $C_F^2$. Furthermore, at higher $C_F$, the maximum in $HF_2^-$ concentration will shift to higher pH values, and the maximum will increase relative to the monofluoride species.

Taking the sum of the surface and concentration effects of the reactive fluoride species, it can be concluded that the dissolution rate of $SiO_2$ in HF-based solutions is determined by the substitution of the surface silanol group to form a SiF group that proceeds along three reaction routes. The total etching rate, shown by Equation 3.12, and is the sum of these three reactions:

$$R_{H_2F_2} = k_0[SiOH_2^+][H_2F_2] \tag{3.9}$$

$$R_{1HF_2^-} = k_1[SiOH_2^+][HF_2^-] \tag{3.10}$$

$$R_{2HF_2^-} = k_2[SiOH][HF_2^-] \tag{3.11}$$

$$R = k_0[SiOH_2^+][H_2F_2] + k_1[SiOH_2^+][HF_2^-] + k_2[SiOH][HF_2^-] \tag{3.12}$$

The surface concentrations of [$SiOH_2^+$] and [SiOH] in these equations can be expressed as a function of proton concentration. The etching rate in turn can be described by the concentrations of proton and fluorine species in Equation 3.13:

$$R = k_0 \frac{K_3[H^+]}{1+K_3[H^+] + \dfrac{1}{K_4[H^+]+a}}[H_2F_2]+$$

$$k_1 \frac{K_3[H^+]}{1+K_3[H^+] + \dfrac{1}{K_4[H^+]+a}}[HF_2^-]+ \qquad (3.13)$$

$$k_2 \frac{K_4[H^+]+a}{1+a+K_3[H^+]+K_4[H^+] + K_3K_4[H^+]^2}[HF_2^-]$$

The equations appear to be complex; however, they can be simplified for pH ranges where:

1. At low pH: the surface is covered with $SiOH^+$ groups. The term "$1 / K_4[H^+] + a$" = 0 and the whole $R_2$ term is negligible.
2. At high pH: the surface is covered with $SiO^-$ groups, and $R_1$ and $R_2$ become negligible.

The reaction constants for these equations for thermal oxide are shown in Table 3.1.

Using Equation 3.13, it is possible to calculate the etching rate and the relative contribution of the different reaction routes. Figure 3.9 shows the plot of etching rate for a 0.2% HF solution as a function of pH together with the three reaction components that contribute to the rate. Surprisingly, the etching rate variation in

**Table 3.1.** Reaction constants for the dissolution of thermally-grown $SiO_2$ in HF based solutions [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

| Constant | Value[a] | Meaning of Reaction Constant |
|---|---|---|
| $k_0$ | 7(1) Å l $mol^{-1}$ $s^{-1}$ | Substitution of $SiOH_2^+$ by $H_2F_2$ |
| $k_1$ | 18(4) $10^3$ Å l $mol^{-1}$ $s^{-1}$ | Substitution of $SiOH_2^+$ by $HF_2^-$ |
| $k_2$ | 12.6(0.5) Å l $mol^{-1}$ $s^{-1}$ | Substitution of SiOH by $HF_2^-$ |
| $K_3$ | 0.28(0.06) l $mol^{-1}$ | Equilibrium between $SiOH_2^+$ and SiOH |
| $K_4$ | 13(2) $10^3$ l $mol^{-1}$ | Equilibrium between SiOH and $SiO^-$ |
| $\alpha$ | 0.85(0.06) | Variation on $K_4$ due to surface charge |

[a] The error is shown between parenthesis

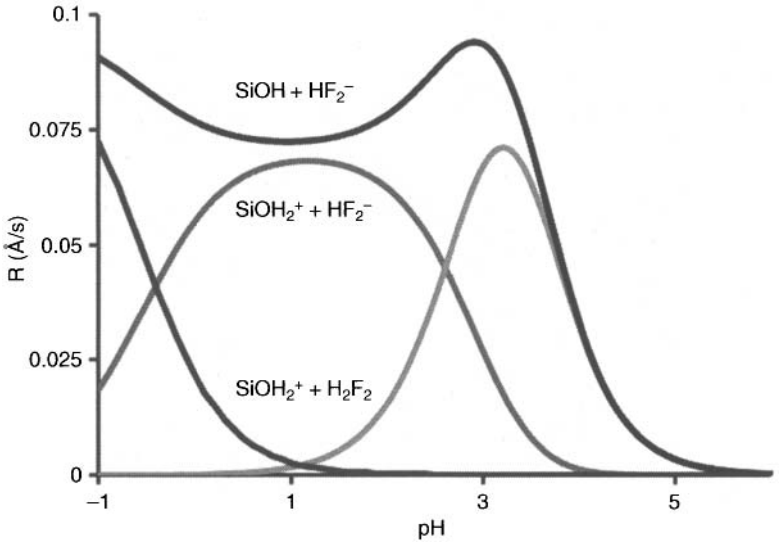


**Figure 3.9.** Dissolution rate of thermally grown $SiO_2$ in HF-based solutions with $C_t$ = 0.1 M (~0.2% HF) [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

the pH range of −1 to 3.5 is small varying between 0.072 and 0.094 Å/sec. For this pH range, the main reaction route contribution is from $k_2[SiOH_2^+][HF_2^-]$ and at the lower pH (<1) and higher pH (>1) values, the reaction velocity is maintained by $k_1[SiOH_2^+][H_2F_2]$ and $k_3[SiOH][HF_2^-]$, respectively. It is important to note that at pH <1 the active fluoride component is changing from $HF_2^-$ to $H_2F_2$. Keep in mind that at pH values < 0, this model might slightly overestimate the reaction rate because $[SiOH_2^+]$ is probably lower.

The same calculations can be done at different HF concentrations. Figure 3.10 shows etching rate plotted against pH starting from 0.01 M HF (~0.02% HF) to 27 M, which is the equivalent of a 50 wt% HF solution. Indicated in this plot is the line of aqueous HF without additives ('pure HF'). On the right hand of this line, basic components, such as ammonia (also $NH_4F$, but adding this will change the total fluoride concentration of the solution), are added and, on the left, strong acids are added.

Once the surface silanol has been transformed into surface silicon fluoride, the removal process of this SiF unit proceeds rapidly. The dissolution rate of $SiO_2$ in HF is determined by the activation step. Moreover, the successive dissolution step, breaking of the three Si-O-Si bridges, is 18–20 times faster than the activation step. The activation step is slow because the $OH^-$ group first has to be eliminated before the $F^-$ can be added to the silicon, a so-called elimination-addition reaction: Si-OH → $[Si^+]$ → Si-F. Although this process is aided by the $HF_2^-$ complexation (Figure 3.6), it remains a step with a high activation energy because an energetically unfavorable $[Si^+]$ needs to be formed. The dissolution steps are much faster because the elimination reaction is no longer required. A nucleophilic attack by a fluoride species onto the silicon in Si-F results in a nucleophilic substitution reaction, as shown in Figure 3.11. While forming a new Si-F bond, the Si-O on the opposite site breaks

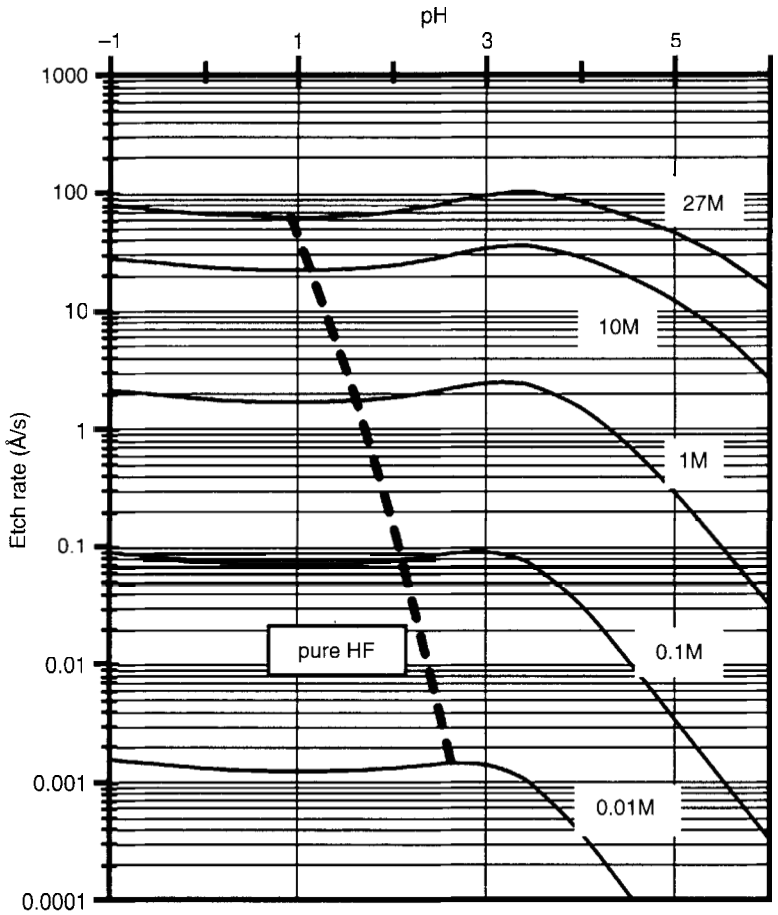


**Figure 3.10.** Etching rate of thermally grown $SiO_2$ in HF solutions with different total fluoride concentrations, data from reference [11]. Used with permission of the author.

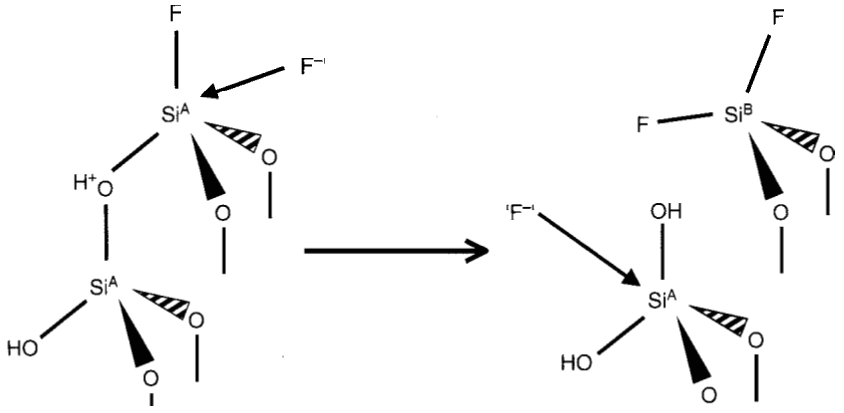


**Figure 3.11.** Etching of non-stoichiometric $SiO_4$-unit [11]. Reprinted with permission from Knotter, D. M., *J. Am. Chem. Soc.*, 122(18):4345. Copyright 2000 American Chemical Society.

slowly. Activation energies of such nucleophilic substitution reactions are lower than elimination reactions.

The reaction mechanism described thus far is the dissolution of thermally grown $SiO_2$, but it does not explain why the dissolution rates of other types of vitreous $SiO_2$ are faster. Ideally, every silicon atom in a $SiO_2$ matrix is bonded to four bridging oxygen atoms which, in turn, are bonded to two silicon atoms. The removal rate, $R_B$, of a fully bridged $Si^B$ atom out of the $SiO_2$ matrix is determined by the substitution of the surface OH group and will be identical to the etching rate of thermally grown $SiO_2$. In less ideal $SiO_2$, not every oxygen atom is bridged between two silicon atoms, instead some oxygen atoms bond to hydrogen atoms and silicon atoms bond to non-bridging atoms such as F. When such an imperfect silicon atom, $Si^A$, emerges on the surface, the surface OH group can be substituted by $F^-$ *via* a fast nucleophilic substitution reaction and not by the less favorable elimination-addition reaction shown in Figure 3.11.

The etching rate of a less ideal oxide, $R_{tot}$, is determined by the fraction of the imperfect $Si^A$ units, $f$. It can be expressed as the sum of the two etching rates – the removal rate of the $Si^A$ unit, $R_A$, and the removal rate of the $Si^B$ unit, $R_B$:

$$R_{tot}(f) = R_A \times f + R_B \times (1\text{-}f) \tag{3.14}$$

In the case of non-stoichiometric silica, $SiO_xH_{x-2}$ with $2 < x < 2.5$, the etching rate can be expressed as [11]:

$$R_{tot}(x) = (5R_B - 4R_A) + (2R_A - 2R_B)x \tag{3.15}$$

When $x$ exceeds 2.5, the average silicon atom in the $SiO_x$ matrix will have more than one non-bridging oxygen atom. The etching rate will approach $R_A$, about 18–20 times $R_B$.

Since the etching rates of $SiO_2$ layers are expressed in metric units while kinetic calculations are done in moles or mass units, etching rates of non-stoichiometric $SiO_2$ layers can appear even higher. Silicon dioxide layers of this type are deposited using plasma techniques or by spin-on techniques, such as low-κ dielectrics and SOG. The density of these non-stoichiometric layers is lower than that of thermally grown $SiO_2$ resulting, therefore, in even higher etching rates.

### 3.2.2 Water-based Etching

The ability of water or water-based solutions to etch $SiO_2$ is known by semiconductor process engineers who have struggled with the selectivity of a freshly prepared bath of hot phosphoric acid silicon nitride etch to be discussed in Section 3.4.2. The dissolution of $SiO_2$ shown in Eq. 3.16 has an equilibrium constant of $1.1 \times 10^{-4}$, thus, 6–10 mg of $SiO_2$ will dissolve in 1 L of water at room temperature and at 100°C, about 10 times more silica will dissolve in 1 L of water [15].

$$SiO_2(s) + 2\,H_2O \leftrightarrow H_4SiO_4(aq) \tag{3.16}$$

The pH influences the dissociation of silicic acid to silicic acid mono- or di-anions:

$$H_4SiO_4(aq) + OH^-(aq) \leftrightarrow H_3SiO_4^-(aq) + H_2O \quad (3.17)$$

$$H_3SiO_4^-(aq) + OH^-(aq) \leftrightarrow H_2SiO_4^{-2}(aq) + H_2O \quad (3.18)$$

As $H_4SiO_4$ in Eq. 3.16 is removed by $OH^-$ (Eq. 3.17), more $SiO_2$ can be dissolved in water at a higher pH. In fact, the solubility increases from pH > 9.6 while at lower pH solubility remains constant [16]. For example, it is in this pH range that SC-1 (RCA standard clean-1) or APM (ammonium hydroxide hydrogen peroxide mixture) is used.

Because there is no interest to exploit the etching of $SiO_2$ in water for semiconductor processing, knowledge about the dissolution process comes from geologic literature where time scales are expressed in years, and enough time is available to reach equilibrium. Therefore, on manufacturing time scales, the dissolution is kinetically controlled, and the dissolution rate, $R$, is determined by the amount of $SiO_2$ already dissolved [17]. If the concentration of dissolved silica ($C_S$) reaches the saturation level ($C_{eq}$), then the etching rate will slow. If water does not contain any silica, the maximum etching rate is obtained, shown as:

$$R = k(1 - C_S/C_{eq}) \quad (3.19)$$

The outcome of this phenomenon is that pure water, with less dissolved silica, results in increased etching rates of silica. Hence, the high purity water used for IC manufacturing actually dissolves the silica. Consequently, storing wafers in water during an emergency or tool failure yields undesirable silica loss at process steps where no or minimal silicon/silica loss is required. Conversely, the phenomenon has been used to advantage. For $Si_3N_4$ etching, if some silica is dissolved in $H_3PO_4$, the etching rate of $SiO_2$ slows down and even stops depending on the amount of silica in the solution. The etching rate of $SiO_2$ in $H_3PO_4$ can be controlled by the amount of dissolved silica [18]. However, as the amount of dissolved silica increases, process variations in the barrier $SiO_2$ layer thickness are introduced.

Besides pH, temperature, and the amount of dissolved silica in the water, the etching rate strongly depends on the type of silica layer and the contaminants such as dopants. Therefore, it is difficult to estimate etching rate values with high reliability. The following reported data are those for thermally grown $SiO_2$. For 2.5 M NaOH (aq) the etching rate of thermal oxide is 0.01, 0.5, and 50 nm/min at temperatures of 23, 55, and 90°C, respectively [19]. Dilution of the NaOH concentration to 0.1 M reduces the etching rate to <0.02 nm/min at room temperature [20], and the activation energy of this reaction is approximately 110 kJ/ mol. In 5M KOH at 85°C, etching rates are reported to be 5 nm/min [21]. A bit more relevant for the semiconductor engineer are the etching rates of silica in standard SC-1 and APM solutions ($H_2O$:$H_2O_2$:$NH_4OH$ mixtures) which are 0.1 nm/min at 60°C and 0.37 nm/min at 85°C [22]. In fresh hot phosphoric acid, the etching rate is 0.15 nm/min at 160°C.

## 3.3 Silicon Etching

Silicon is present in several forms in and on a wafer used for IC devices:

1. Single-crystal silicon comprises the wafer and the epitaxial layers grown on the surface.
2. Polycrystalline silicon (polySi) in which the small regions of silicon have different crystalline orientations.
3. Amorphous silicon (a-Si or α-Si) where the structure lacks any crystalline ordering.
4. Amorphous polySi is sometimes used to describe an amorphous silicon layer that crystallizes during a heat treatment.

Independent of its crystallinity, silicon is in a metallic state that is difficult to dissolve. In order to successfully etch silicon, it must be transformed into a soluble state, and, therefore, it has to be oxidized to silicon dioxide. As previously discussed in Section 3.2, $SiO_2$ dissolves in an alkaline environment or in HF. Therefore, silicon etching solutions will always be composed of an oxidizing agent and an agent that dissolves silicon dioxide. In the following paragraphs, an overview of recipes used to etch silicon is presented. These recipes are not only used to pattern silicon wafers, but also to make defects in the crystal structure of the silicon visible and to etch specific silicon crystal orientations for examination in cross sectional microscopy. Lee and Polcari [23] present an overview and assessment of various methods for etching silicon.

Silicon-etching solutions can be separated into acidic- or alkaline-based mixtures. The acidic etching solutions, based on HF-$HNO_3$ or HF-$H_2O_2$, are commonly used for isotropic etching of amorphous and polySi. The application of HF-$H_2O_2$-based mixtures is limited because of the self-decomposition of $H_2O_2$. Alkaline etch solutions are anisotropic in nature and are used for the etching of single crystal silicon. The high selectivity of the alkaline etch can be employed to etch polySi selectively to silicon dioxide, aluminum, and tungsten.

The reaction mechanism of silicon etching is nearly identical to that of silicon oxide. Figure 3.12 depicts the mechanism for etching silicon. The difference is that for etching hydrogen-terminated Si, silicon (≡Si-H) must be oxidized to a ≡Si-OH. Furthermore, the removal of the Si-OH unit requires three Si-Si bonds to be broken by HF or H-OH insertion while $SiO_2$ requires three Si-O bonds to be broken.

Etching of silicon starts with a surface activation reaction: oxidation of the Si-H bond. The Si-H bond is slightly polarized with the Si being positively charged, and the H is negatively charged ($Si^{\delta+}$-$H^{\delta-}$). The Si-H units are a silicon hydrides (like silanes) and these are known to be readily oxidized with a proper oxidizing agent (Eq. 3.20) or hydrolyzed in an alkaline solution (Eq. 3.21):

$$Si^{\delta+}\text{-}H^{\delta-} + \text{'O'} \rightarrow SiOH \tag{3.20}$$

$$Si^{\delta+}\text{-}H^{\delta-} + OH^- \rightarrow SiO^- + H_2 \tag{3.21}$$

In acidic and neutral water without a strong oxidant, a hydrogen-passivated silicon surface is inert. However, once areas are oxidized, less strong oxidizing

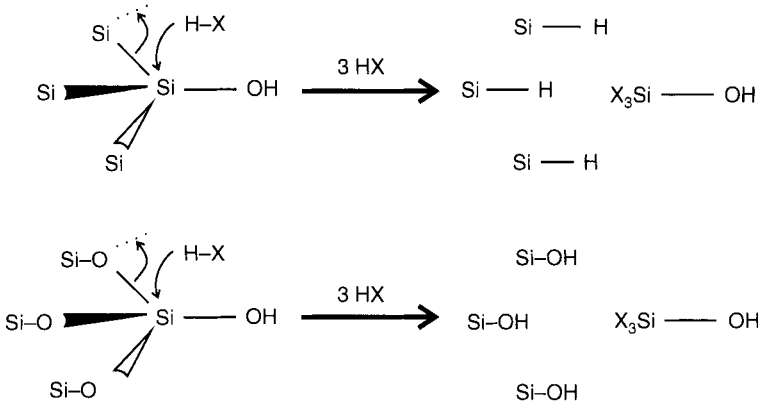


**Figure 3.12.** Similarity between etching of a Si-OH unit out of a Si or $SiO_2$ matrix: $X^- = F^-$ or $OH^-$. Used with permission of the author.

agents can continue the oxidation process. Oxidation of the silicon surface spreads from the initial silicon oxide nuclei and islands to eventually form a continuous oxide layer. The reason is that the OH or F groups bonded to Si are incorporated into a silicon lattice and cause polarization of Si-Si bonds ($Si^{\delta+}$-$Si^{\delta++}$-$X^{\delta-}$). These polarized Si-Si bonds are prone to attack by nucleophiles, such as $OH^-$ and $F^-$. The nucleophilic attack on the polarized Si-Si is the mechanism by which the oxidized silicon is dissolved. Oxidation without dissolution results in a $SiO_2$ layer that contains Si-H and Si-OH groups depending on the oxidation method.

Upon examination, it is not obvious there is an etch selectivity between Si and $SiO_2$. Si must be oxidized to $SiO_2$ before it can be dissolved. Obviously, if no oxidizing agent is present, Si will not be etched while the etching of $SiO_2$ is still possible. Thermodynamics is important for the preferential etching of Si over $SiO_2$. The bond strengths of the reactants differ considerably – Si-Si bond is 327 kJ/mol and Si-O bond is 810 kJ/mol [24–26]. The strengths of the three new bonds formed at the surface (see Figure 3.12) are also different –Si-H bond (<299 kJ/mol) and O-H bonds (428 kJ/mol). The net energy balance strongly favors the etching of Si-OH from a silicon matrix, and this is independent of the etching agent (HF or H-OH).

Etching Si selectively over $SiO_2$ remains a process in need of some tuning [27]. If the oxidation (the surface activation step) is fast with respect to the etching (the dissolution step), not only is the first monolayer of silicon oxidized, but also the second and deeper layers as depicted in Figure 3.13. Surfaces that are oxidized beyond more than one monolayer of silicon dioxide behave like silicon dioxide, and have similar etching rates. An example of such passivation is observed in the cleaning of silicon with APM where an excess of hydrogen peroxide is used. If the hydrogen peroxide is less than a 3 mmol/L threshold, silicon is etched [28].

In the following sections, typical silicon etching solutions are further described. In all cases, an excess of oxidation agent or a lack of etching species will result in the loss of selectivity towards $SiO_2$ and also $Si_3N_4$.

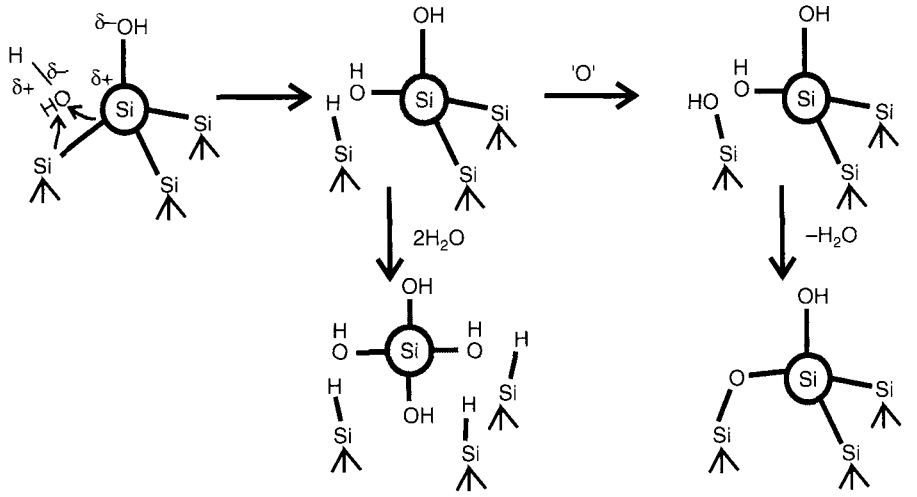


**Figure 3.13.** Etching of a monolayer of SiOH by water and, alternatively, formation of a silicon dioxide layer. Used with permission of the author.

### 3.3.1 Hydrofluoric Acid and Nitric Acid Mixture

Etching silicon with the $HF/HNO_3$ mixture is an isotropic process, and the etching rate is independent of the dopant concentration in silicon. The most frequently used application is the etching of polySi from the back surface of the wafer. In this application, the front of the wafer is covered with a protective coating – usually unpatterned photoresist. The required selectivity of the $HF/HNO_3$ mixture is silicon to photoresist. At room temperature, the photoresist is removed within 5 minutes, which means that the selectivity is poor. For this application, backside spin etchers are ideal in which only one side of the wafer is exposed to the chemical. This also permits solutions with very high rates for bulk silicon etching – ideal for wafer thinning. Applications for the front side are limited to etching large areas where the silicon can be isotropically etched and to removing silicon grains or freckles that remain after wet etching of aluminum containing a few percent (<6%) of silicon. For this latter application, a $HF/HNO_3$ mixture containing a high concentration of fuming nitric acid and a small amount (1–2 wt%) of HF is used. Due to the high concentration of nitric acid, the aluminum is oxide passivated and is not etched. However, the photoresist is removed in this step which can be advantageous.

The overall dissolution equation for silicon is:

$$3\,Si(s) + 4\,HNO_3(aq) + 18\,HF(aq) \rightarrow 3\,H_2SiF_6(aq) + 4\,NO(g) + 8\,H_2O \quad (3.22)$$

The etch mechanism of the $HF/HNO_3$ mixture is described by Schwartz and [29–32]. It involves $HNO_3$ oxidation that is auto-catalyzed by the reaction product nitrous acid, $HNO_2$. Nitrous acid is present in small quantities in the initial etching solution that will oxidize silicon to silicon dioxide and, thereby, form additional nitric oxide:

$$Si + 4\,HNO_2 \rightarrow SiO_2 + 4\,NO(g) + 2\,H_2O \quad (3.23)$$

Nitric oxide will react with nitric acid to reform nitrous acid:

$$2\ NO\ (g) + HNO_3 + H_2O \leftrightarrow 3\ HNO_2 \tag{3.24}$$

Because the solubility of nitrous acid is limited, this reaction can go in reverse liberating gaseous nitric oxide. When silicon wafers are being processed, the concentration of $HNO_2$ will equilibrate to a constant value permitting the net reaction to proceed at a constant rate:

$$3\ Si + 4\ HNO_3 \leftrightarrow 3\ SiO_2 + 4\ NO(g) + 2\ H_2O \tag{3.25}$$

In a used bath, the nitric oxide slowly evaporates reducing the initial etching rate for the next batch. This initiation phenomenon is only critical when the etching time is very short.

The etching rates of $HF/HNO_3$ mixtures depend on the concentration of the component that is present in the lowest concentration. In an excess of $HNO_3$, the etching rate depends on the HF that dissolves the just-oxidized silicon, and the etch process is *dissolution limited*. However, it is found that in these regimes, *diffusion limitations* are reaction rate limiting. These mixtures isotropically etch silicon and polish the wafer surface. If $HNO_3$ is the minor component, then the oxidation products are removed more quickly than they are formed, and the reaction is *oxidation limited*. Additives such as water or acetic acid are used to dilute the solution keeping the reaction products soluble and slowing the etching rate. However, addition of excessive amounts of acetic acid can cause erratic etching rates [23]. Addition of too much water can make the oxidation reaction cease for highly concentrated HF solutions because mixtures with less than 2 M nitric acid have little or no oxidizing power. In Table 3.2 etching rate data are listed, and, in Figure 3.14, a tri-component

**Table 3.2.** Examples of silicon etch mixtures based on $HF/HNO_3$.

| $HNO_3$ Oxidant | HF Etchant | Additives | T (°C) | Silicon <100> and Other Film Etching Rates (μm/min) | Reference |
|---|---|---|---|---|---|
| 21 L | 4 L | | 25 | 13.8; $SiO_2$ mask 8.39 | [33] |
| 7 L | 3 L | | 25 | 127 | [32] |
| 25 L | 1 L | $H_2O$ 25 L | 25 | c-Si 0.36; polySi 0.69; n+ polySi 0.54 | [34] |
| 7 L | 35 L | $H_2O$ 8 L | 25 | 40 | [32] |
| 75 L | 8 L | H-Ac 17 L | 25 | 5 | [35] |
| 3 L | 1 L | H-Ac 10 L | 25 | 3 depends on dopant and concentration | [35] |

HF = 50 wt%; $HNO_3$ = 70 wt%; H-Ac = 100 wt% acetic acid.

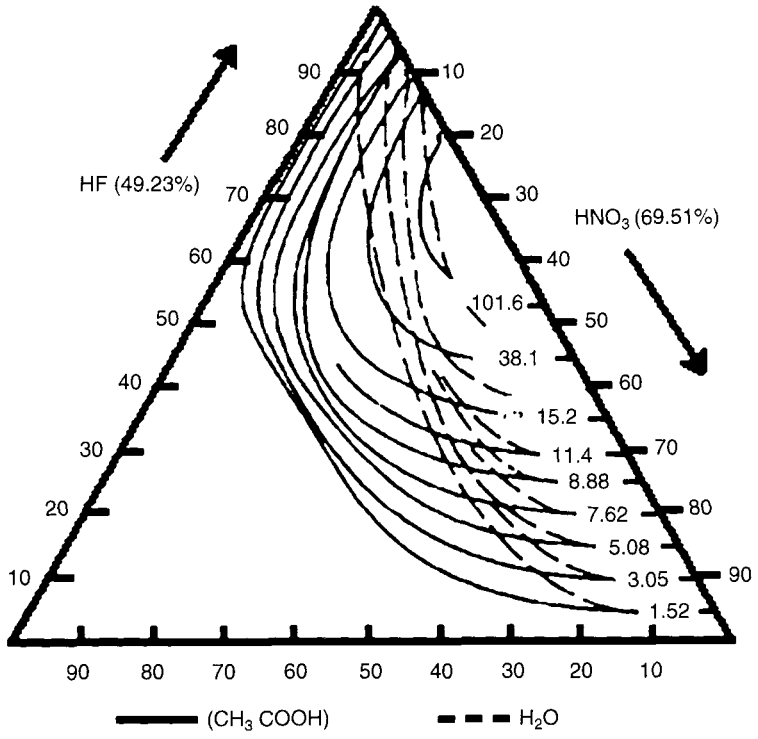


**Figure 3.14.** Isoetch rate curves (μm/min) of a three-component diagram $HNO_3$ (right), HF (left) and acetic acid or water (bottom) [31]. Reproduced with permission of ECS – The Electrochemical Society from Schwartz, B. and Robbins, H., *Journal of the Electrochemical Society.*

diagram with isoetch rate curves is depicted at 23 °C [31]. This figure is used for determining the etching rate of $HF/HNO_3/CH_3COOH$ (H-Ac) or $HF/HNO_3/H_2O$ mixtures. The etching rate of a $HF/HNO_3$ mixture reaches a maximum of 168 μm/min for an $HF/HNO_3$ ratio of 35:65. It should be noted that these etching rate values are not conclusive because of contradicting literature numbers.

The reaction rate in $HF/HNO_3$ can be increased by increasing the temperature or by applying agitation. Since the etching rate strongly depends on the temperature, maintaining a stable temperature of the etching solution is critical. Solutions with high etching rates generate so much heat that non-uniform etching may result. Therefore, the addition of fuming nitric acid (70 wt%) is kept below 65 wt% of the total because, for higher concentrations, the etching rates and heat production can be excessive. Agitation can improve heat transport, but can also enhance diffusion-limited reactions. Etching mixtures with the major component being $HNO_3$ have an activation energy of 15 kJ/mole compared to HF-based etch mixtures with higher activation energies of 40 to 60 kJ/mol. This indicates that the $HNO_3$-based mixtures are diffusion-limited processes while the HF-based are reaction rate-limited. Applying agitation can easily triple the reaction rate of a $HNO_3$-based mixture.

With $HF/HNO_3$ mixtures, selectivity can be obtained with respect to other materials used in semiconductor manufacturing. Silicon dioxide and also $Si_3N_4$

etch slower if less HF is added, but the selectivity is not necessarily improved. Aluminum is etched with small amounts of water present in the etching solution.

### 3.3.2 Potassium Hydroxide and Alcohol Mixtures

Potassium hydroxide, KOH, is one of the compounds used to make alkaline solutions that etch crystalline silicon anisotropically. Typical etching rates are shown in Table 3.3. Other commonly used bases are NaOH, $NH_4OH$, tetramethyl ammonium hydroxide (TMAH), aminoethanol, and hydroxylamine. Potassium hydroxide solutions are used for the removal of monocrystalline or polySi (*e.g.* for wafer thinning). Anisotropy is not required; however, it is desirable that these processes be rapid. Applications that use the anisotropic characteristics of the KOH etch are the etching of markers for e-beam lithography and in micromachining [36]. One of the problems is that organic-based photoresist also dissolves in these solutions requiring silicon dioxide or silicon nitride hard masks to prevent unintended resist removal.

The etching of silicon by KOH is described as a two-step process – a surface activation step and the dissolution of the activated group [38, 39], as depicted in Figure 3.15. A hydroxyl anion attacks the surface silicon thereby forming an intermediate triangular complex with the H and OH bonded to the silicon atom [40, 41]. By the

**Table 3.3.** Anisotropic silicon etch mixtures.

| $H_2O$ Oxidant | KOH Etchant | Additives | T (°C) | Silicon Etching Rates (μm/min) | Reference |
|---|---|---|---|---|---|
| 560 mL | 440 g | | 120 | <111> 0.02, <100> 5.8 <110> 11.7 | [37] |
| 650 mL | 350 g | | 85 | <111> ± 0, <100> 2.2 | [37] |
| 450 mL | 140 g | IPA 52.5 mL | 85 | 0.5 | [37] |
| 633 mL | 234 g | IPA 139 mL | 80 | <111> 0.06, <100> 1.0 [B] dependent | [37] |

IPA= *iso*propyl alcohol

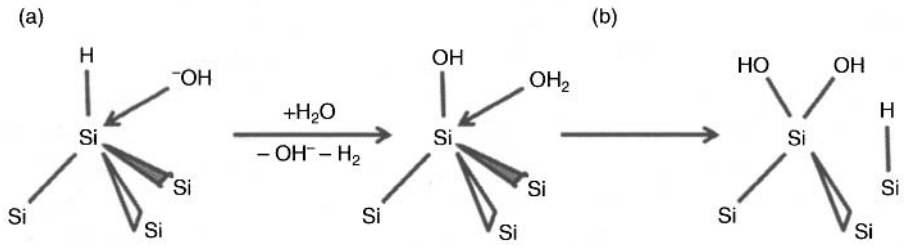


**Figure 3.15.** Two step reaction mechanism of the etching of silicon in KOH: A is the surface activation step where SiH is oxidized to SiOH and B is the first of three nucleophilic substitution reactions where one of three Si-Si bonds are broken. Used with permission of the author.

addition of water, hydrogen is formed, thus, oxidizing the silicon. Alternatively, the electrons that are released in this process can be absorbed into the conduction band of the substrate or another oxidation agent. The followings steps detail the breaking of the silicon-silicon backbone, the detaching of a SiOH group from the surface, and recreating a surface with SiH termination ready for the next etching cycle.

The most common substrate used in IC manufacturing is <100> silicon that has a di-hydride terminated surface. The net equation for the etching reaction of this crystal plane is given in (Eq. 3.26). In the following equations, the specific intermediate reaction steps, as proposed by Allongue *et al.* [39] for the di-hydride terminated surface, have been listed. As the $OH^-$ groups are consumed, the pH of the etch solution will slowly decrease. Since KOH solutions are used to etch bulk silicon, the concentration of the KOH must be high. In Eq. 3.27, the first reaction step of the etching process, the oxidation of Si by $OH^-$, has been generalized, but basically will not differ from what is shown in Figure 3.15. Since the di-hydride was only attached to two silicon atoms, only two Si-Si bonds have to be broken. The initial reaction product is $Si(OH)_3H$ (Eq. 3.29) that will be further oxidized in the solution:

$$Si(s) + 2\,OH^-(aq) + H_2O \rightarrow SiO_3^{2-}(aq) + 2\,H_2(g) \tag{3.26}$$

$$=SiH_2 + H_2O \rightarrow =Si(OH)H + H_2(g) \tag{3.27}$$

$$=Si(OH)H + H_2O \rightarrow -Si(OH)_2H \tag{3.28}$$

$$-Si(OH)_2H + H_2O \rightarrow Si(OH)_3H \tag{3.29}$$

$$Si(OH)_3H + H_2O \rightarrow Si(OH)_4 + H_2\,(g) \tag{3.30}$$

$$Si(OH)_4 + 2\,OH^- \leftrightarrow SiO_3^{2-} + 3H_2O \tag{3.31}$$

The etching of silicon is one of the few examples where it is possible to do a wet anisotropic etch. For example, with KOH solution square holes are etched in a <100> silicon wafer (Figure 3.16). The reason for the shape is that etching along the <100> planes is faster than lateral etching along the <111> planes. Eventually, the etching will stop or slow down when the <111> planes meet at the bottom of the pit.

Thus, the etching rates depend on the crystallographic orientation of the silicon. Experimentally it is found that the etching rate ratios in KOH (22.7 wt%) at 85°C for silicon <110>, <100>, and <111> are roughly 10, 5, and 1 [37]. These experimental ratios partly reflect the atomic packing density which is $2.39 \times 10^{14}$, $3.39 \times 10^{14}$, and $8.95 \times 10^{14}$ atoms/cm$^2$, respectively. Planes with the lowest packing density are expected to etch faster with respect to the depth of Si removed because fewer atoms need to be removed for each layer. For example, in the <111> plane $8.95 \times 10^{14}$ atoms/cm$^2$ must be removed to etch one monolayer while only one quarter of the number of atoms must be removed to etch one monolayer of the <110> plane (see Figure 3.17). Since the oxidation rate of silicon is highest for crystal planes

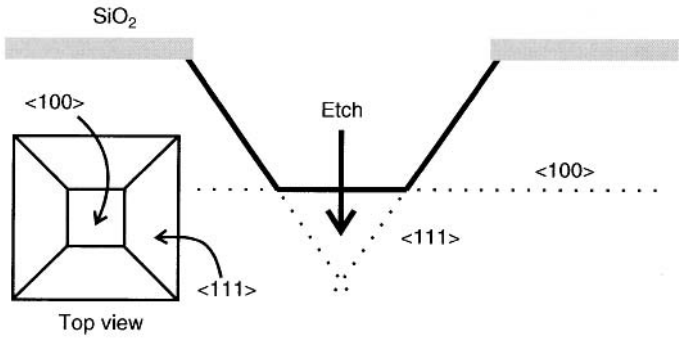


**Figure 3.16.** Etch profile due to anisotropic etch of <100> silicon in KOH (aq). Used with permission of the author.

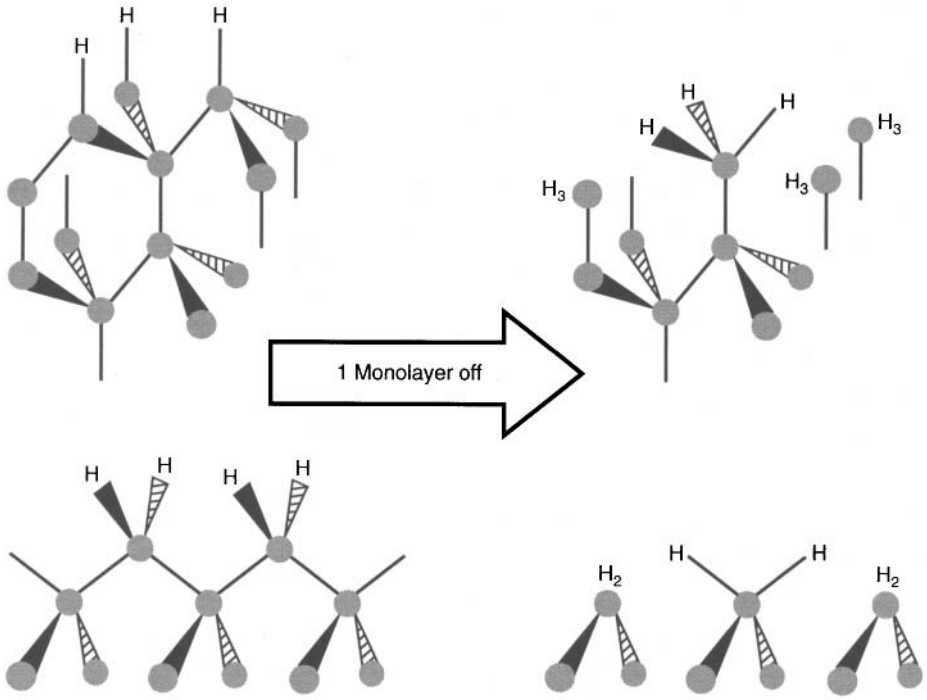


**Figure 3.17.** Etching of the surface layer of silicon: top is Si <111> and bottom is <100> or <110>. Used with permission of the author.

with the highest atom density, and the <111> plane has the lowest etching rate, it can be concluded that this oxidation is not rate determining in the etching process.

The etching rates of the respective silicon crystallographic planes are strongly influenced by the addition of alcohols to the KOH solution [41]. Alcohols decrease the etching rates for all orientations, but not equally. Addition of simple aliphatic mono alcohols (*i.e.* propanol and butanol), regardless of whether the alcohol is primary, secondary, or tertiary, the etching rate is half of the normal etching rate while the <111>/<100> selectivity is doubled with respect to the pure KOH solution. The reason for the different crystal plane selectivity of the alcohols is not clear.

Next Page



Suggestions made in literature [41, 42] is the alcohols (R-OH) reacts with SiOH to form esters, Si-O-R, but are not supported by this data.

The selectivity of KOH solutions between silicon and silicon dioxide is important because $SiO_2$ is a frequent choice for hard mask material. This selectivity can be controlled by modifying the concentration and temperature. In Figure 3.18, the silicon etching rate and $Si/SiO_2$ selectivity for the KOH etch is plotted as a function of concentration of KOH at 70°C. The etching rate is approximately 800 nm/min and does not vary significantly with the concentration. This indicates that the rate determining step in the silicon etching process does not involve the $OH^-$ concentration. However, the etching rate of $SiO_2$ increases at higher KOH concentrations until the $SiO_2$ etch process becomes diffusion limited. From the graph it can be concluded that the best $Si/SiO_2$ selectivity is obtained at concentrations below 20%.

The etching rates of Si and $SiO_2$ depend on the temperature and in both cases it will increase at higher temperatures. In Figure 3.19 the etching rate of <100> silicon in 25 wt% KOH is depicted as a function of temperature. Using an Arrhenius

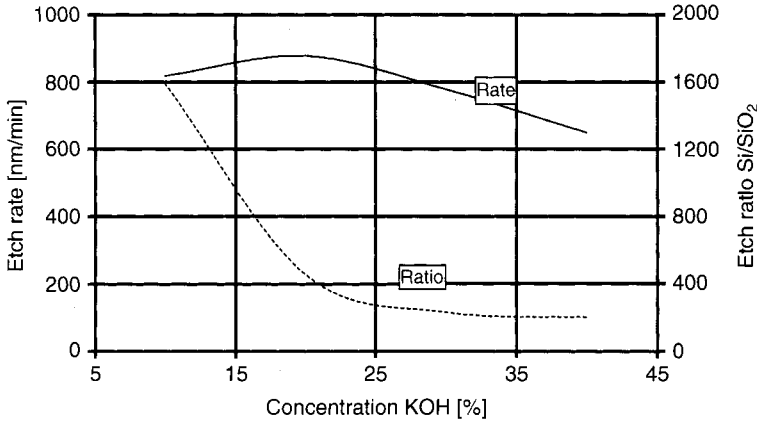


**Figure 3.18.** Etching rate of silicon <100> in KOH at 70°C [43]. Used with permission of A. A. M. van de Vorst (NXP).

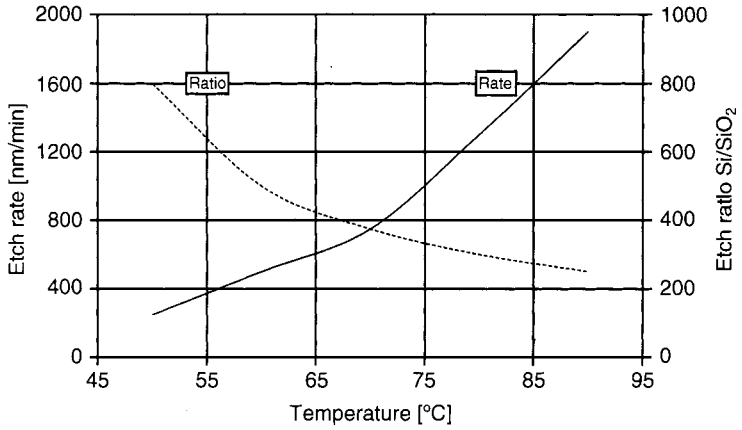


**Figure 3.19.** Etching rate of silicon <100> in 25 wt% KOH [43]. Used with permission of A. A. M. van de Vorst (NXP).

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4

# Surface Phenomena: Rinsing and Drying

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*Abstract*
Rinsing and drying processes are critical to control after the cleaning and etching steps. Rinsing and drying should not adversely affect the cleaned wafer surface. The rinse must completely wet the wafer, and then be efficiently removed from both planar surfaces and features. The chemicals and the cleaning byproducts must be removed leaving no residual layer of water on the surface. Watermarks must be prevented from forming on hydrophobic surfaces by controlling the drying process and minimizing the amount of dissolved silica in the water. Additionally, contaminants must not redeposit on the wafer surface during these processes. This chapter reviews the physics and chemistry of rinsing and drying by discussing Young's wetting equation, surface tension and energy, stiction, and electrostatic charging.

*Keywords:* rinsing, drying, surface charge, surface energy, surface tension, watermarks, water droplet, silica solubility, silicic acid, quick dump rinser, overflow rinser, cascade rinser, spin rinse dryer, Marangoni dryer, stiction

## 4.1 The Surface Phenomena of Rinsing and Drying

The ability to rinse and dry a surface after being exposed to cleaning and etching chemical is critical for the surface conditioning process. Rinsing and drying are challenging because some of the chemicals are viscous and not easily rinsed, others are trapped deep inside high aspect ratio (HAR) features, and still others easily redeposit and leave residues on the surface if not effectively flushed away. This chapter will cover the surface aspects of rinsing and drying expanding on the content of Chapter 1 that introduced and described in detail wetting of hydrophilic or hydrophobic surfaces and high aspect ratio features. Also, together with Chapters 2 and 3, that discussed the cleaning and etching of a silicon surface, this chapter completes the surface aspects of these processes.

This chapter first reviews the basics of rinsing and drying – convection of impurities away from the wafer during the rinsing process and prevention of their re-deposition and then drying the wafer surface without leaving residual

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contamination. Additional topics covered include charging during the rinsing and drying cycles, the formation of watermarks due to dissolution of silica, and methods for limiting the amount of dissolved silica in the rinsing water.

### 4.1.1 Introduction to Surface Phenomena in Rinsing

Water must be used to rinse wafers after exposure to the processing chemicals used in integrated circuit (IC) manufacturing fabs. Quick dump rinsers (QDR), cascade rinses, spray rinsers (also called gravity rinsers), overflow rinsers, and spin rinsers, are all commonly used and commercially available. Some of these rinsing methods can be incorporated with dryers in the same module. Rinses can use deionized water (DIW) or, in some cases a neutralizing chemical, for example, is used after a hydroxylamine-based cleaning process as discussed in Chapter 9. This section will focus on water rinsing. Ultrapure water (UPW) that is deionized (18.2 MΩ-cm), cleaned of bacteria and other organic material is commonly used. In addition, the surface phenomenon of wetting planar surfaces and features, silicon oxide solubility and the formation of watermarks will be discussed in Section 4.2.

Successful rinsing entails:

1. Complete removal of chemical from the wafer surface.
2. Complete removal of chemical from all features on the wafer surface.
3. No residual contamination, such as ionic, metallic, or organic, including silica.
4. Minimal particle adders.
5. Minimal static charge.
6. Minimal use of water.

### 4.1.2 Introduction to Surface Phenomena in Drying

There are many different methods to dry wafers in IC manufacturing. Spin rinse dryers (SRD), vapor driers, hot $N_2$ driers, and surface tension gradient (STG) effect driers are among many commercially available tools and each of these techniques have supporters and detractors. Drying must achieve:

1. Complete removal of water from the surface, features, edges, and touch points.
2. No residual stains, watermarks, or haze.
3. Minimal particle adders.
4. Minimal static charge.

The process must also be rapid, efficient, and low cost. The surface phenomena in drying will be discussed in Section 4.3.

## 4.2 Overview of Rinsing

Rinsing involves three distinct steps to remove the contamination from the water surface. Figure 4.1 depicts these steps:

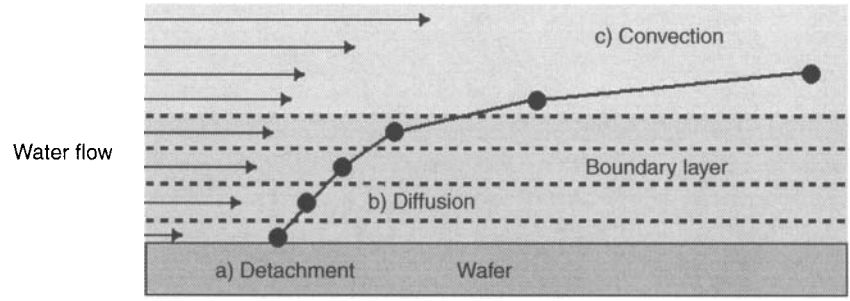


**Figure 4.1.** Schematic of the three steps in efficiently rinsing a planar wafer surface: a) detachment, b) diffusion, and c) convection. Courtesy of FSI International.

1. Detachment – the contamination is physically or chemical removed from the wafer surface and for soluble material, dissolved in the water.
2. Diffusion – the contamination diffuses into the boundary layer – away from the wafer surface but able to reattach or redeposit if the water is evaporated.
3. Convection – the contamination diffuses into the boundary layer and is swept away.

Rinsing efficiency has improved over the years, as has the associated drying step. Overflow rinsing is very good for quenching the cleaning or etching process because the wafers are immediately submerged in the water bath. However, this method is not very good at rapidly reducing the amount of contamination on the wafer because the bath is continuously flowing and DIW change over occurs over a long period of time, thus, the chemicals are not removed quickly from the area surrounding the wafer. This is especially true with viscous chemicals that have high carry-over volumes. Christenson estimated the overflow velocity to be ~1 cm/sec and used ~13 to 20 liter per 200-mm DIW per rinsing step [1, 2].

Christenson also states that the efficiency of rinsing in such a bath is limited by the rate at which contaminants diffuse away from the silicon surface, through the boundary layer, and into the flow stream [1], as depicted in Figure 4.1. Diffusion is the only way chemicals are removed from deep trenches [3] unless agitation is provided. Thinning the boundary layer is possible by megasonic, rapid, or oscillating flow, as discussed in Section 4.2.2. Therefore, rinsing methods that can quickly remove the contamination from the surface by dumping the content or thinning the boundary layer are preferable. The flow velocity over a 200-mm wafer spinning at 100 rpm (rotations per minute) using a single wafer spin dry station is calculated at ~1,000 cm/sec, a substantial improvement over an overflow rinse, and this method uses less DIW. An overview of rinsing techniques is given by Gale *et al.* [4].

## 4.2.1 Wafer Charging

### *4.2.1.1 Charging from Immersion in Water*

The mere action of immersing a wafer in water imparts charge to the surface. Silica surfaces whether from a native, chemical, or thermal oxide acquire a negative charge upon immersion in $H_2O$ [5]. This occurs from the deprotonation of the

terminal silanol groups at pH > 4 [6]. The surface charge is positive on a hydrogen-terminated silicon surface. Endo *et al.* at Osaka University have determined that within a Si-H bond H atoms attract electrons because the electronegativity of the H atom is greater than the Si atom [7] creating the positive charge on the surface.

The positive charge on the hydrophobic H-terminated Si surface in turn attracts negatively charged particles. Since the particles found in DIW are primarily negatively charged, most being silicate particles or metallic contamination, they are attracted to the H-terminated surface. This is the reason particle-free surfaces on hydrophobic wafers after a HF-last cleaning step are so difficult to produce. The chemical environment also influences charge; Chapter 3 discussed the charge on a Si and $SiO_2$ surface with respect to pH.

#### *4.2.1.2 Wafer Charging During Spinning*

Static charge was recognized by Ohmi *et al.* in 1989 as an issue with spin drying of wafers [8]. The batch spin drying process has been shown to generate static electricity between approximately −1.2 to −3.3 kV/cm [8, 9]. Single wafer processes also experience charging of the surface from the drying step and during the chemical cleaning steps. Not only is static charge generated on the wafers, but the carrier and cassette are also charged. Since insulators, such as $SiO_2$, do not have a conductive path, charge builds up on the surface and cannot be dissipated easily in a semiconductor manufacturing environment because of the low humidity and high resistivity water. The charge on the surface of both insulating $SiO_2$ and semiconductor Si is discussed in Chapter 1.

It has long been known that friction between two materials creates static charge [10], and this charge can attract particles onto surfaces [11]. The very act of spinning a material in air imparts charge onto the surface [12]. Figure 4.2 shows the charge build-up for different air flows. Although these flows are very low compared to what a wafer would experience while spinning. This is a good indication that the fast spinning process builds up a higher concentration of positive and negative ions [13]. Halladay *et al.* showed that the faster the spin on a single wafer tool the more charge is accumulated [14]. Because of the charge on the wafers and carrier, particulate matter is attracted to these surfaces. The atmosphere surrounding the wafer has both positively and negatively charged particles. Thus, if the surface of the wafer is negatively charged, the positive particles will be attracted and the negative particles will be repelled. Relative humidity levels of 30–40%, such as those found in a cleanroom are low enough to defeat charge-reducing effects on insulators although this may not be the case for the controlled environment of spin processing systems. Additionally, the use of high resistivity DIW (>18 MΩ-cm) cannot dissipate the charge during the spinning process [14, 15]. Adding a conducting source during rinsing, for example, $CO_2$ sparged DIW, the charge upon spinning decreases [14].

Mitigation of static charge in batch SRD systems has been in place for many years [13]. A deionizer is used to neutralize both positive and negative charges (the predominant charge on oxidized wafers) on the wafer surface [16], and most if not all SRD systems come equipped with deionizers. Results of deionizer neutralization on a SRD have show a reduction of ~2 kV to <0.0.4 kV/cm after implementation [9].

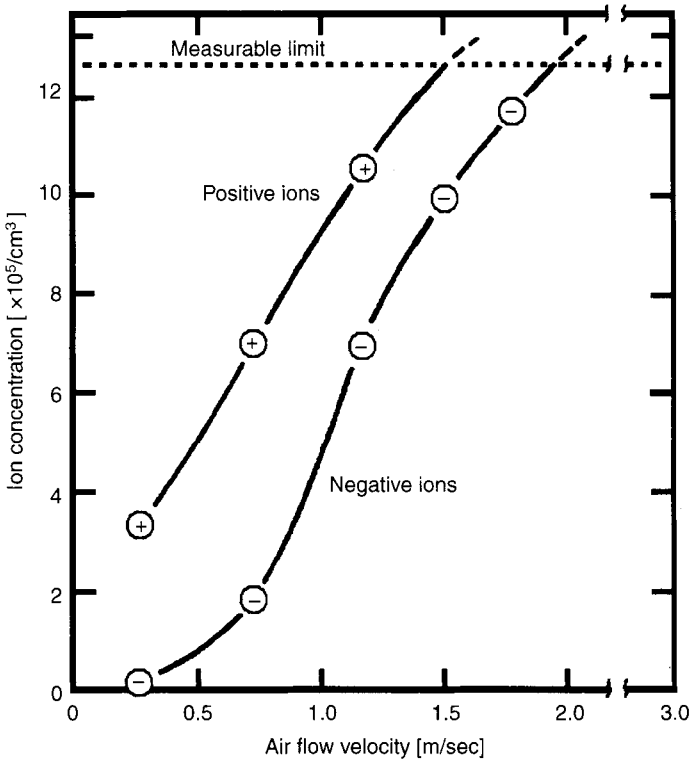


**Figure 4.2** The positive and negative ion concentration *vs.* the air flow velocity [13]. Used with permission of Inaba, H., Sakata, S., Yoshida, T., Okada, T., and Ohmi, T., *IEEE Transactions on Semiconductor Manufacturing*. © 1992 IEEE.

Additionally, other types of charge dissipation are employed – not only on the spin processing tools, but also in the cleanroom [15].

Ohmi found that using an isopropyl alcohol (IPA) vapor drying system, the charge on the wafers is 0 kV. He further found that IPA drying, not the IPA itself, actually dissipates charge caused by chemical processing and rinsing, and after rinsing the charge on the 75-mm wafer was –15 kV [8].

Murali *et al.* have shown wafers have a radial pattern of charge – greater negative charge in the center of the wafers and lesser at the edge [17] using a SRD that spins around a center axis, as measured by surface charge analysis (SCA). The charge build-up is believed to be due to residues, such as dissolved silica, formed during the rinse cycle. Menon *et al.* have shown that the number of particles correlate to the charge on the $SiO_2$ surface [18]. They observed that the greater the charge, the more particles were found on the surface. Yamada *et al.* have also shown that the charge across the wafers caused by single wafer spin processing correlates to the number of particles [19]. Halladay *et al.* [14] and Yamada *et al.* [19] used surface potential measurements to quantify the charge, described in [20].

Figure 4.3 shows the charge on hydrophilic oxidized wafers after QDR and spin dry, and after QDR and SRD, in which the wafer began with a positive potential. The wafer before processing showed little charge difference from the center to the

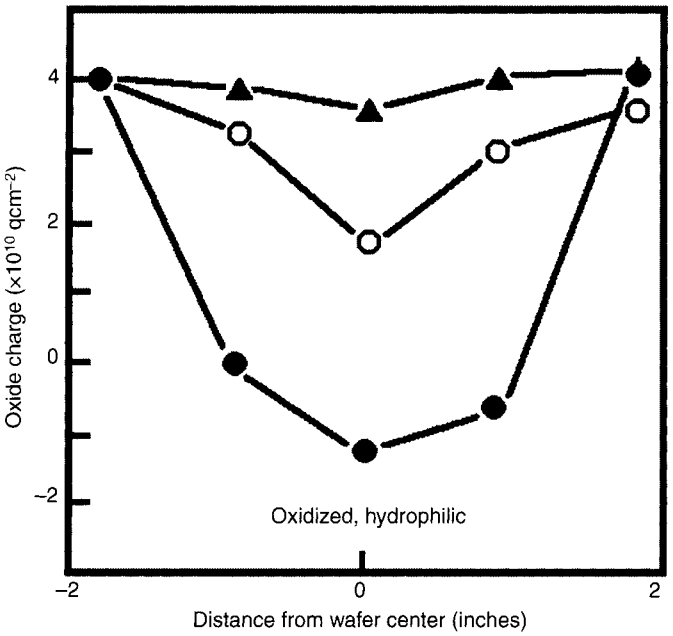


**Figure 4.3.** The charge across the diameter of hydrophilic oxidized wafers △ prior to dump rinse, ○after dump rinse and spin dry, and ●after dump rinse and spin rinse dry [17]. Used with permission of V., Wu, A. T., Chatterjee, A., and Fraser, D. B., *IEEE VLSI Symposium Technical Digest.* © 1990 IEEE.

edge; however, the delta increases with the spin dry, and the combination spin rinse dry greatly increases the negative charge in the center of the wafer [17].

Figure 4.4 compares the charge on a bare silicon wafer to an oxidized wafer after a single wafer megasonic-assisted back surface cleaning step. The bare silicon wafer has very little charge difference across the wafer compared to the oxidized wafer. Additionally, the particle maps associated with the wafers show a somewhat random distribution across the silicon surface while on the oxidized wafer concentric rings with high particle densities were observed. These heterogeneities were attributed to areas with large differences in charge.

## 4.2.2 Wetting a Surface

Complete wetting of a water surface is critical for effective etching, cleaning, and rinsing. Any area not entirely wetted will not undergo the required process. Chapter 1 discusses the surface energy associated with the liquid-solid interfaces associated with wet cleaning. As applied to rinsing, the wetting of a surface is dependent on its hydrophobic or hydrophilic nature as well as its surface energy and the features to be wetted. The surfaces can be planar or with features containing moderate or high aspect ratios.

### *4.2.2.1 Surface Energy and Surface Tension*

Liquid-solid interactions are governed by properties such as surface energy and surface tension. Surface (free) energy is the energy of a material surface that is in

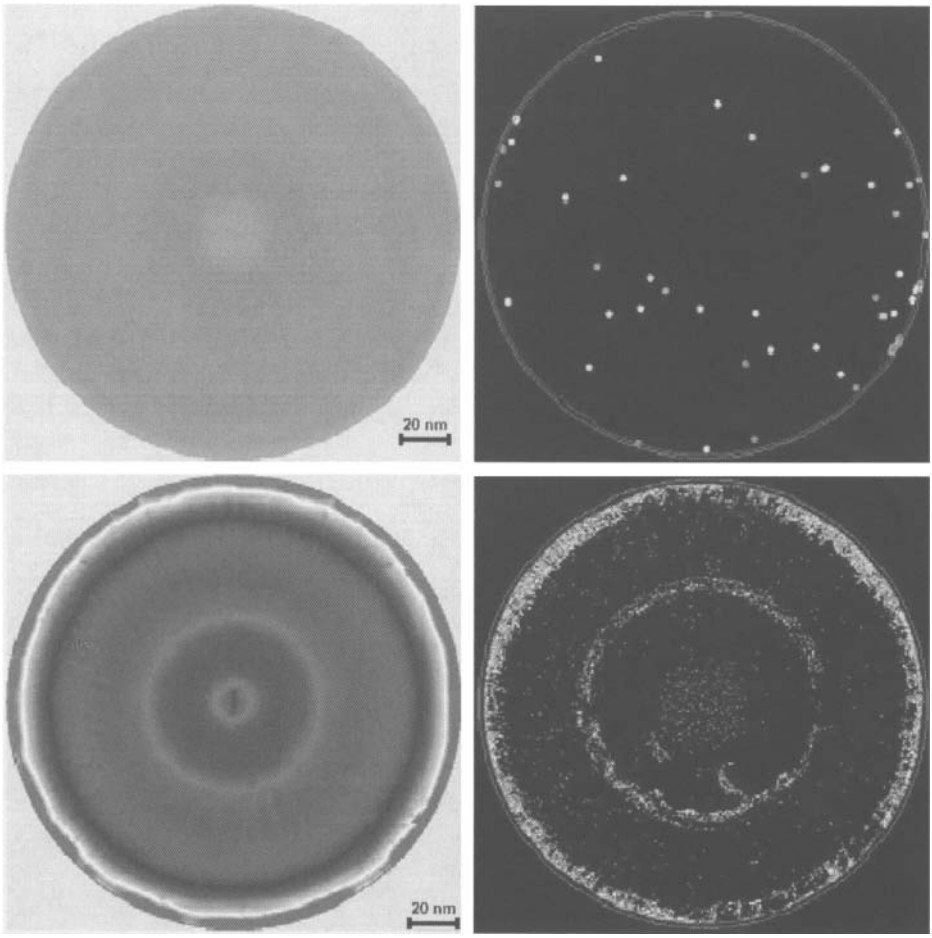


**Figure 4.4.** The charge and the particle maps of 300-mm wafers for a) silicon surface and b) oxidized surface [19]. Used with permission of QCept.

excess of the energy of its bulk. While numerically equivalent, surface tension is defined as the work required to create additional area on a given surface. Surface tension ($\gamma$) generally decreases with temperature:

$$\frac{d\gamma}{dT} = -\frac{\Delta S}{A} \tag{4.1}$$

because excess entropy ($\Delta S$) will increase for a given surface area ($A$) as temperature ($T$) increases. Eq. 4.1 shows that liquid surface tension decreases as a function of temperature; consequently, the work required to remove a droplet will decrease at elevated temperatures. In a three phase system (*e.g.* liquid droplet on a solid surface), the behavior of the liquid will be determined by the *adhesion* of the liquid to the solid and the *cohesion* within the liquid.

It is this balance between the cohesive tendency of the liquid and the adhesive interactions of the liquid and the solid that determine wetting. When the adhesive

force between the liquid and solid is more than the cohesive force within the liquid, the liquid will wet the surface. Young's equation describes this interplay of forces:

$$\gamma_{sv} = \gamma_{sl} + \gamma_{lv} cos\theta \tag{4.2}$$

where $\gamma_{sv}$, $\gamma_{sl}$, and $\gamma_{lv}$ are the solid, solid-liquid interfacial, and the liquid surface free energies and $\theta$ is the contact angle between the liquid and the solid. When there is strong adhesion and weak cohesion, the liquid wets the surface (lyophilic), and the contact angle is low. If there is limited adhesion and strong cohesion, then the liquid will not wet the surface (lyophobic), and the contact angle is high.

The work required to remove a liquid droplet from a solid surface ($W_{sl}$) can be represented as:

$$W_{sl} = \gamma_{lv} + \gamma_{lv} cos\theta \tag{4.3}$$

In this text, surface tension will be used interchangeably with surface energy. However, Adamson notes that ..."surface tension is a definite and accurately measurable property of the interface between two *fluid* phases" (emphasis added) [21]. Figure 4.5 depicts the contact angle and the associated surface tension between the interfaces; solid, liquid, and vapor.

### 4.2.2.2 *Wetting and Rinsing Small Features*

Wetting small features, including HAR features, is governed by capillary action, which is the adhesion of the liquid to the surface from the differences in surface energy. The fundamental properties and the force equations that govern feature wetting were addressed by Mastrangelo when evaluating forces and stresses encountered in fabricating micro-machined structures [22] and discussed in more detail in Section 4.3-5.

When surfaces are wetted with greater adhesion forces than cohesion, the wetting between two lines produces a liquid surface that is concave, Figure 4.6a. When the cohesive forces are greater than the adhesive forces, the liquid surface is convex, Figure 4.2-6b. This phenomenon was first investigated in 1916 by

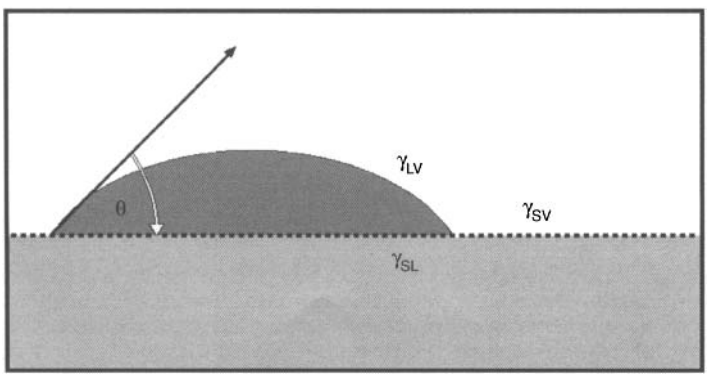


**Figure 4.5.** Depiction of a liquid droplet on a solid surface. The contact angle of the droplet is shown in relationship to the surface energies of the materials. Used with permission of the authors.

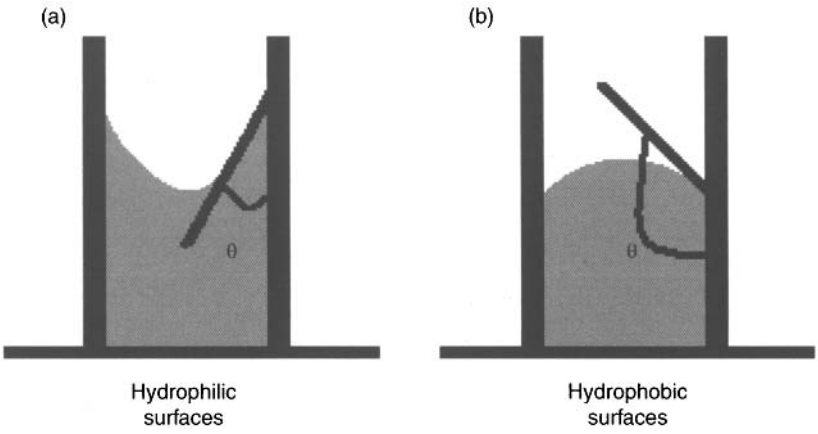


**Figure 4.6.** Depiction of a liquid droplet on a solid surface; a) hydrophilic surfaces with contact angle <90° and b) hydrophobic surface with contact angle >90°. The contact angle of the droplet is shown in relationship to the surface energies of the materials. Used with permission of the authors.

Smoluchowski [23]. Applying pressure or other physical means to assist in removing the liquid through the capillary (*i.e.* a contact, capacitor, via, trench feature) provides additional force on the liquid and allows it to penetrate into the feature and mix effectively by thinning the boundary layer.

The ability to efficiently get DIW into the features is critical to dissolve the residual chemicals and byproducts of the cleaning or etching step and then to remove them from the surface to prevent them from re-depositing. Chapter 1 thoroughly discusses the ability of water to penetrate into HAR features including hydrophobically-walled trenches. Diffusion models for chemical transport into and, for rinsing, out of deep trenches by Nakao *et al.* have shown that within a few seconds of rinsing a trench with an aspect ratio of 8:1 the chemical is removed to ppm levels. However, performance is dependent on the rinsing velocity and the temperature of the rinsing water [24]. To remove the impurities, water must first diffuse into the trench, and then the flow can assist in agitating the surface of the trench to remove the impurity. Higher flow velocities cause faster dilution of the chemicals. Higher temperatures increase the diffusion because hot water has greater diffusivity than cold water. In this experiment, the temperature of the rinse water was ~50°C. High temperatures for rinsing are used for sulfuric acid/hydrogen peroxide mixture (SPM) to remove sulfates on the surface and can also assist in removing chemicals from between the features. To more effectively remove contaminants, studies by Busnaina suggest that oscillating water flow over deep structures can remove ions from the chemical carry-over better than a laminar flow rinse [25]. Figure 4.7 shows the relative concentration of a chemical solution at the bottom of a trench and the decrease of the concentration as the rinse time progresses. Various flow velocities over the trench are shown including 0 m/sec, where the rate of removal of the contamination is diffusion limited.

### *4.2.2.3 Wetting Rough Surfaces*

Macro-wetting (the visible wetting of a surface measured by contact angle) has often been explained by the use of Young's equation. The field of surface science has

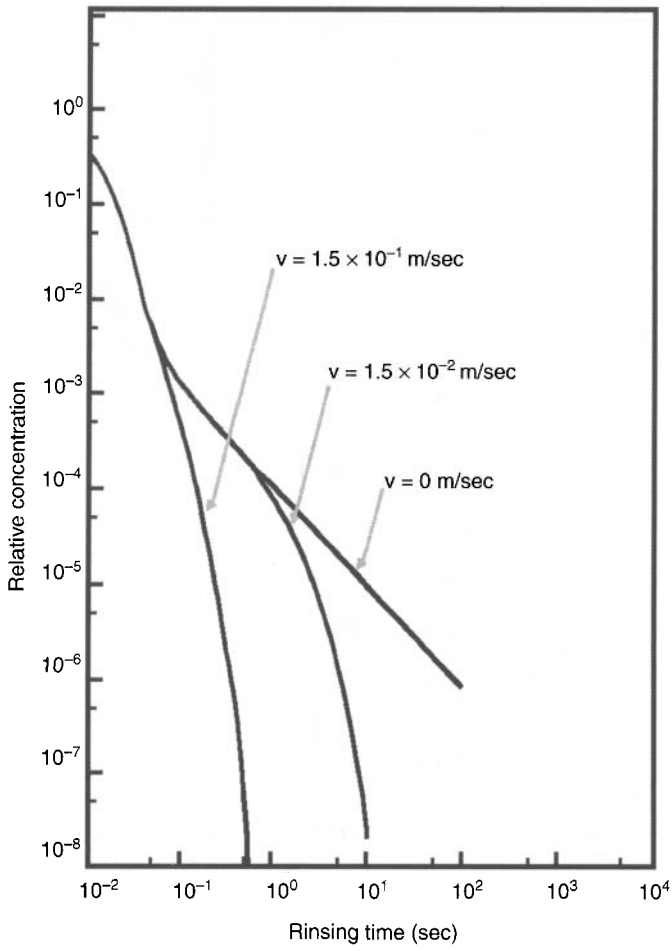


**Figure 4.7.** Concentrations vs. the rinsing time for a chemical solution at the bottom of a trench for various flow velocities [24]. The diffusion coefficient is $1.0 \times 10^{-9}$ m$^2$/sec. Used with permission Reproduced with permission of ECS – The Electrochemical Society from Nakao, I., Umimoto, H., Odanaka, S., Ohzone, T., and Esaki, H., *The Journal of the Electrochemical Society.*

struggled and continues to struggle to explain wetting on rough or patterned surfaces using the Wenzel, Cassie-Baxter, or hybrid modifications of Young's equation. Papers emerge on this debate almost routinely [26, 27] despite the fact that Wenzel [28] and Cassie-Baxter [29] published their work in the first half of the 20th century.

The Wenzel equation:

$$\cos\theta^W = r \cdot \cos\theta^Y \tag{4.4}$$

is the simplest treatment for a surface that is not inherently smooth. In this treatment, the observed "Wenzel" contact angle ($\theta^W$) is related to the true contract angle or "Young" contact angle ($\theta^Y$ is the angle measured if the surfaces were perfectly smooth) corrected by a roughness factor. The factor $r$ refers to the ratio of surface area of the rough area to that of the corresponding projected flat surface ($r \geq 1$). Note that the Wenzel treatment, shown in Figure 4.8b, depicts the rough surface completely wetted by liquid.

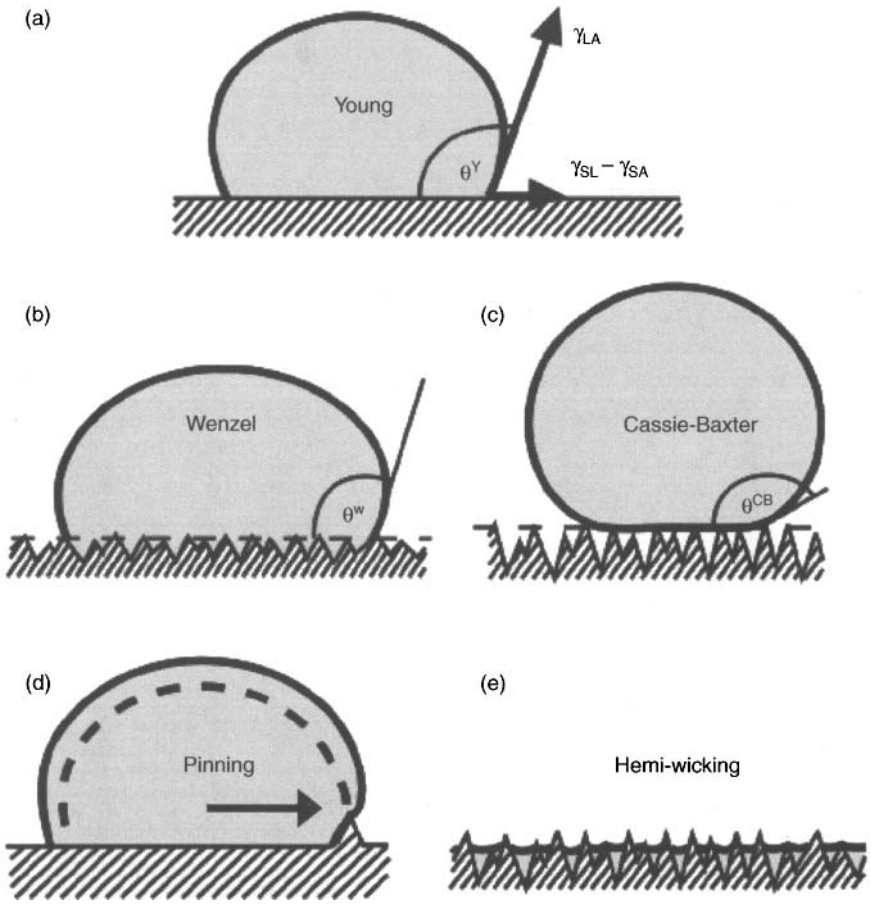


**Figure 4.8.** Graphic showing the physical differences as related to various theories of wetting [30]. Reprinted with permission from *Langmuir*, 24(10):5411 (2008). Copyright 2008, American Chemical Society. Note that the Spori *et al.* [30] employ different notation for the respective surface energies than used in Eqs. 4.2, 4.3 and Figure 4.5 (using *A* for ambient rather than *V* for vapor).

Based on the Wenzel equation, surface roughness tends to move the contact angle of rough surfaces away from 90°. Thus a hydrophobic surface ($\theta^Y > 90°$) is expected to become more hydrophobic when roughness is introduced, and a hydrophilic surface ($\theta^Y < 90°$) is expected to become more hydrophilic with increasing roughness.

In contrast to the Wenzel treatment, the Cassie-Baxter interpretation adds more factors associated with the physical properties of the surface. Wenzel assumes the surface is inherently homogeneous. Cassie-Baxter deals with inhomogeneous or "patchy" surfaces. In this model, the "open" area of the inhomogeneous surface is filled with air. This is graphically shown in Figure 4.8c, and described by the more complex formulae, Equation 4.5 [31]:

$$\cos\theta^{CB} = f_1 \cdot \cos\theta^Y - f_2 \tag{4.5}$$

where, $f_1$ is the fraction of the wetted surface represented by the underlying substrate and $f_2$ is the fraction of "open" area, or for simplicity, imbibed air.

Unfortunately, the literature discussing Wenzel and Cassie-Baxter wetting is typically limited to what would still be considered as "macro" domains with respect to nanoelectronics applications. Nevertheless, complete wetting of all surfaces: rough or smooth, hydrophilic or hydrophobic is critical for removing contamination from the wafer.

### 4.2.3 Silica in Water

Silicon is one of the most abundant elements on the earth, second only to oxygen, thus quartz, $SiO_2$, is the most abundant mineral on earth. Although $SiO_2$ is the general chemical representative of any silica material, varying structures and molecules all claim this formula including the silicon oxide film that is grown on the surface of a wafer by thermal or chemical reactions. Chemical oxides and deposited oxides, sometimes represented as $SiO_x$, are different – they are non-stoichiometric, less dense, and have more dangling bonds than thermal oxide. A good review of silica is given in [32]. General properties of $SiO_2$ are given in Table 4.1.

One of the properties that make $SiO_2$ a desirable material in IC manufacturing is that it is an insulator. Due to its stability with respect to temperature and with other materials used in device manufacturing, $SiO_2$ and other silicates are ubiquitous and used in almost every layer in the IC manufacturing process. Therefore successfully cleaning and drying of this material is critical for optimum device performance.

The solubility of silicon dioxide ($SiO_2$) in water can be described by the following equilibrium reaction:

$$SiO_2(s) + 2\,H_2O \leftrightarrow H_4SiO_4(s) \tag{4.6}$$

**Table 4.1.** Properties of silicon dioxide at 25°C and 1 atm.

| **Property $SiO_2$** | **Value** |
|---|---|
| Specific Gravity | 2.0–2.3 g/cm$^3$ |
| Base Unit Structure | Tetrahedral |
| Crystallinity | Amorphous |
| Hardness | 7 on Mohr's Scale |
| Refractive Index | 1.46 |
| Dielectric Constant | 3.9 |
| Thermal Expansion Coefficient | $5.6 \times 10^{-7}$ K$^{-1}$ |
| Thermal Conductivity | $3.2 \times 10^{-3}$ Wcm$^{-1}$K$^{-1}$ |
| Solubility in $H_2O$ | 0.113–0.12 g/L (114–115 ppm) |

In which $H_4SiO_4$, ortho silicic acid (also called mono silicic acid) can also be represented as $Si(OH)_4$, is a weak acid that can be described as being in equilibrium with water:

$$H_4SiO_4(s) + H_2O \leftrightarrow H_3SiO_4^-(aq) + H_3O^+ \tag{4.7}$$

In general silicic acid can be represented as:

$$[SiO_x(OH)_{4-2x}]_n \tag{4.8}$$

with one of the compounds being $H_2SiO_3$, which is considered to be the soluble form prior to precipitation:

$$H_2SiO_3(aq) + H_2O \leftrightarrow HSiO_3^-(aq) + H_3O^+ \tag{4.9}$$

When exposed to heat, silicic acid can polymerize forming chains of Si-O-Si bonds while releasing $H_2O$ and leading to the formation of silica. Upon dehydration, the $H_2SiO_3$ begins to form into a gelatinous mass.

The solubility of silica in water has been studied by many researchers [33] for a variety of reasons such as: silica dissolution for creation of geological formations [34, 35], silica in seawater [36], and silica in the human body [37, 38]. A summary of silica solubility is presented in [39]. Figure 4.9 shows the solubility of silica in water at neutral pH at various temperatures. At typical rinsing temperatures, the solubility of silica is approximately 0.12–0.13 g/liter. The data points graphed are collected from various researchers and compiled by Alexander *et al.* [39].

The solubility equations for the dissolution of amorphous silica or quartz in water to form $H_4SiO_4$ are given as [40]:

$$\log K_{silica} = -8.476 - (485.24 \times T^{-1}) - (2.268 \times 10^{-6} \times T^2) + (3.068 \times \log T) \tag{4.10}$$

$$\log K_{quartz} = -34.188 + (197.47 \times T^{-1}) - (5.851 \times 10^{-6} \times T^2) + (12.245 \times \log T) \tag{4.11}$$

The heat of solution for the dissolution of amorphous silica, $\Delta H$, is 3.35 kcal/mole [41] indicating it is an endothermic reaction.

At pH values different than that of neutral water, the solubility of silica is not greatly affected between a pH of 1 and 9; however, solubility rapidly increases at pH values over 9, where etching of silicon dioxide takes place [42]. Etching of the silicon in basic media is discussed in Chapter 3.

The dissolved silica can redeposit and form watermarks on a hydrophobic H-terminated silicon surface, as discussed in Section 4.3.2.

#### *4.2.3.1 Oxidation of Silicon in Water*

Oxide growth on Si surfaces, both (100) and (111), in DIW requires the combination of water and oxygen [43]. Dissolved oxygen ($O_2$) in the water can cause dissolution and etching of the silicon. This is exhibited by surface roughening and pitting

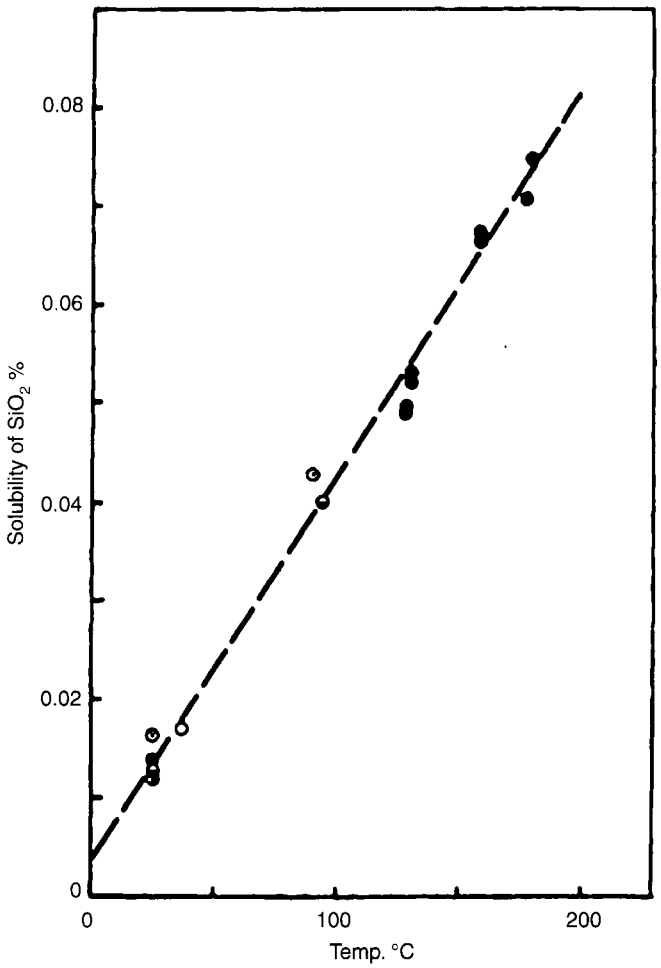


**Figure 4.9.** The solubility of amorphous silica, wt%, in neutral pH water at atmospheric pressure for various temperatures [39]. Reprinted with permission from Alexander, G. B., Heston, W. M., and Iler, R. K., *Journal of Physical Chemistry*, 58(6):453. Copyright 1954 American Chemical Society.

of the crystal structure. Oxygen in other cleaning and etching solutions, such as hydrofluoric acid (HF) [44], also can cause etching and pitting.

Researchers have undertaken studies using high temperatures for non-semiconductor applications and have found that temperature affects the silica solubility [45]. They have also shown that pH affects the etching rate of silica [42]. Initial research on dissolved silica related to watermarks has shown that $O_2$ dissolved in water increases the amount of precipitated silica yielding watermarks, especially on HF-last, hydrogen-terminated silicon [46]. Kanaya *et al.* investigated etching of silicon in low concentrations (5 ppm) of oxygen in water and found that facets appeared after rinsing for a long period of time (20–45 hr). However, this extended rinse time would never be used in production, but is a good indication that oxidation in water with low $O_2$ content is exceedingly slow [47]. A quick dip, such as that experienced with a 5 minute QDR in room temperature DIW does not cause excessive etching, it is enough to dissolve silica.

Miya *et al.* found that spinning the wafer in an ambient environment increased the concentration of oxygen [48]. Additional research was performed investigating the effect of degassing the water to remove the dissolved oxygen through the addition of $N_2$ or $CO_2$ [49]. They found that $N_2$ addition, which also decreased the dissolved $O_2$ concentration and, consequently, suppressed the amount of dissolved silica. Additionally, when they augmented the $N_2$-bubbled water with HCl to acidify the solution, the dissolved silica concentration was further suppressed. Figure 4.10 shows the increased solubility of silica as a function of pH for $N_2$-bubbled water and facility-supplied water that is high in dissolved $O_2$.

Conversely, for wafers with surface oxide on Si (111), dipping into a hot water (~80°C) solution with low dissolved oxygen concentrations (0.004 to 4 ppm) actually hydrogenates the surface removing the hydroxyl groups after 1 hr immersion [50, 51].

### 4.2.3.2 *Precipitation of Silica in Water*

Watermarks form because the silica in the processing solution precipitates onto the surface of the wafer. The amount of silica that is soluble in water is based on the pH, pressure, temperature, and components in the water, such as dissolved gases or organic compounds. The solubility product for a salt or the equilibrium constant ($K_{sp}$) for simple dissolution gives the maximum quantity of a chemical that can be dissolved in water and remain in solution without precipitating. Once water is saturated with the chemical, it will not precipitate out of the water and no more material will dissolve. A silicon wafer immersed in water will dissolve silicon or silicon dioxide at a very slow rate. However, reaction with the water at high pH or with additives may affect the dissolution rate. The addition of organic

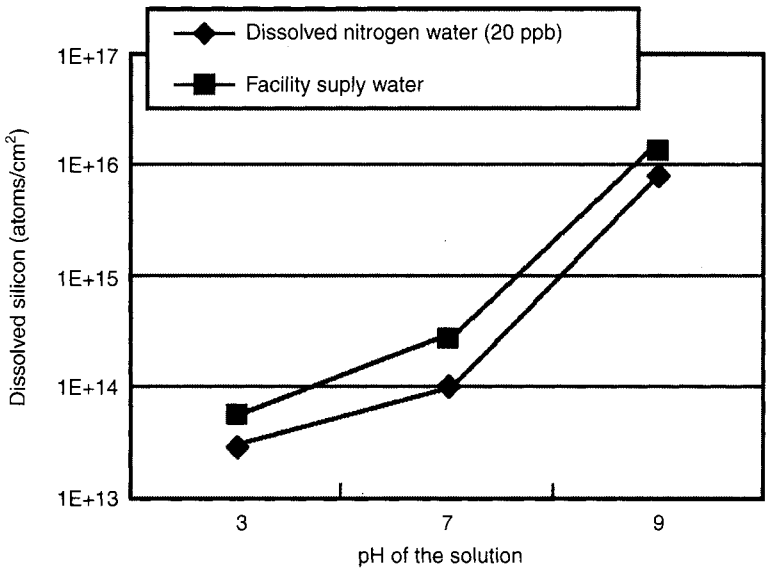


**Figure 4.10.** The solubility of silicon in water with respect to the pH and the gases dissolved in the water [49]. Used with permission from DNS.

compounds, primarily organic acids with a pH close to 7, was found to increase the solubility of silica in water [52].

## 4.3 Overview of Drying

Drying of wafers can be independent of the rinsing step or can be an integrated process. For example, between chemical baths, a QDR is used before going to the next chemical bath. While at the end of the process, a SDR or single wafer process module initiates with a spin rinse step at a slower spin rate than the drying step, then ramps to a higher spin rate with a $N_2$, usually hot, dry step. A Marangoni dryer can have an integrated overflow rinser or QDR after the rinsing the bath that can be filled with water, the IPA condensed, and subsequently drained.

Removing water can occur by various methods – the water can be evaporated, it can be spun off the wafer at high velocity, and it can be displaced by another fluid with a lower surface tension. For spin drying, the residual water remaining on the surface is affected by the radial velocity – the higher the spin speed the more efficient the removal of water, especially droplets from hydrophobic surfaces. The drain speed of the water from an immersion STG dryer or the meniscus movement from a radial spinning STG dryer is key to removing the water without leaving watermarks and completely drying HAR features. No matter what the drying process, to be effective it should accomplish the following:

1. Removing the bulk water off the wafer surface.
2. Remove residual wafer from the contact points on the wafer.
3. Removing residual water from the features.
4. Drying the remaining water layer from the hydrophilic areas that are hydrogen bonded.

This section will discuss the various phenomena in drying.

### 4.3.1 The Chemistry and Physics of Watermarks

Watermarks are the bane of rinsing and drying. Even with the best drying techniques, if not fully optimized, watermarks and stains can remain on the wafer surface sometimes causing simple cosmetic issues if the watermark is in a non-functioning area of the device or causing catastrophic failures due to problems with adhesion of the subsequent layers and gate oxide integrity issues, for example. To eliminate these problems, procedures such as Marangoni drying [53] and proper rinsing by keeping the wafers wet until the drying step have been implemented. This section discusses the formation and mitigation of watermarks caused by silica deposition.

#### *4.3.1.1 Watermarks Formation*

A wafer frequently experiences wet cleaning processes and at each of these steps if must be free of defects, including watermarks. In 1988 Matsuzaki and coworkers

at Hitachi noticed that their wafers had watermarks despite a high water removal rate from the surface of the wafer. They attributed these types of watermarks to organic material [54]. However, typical UPW used for rinsing has very low levels of organic contamination – total organic contamination (TOC) of less than 1 ppb and low bacteria counts [55]. Further investigation by Watanabe *et al.* showed that watermarks on hydrophobic silicon and polycrystalline silicon (polySi) surfaces were composed of precipitated silica [46]. Watanabe also postulated the mechanism of formation of the watermarks. As depicted in Figure 4.11, dissolved silica in a water droplet, once dried, is the source of the watermark. Furthermore, the researchers found that for HF-last cleaned surfaces, the generation of watermarks was dependent on the oxygen content of the water – higher $O_2$ concentrations increase the likelihood of watermark formation.

Watermarks are found in a variety of shapes and sizes. Watermarks can be caused by a droplet of water left over on the surface because the droplet was not removed or because of an inadvertent splash. Water beads with a high contact angle on a hydrophobic surface and can even nucleate at high $H_2O$ vapor pressures in $N_2$ atmospheres [56]. The contact angle is dependent on the surface energy (discussed in Chapter 1 and Section 4.2-2) and the surface roughness. Small water droplets on hydrophobic surfaces are not easily removed. In combination with silicon dissolution, hydrophobic surfaces are the most prone to watermarks.

Figure 4.12 shows a wide range of watermarks formed by various processes. Watermarks caused by SRD are usually spider web-like, probably caused by the

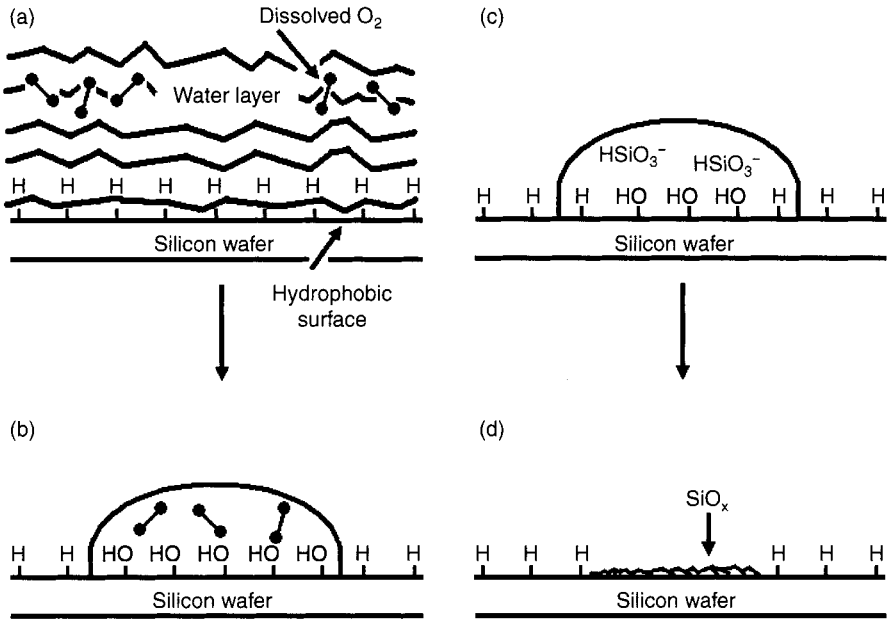


**Figure 4.11.** Schematic of the formation of watermarks on a hydrophobic surface by leaving spots of residual water; a) dissolution of $O_2$ in the rinsing water, b) causes oxidation of the silicon surface shown in the water droplet left on the wafer after drying c) that allows the dissolution of silica into the oxidized silicon into the water, and d) complete drying of the droplet and the formation of the watermark. Used with permission of the author.

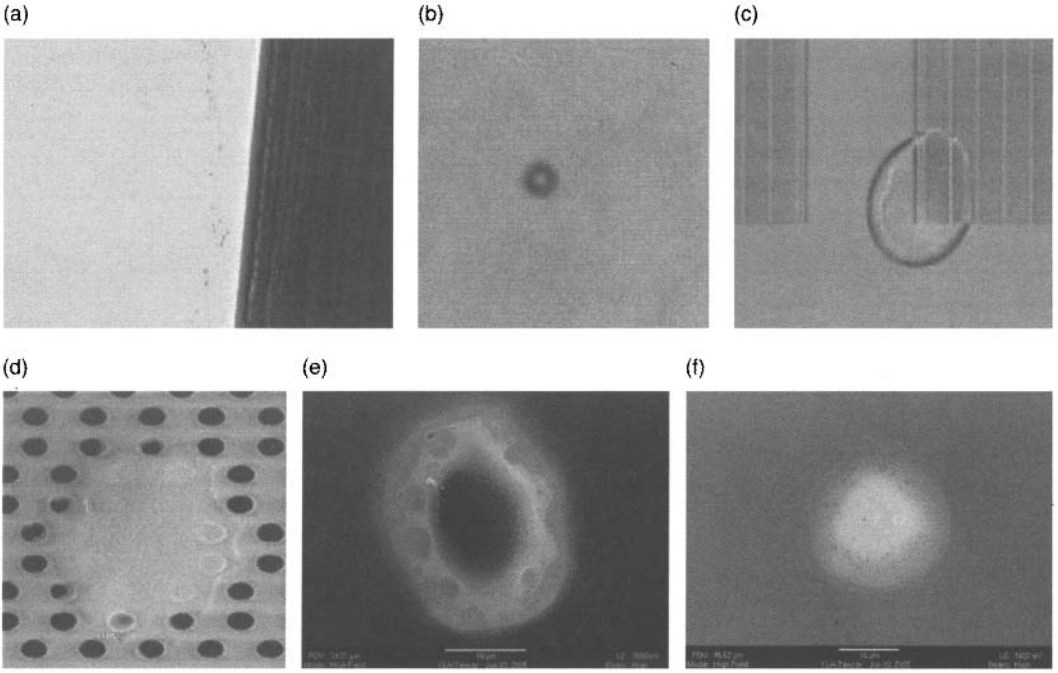


**Figure 4.12.** Various examples of watermarks; microscope photos of a) spider web-like watermark on the edge of a blanket silicon wafer after SRD, b) round symmetrical watermark on oxide wafer after Marangoni drying probably from a bubble or droplet from a splash and c) round watermark on the edge of a patterned feature; scanning electron microscope (SEM) images of d) 3-μm diameter watermark on contact pattern after single wafer STG drying, probably caused by back-splash, and e) 20–30-μm diameter silica watermark on blanket silicon surface and f) 20-μm diameter watermark on copper. a) and b) Used with permission of the author. c) Courtesy of FSI International. d) Used with permission of DNS. e) and f) Used with permission of Yehiel Gotkis, KLA-Tencor.

spreading out and then drying of the water droplet while spinning. Discreet spots, both symmetrical and asymmetrical, are thought to be caused by the evaporation of a water droplet leaving behind the dissolved silica residue. A great deal of research has been conducted, not only to understand watermark formation, but how to mitigate them. Namba and coworkers have shown that evaporation of a water droplet forms very distinct watermarks depending on the concentration of HF in the droplet [57]. In cases with a high amount of HF (>$10^5$ ppm), $H_2SiF_6$ is formed from the reaction of the HF with the $H_2SiO_3$ in the droplet as observed with energy dispersive X-ray spectroscopy (EDS) analysis. For very low concentrations of HF (<0.5 ppm), the watermark is primarily silicon with small amounts of oxygen. As the HF concentration increases to $10^5$ ppm, the watermark material contains more oxygen. The appearance of the watermarks can differ, based on the HF concentration in the rinsing water – a low HF concentration watermark is planar Figure 4.12d while the mid HF concentration is rough and more solid in appearance, such as Figure 4.12b and e.

The ambient environment around the wafer, the wafer's surface, and the drying method are very important. Most, if not all, watermarks are caused by the drying

process. The Marangoni dryer that uses the surface tension gradient effect to remove the water from the wafers, typically with IPA as the lower surface tension solution compared to water is discussed in Chapter 1. Researchers at Samsung have investigated the effect of the IPA vapor pressure on the single wafer drying efficiency [58]. They found the environment with single wafer drying is not as well controlled as with batch water drying and that the environment immediately above the wafer surface must be well controlled to prevent any undesirable consequences of the spin dry process. Kurumoto and coworkers have shown that an $N_2$ environment over the wafers to reduce the amount of dissolved $O_2$ in the water is also important for prevention of watermarks during single wafer IPA drying [59]. However, their observations and conclusions matched the results of Namba [57] – the HF concentration of the water has the largest effect on the formation of watermarks on hydrophobic silicon due to the dissolved silica in the water as shown in Figure 4.11.

#### *4.3.1.2 Watermarks on Wafers Caused by Cleaning*

By the late 1990's the IC industry started to understand the source of the watermarks and the effects on IC devices. In 1995 Park and Pas did a thorough study of the formation of watermarks caused by drying processes [60]. They studied patterned wafers that were hydrophilic, hydrophobic, and a combination of hydrophilic and hydrophobic surface states and determined that only the hydrophobic wafers showed a dependence on exposure time to air before drying when using spin drying validating the results of Watanabe. These wafers did not show watermarks when properly dried with an IPA vapor dry. The hydrophilic wafers, such as those with a thick (>20 Å) thermal oxide, no matter what type of drying was performed, spin dry or IPA vapor dry, were not prone to watermarks. However, the combination hydrophilic and hydrophobic wafers showed watermark formation only on the hydrophobic sites – with both drying techniques. The character of the watermarks was different – the vapor dryer yielded small round spots a few microns in diameter while the spin dryer yielded larger round spots tens of microns in diameter. A previous study on unpatterned wafers undertaken by Park showed similar results [61].

Gate oxide integrity (GOI) was affected by the presence of watermarks leading to differences in gate oxide breakdown voltage of fabricated capacitors [62]. Other researchers studied the formation of watermarks and found that wafers cleaned with HF-last processing using megasonics in the rinse step yielded a high density of watermarks [63]. With no megasonic energy applied in the rinse step, even with hydrophobic wafers, no watermarks were found. They found that watermarks did not affect the GOI of 58-Å thick oxide; however, this is a very thick oxide for current devices.

Watermarks are especially apparent after a deposition step that decorates the region where the stains occur. Nagai studied the formation on silicon wafers prior to polySi deposition and found that more watermarks formed on rougher surfaces [64]. The watermarks on these rougher surfaces were 100–300 nm in diameter. Based on these results, the authors suggested that microroughness be controlled to ≤8.0 nm for large areas ($20 \times 20$ μm$^2$) and ≤0.2 nm for small areas ($0.1 \times 0.1$ μm$^2$) to limit watermark formation.

Nagai also provided some insight into the relationship between roughness, contact angle, and watermark formation [64]. Using dynamic contact angle measurements to define wettability, he measured the contact angle of a droplet into which additional liquid was added allowing it to advance across the surface (with a contact angle $\theta_A$), and the contact angle of a droplet from which liquid was removed causing it to recede across the surface (with a contact angle $\theta_R$). The difference between the advancing and receding contact angles (contact angle hysteresis) provides some description of the "resistance" that a droplet may experience moving across a wafer. Previous results by Dettre and Johnson indicated that increasing roughness generally increases hysteresis [65]. It is reasonable to conclude that enhanced roughness creates greater resistance to contraction of a droplet lengthening the time for drying and, therefore, enhances the opportunity to form watermarks.

High aspect ratio features are also hard to spin dry without leaving stains due to the inability of this method to remove the water from the holes. Marangoni drying can effectively remove the water and also reduces or eliminates the staining. Gale *et al.* showed that a Marangoni IPA dry after a HF etch step for a tetraethoxysilane (TEOS) dielectric contact layer leaves no observable watermarks compared to a spin drying system [66].

Watermark formation is not limited to wet immersion cleaning steps. They also form after chemical mechanical polishing (CMP) processes. High via resistance due to watermark formation on top of tungsten plugs after CMP was observed by Chew *et al.* in which the watermarks acted as insulators between the metal layers [67].

#### *4.3.1.3 Watermarks on Wafers Caused by Immersion Lithography*

In addition to cleaning applications, water is now an important constituent for 193-nm immersion lithography. A droplet of water contacts both the lens and the wafer replacing the air that was the original transmission medium. This change in the refractive index allows for higher resolution. However, due to the water lens, debris and dissolved silica can collect in the residual water making watermark formation an issue. Figure 4.13 shows an example of a watermark bridging a series of parallel photoresist lines during exposure. The watermark caused the subsequent develop step to leave the bridging lines.

Mitigation of watermarks by adequate rinsing and cleaning before the development process is critical. Work is underway to improve water removal by having a rinsable top coat during the tetramethyl ammonium hydroxide (TMAH) develop step [68]. The development of a hydrophobic topcoat is another approach [69]. Other researchers have looked into the drying of the wafer after exposure to remove the water droplets [70] in a manner similar to single wafer spin drying systems that could be used on the develop tool or even the exposure tool.

### 4.3.2 Drying High Aspect Ratio Features and Stiction

After rinsing, HAR features must be dried without damage. Damage from residual contamination or collapse of features from stiction must be avoided during drying

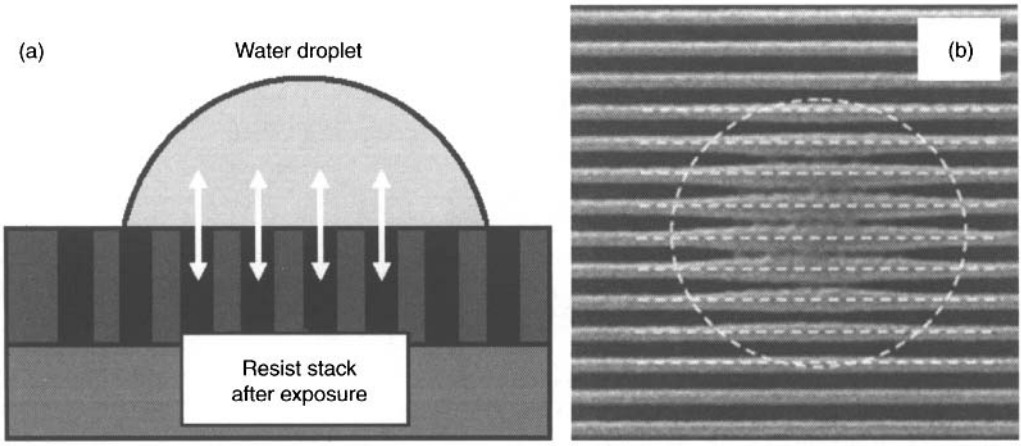


**Figure 4.13.** Schematic and SEM of a watermark after immersion lithography exposure; a) water droplet remaining on the resist surface after immersion exposure and b) the watermark after develop causing bridging of the 220-nm.lines [71]. Reproduced with permission from Wei, Y., "*Non-lensing defects and defect reduction for 193i*", SPIE Newsroom, 5037:917 (February 10, 2008).

the smaller linewidths in the newest generation devices. Wetting of rough surfaces and HAR features is discussed in Chapter 1.

Evaporative drying [72] and spin drying were once the only methods to remove water out of deep features. Evaporative drying had a tendency to leave residues in the bottom of the contact holes. Spin drying would remove most of the water, but some would remain in the holes. This was unacceptable because chemicals could remain in the bottom of the hole and cause corrosion. Silica can deposit and form a resistive layer causing high contact chain resistivity, and particles or unreactive polymer could remain sequestered in the features. The IPA vapor dryer and the Marangoni STG dryer described in Chapter 1 and also in reference [4] have prevented most of these issues.

Features such as DRAM (dynamic random access memory) capacitors that have the bottom electrode free-standing after oxide removal are prone to stiction upon rinsing and drying where the high surface tension of the DIW can draw the sensitive features together. Once dried, these fused structures cannot be separated, thus, creating a non-yielding device. To understand this mechanism, the capillary forces acting on the structures must be understood.

Tas and co-researchers have used cantilever structures to measure the stiction between two solids [73]. They investigated various attractive and adhesion forces such as capillary forces, hydrogen bonding, electrostatic forces, and van der Waals forces. A review of adhesion for micro-mechanical structures similar to some of the IC features is given in [74]. Stiction has been defined as the acting of adhesion mechanisms whenever flexible and smooth structures are brought in contact, whether with the substrate or with one another [75]. Like particle adhesion, capillary forces are the strongest [73], and therefore the stiction forces are investigated for this issue [76].

When two hydrophilic surfaces are separated by a thin liquid film, this layer acts an adhesive. If the contact angle between the surfaces is <90° indicating a

hydrophilic surface (Figure 4.6a), the two surfaces can have a net attractive force. Upon drying the liquid layer evaporates, and the two surfaces are pulled together due to capillary forces. This is dependent on the length and the rigidity of the feature – a threshold must be met by one of both surfaces for stiction to occur. The adhesion force where the features will be deformed at the critical length ($l_{crit}$) for the surface energy ($Y_s$), is defined as:

$$l_{crit} = \sqrt[4]{\frac{3}{8}\frac{Et^2g^2}{\gamma_s}} \tag{4.12}$$

where $E$ is the elastic modulus, $t$ is the thickness of the feature, and $g$ is the width between the two surfaces.

Upon drying, if the feature's critical length is reached, they will adhere and cannot be separated, and the length is defined as:

$$l_{crit} = \sqrt[4]{\frac{3}{16}\frac{Et^2}{\gamma_{lv}}\frac{g^2}{\cos\theta}} \tag{4.13}$$

Thus, by lowering the surface tension of the liquid rinsing the features, or upon drying, replacing a high surface tension liquid, such as water, with a lower one such as IPA or even supercritical $CO_2$, the length of the features can be increased without stiction occurring. Pacco compared various drying techniques (wet and supercritical $CO_2$) after a dilute HF cleaning step for HAR cylindrical DRAM capacitors with polySi lines on deposited oxide separated by 200 nm spaces at various lengths [77]. Both aerated and de-aerated DIW were used for rinsing. Results showed that keeping the surfaces as hydrophobic as possible after the HF bath by using de-aerated water prevented stiction. Keeping the wafers wet without allowing evaporation and collapse of the features before the crucial drying step, was also important. Additionally, the SRD technique yielded the same critical length as the Marangoni drying process, about 660 nm in this case, indicating that the rinsing step initiates the capillary forces, and the STG dryer cannot separate the structures once adhered. Figure 4.14 shows an example of a cylindrical capacitor experiencing stiction and a free-standing one without stiction.

### 4.3.3 Adhesion of Particles during Rinsing and Drying

The rinsing and drying steps should not add additional particles to the wafer surface. Even if particles are removed during the chemical processing steps, the particle removal efficiency (PRE) is never completely 100%. Upon drying, capillary forces similar to those experienced with stiction cause the adhesion of the particle to the wafer surface. As discussed in Section 4.2.1, the positively charged hydrophobic surface attracts negatively charged particles during the rinsing process and the negatively charged hydrophilic surface attracts positively charged particles, shown in Table 4.2. Negatively charged particles include silica and also some organics particles such as polystyrene latex (PSL) that many particle count studies use. Silicon nitride

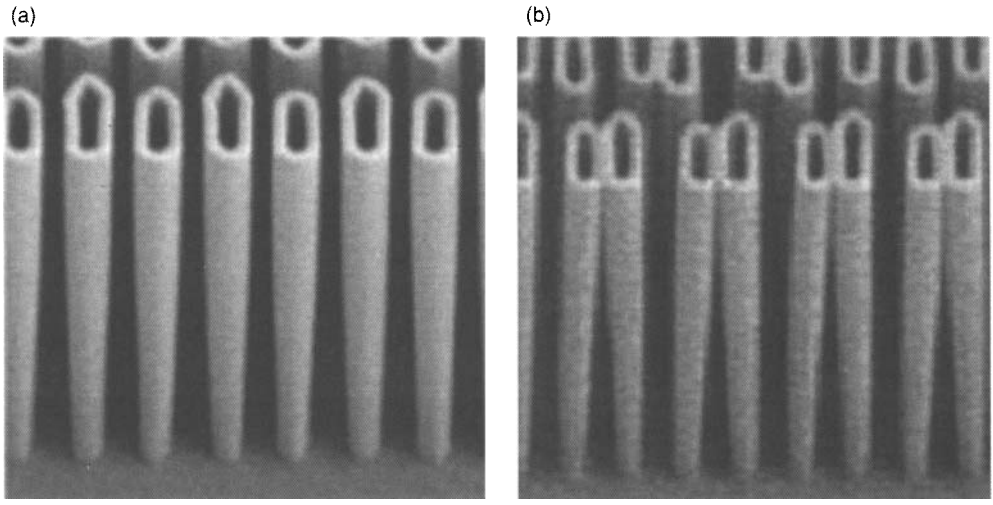


**Figure 4.14.** Scanning electron microscope images of a cylindrical DRAM capacitor with a) free-standing, no-stiction and b) stiction [78]. Courtesy of FSI International.

**Table 4.2.** Summary of hydrophilic and hydrophobic surfaces and particle adhesion propensity.

| | **Hydrophilic** | **Hydrophobic** |
|---|---|---|
| **Surface Charge** | Positive | Negative |
| **Attracts Particles with Charge** | Negative | Positive |
| **Wafer Raised** | Attached | Removed |
| **Wafer Immersed** | Removed | Attached |

and aluminum oxide, however, are positively charged and behave differently on wafers than silica and PSL. Thus, the pH of the rinsing solution is important, and is sometimes adjusted to minimize the adhesion of the type of particle that is expected to be in the solution, slurry particles after a CMP step, for example.

Sometimes megasonic energy is added to the rinsing step when the particle count on the wafer is critical, for example, during CMP processing. Researchers at IMEC have advocated the use of megasonic energy during the rinsing cycle prior to Marangoni drying [79]. They used an overflow rinsing bath equipped with a megasonic transducer. They also adjusted the pH of the rinsing step.

When a wafer has both hydrophobic and hydrophilic areas, upon drying, the particles tend to migrate to the hydrophobic areas where water droplets sometimes remain. Marangoni drying can either attach particles to the surface or remove particles depending on whether the water is drained or the wafer is raised. The behavior of particles on a wafer raised from the IPA/DIW meniscus is shown in Table 4.2 and depicted in Figure 4.15.

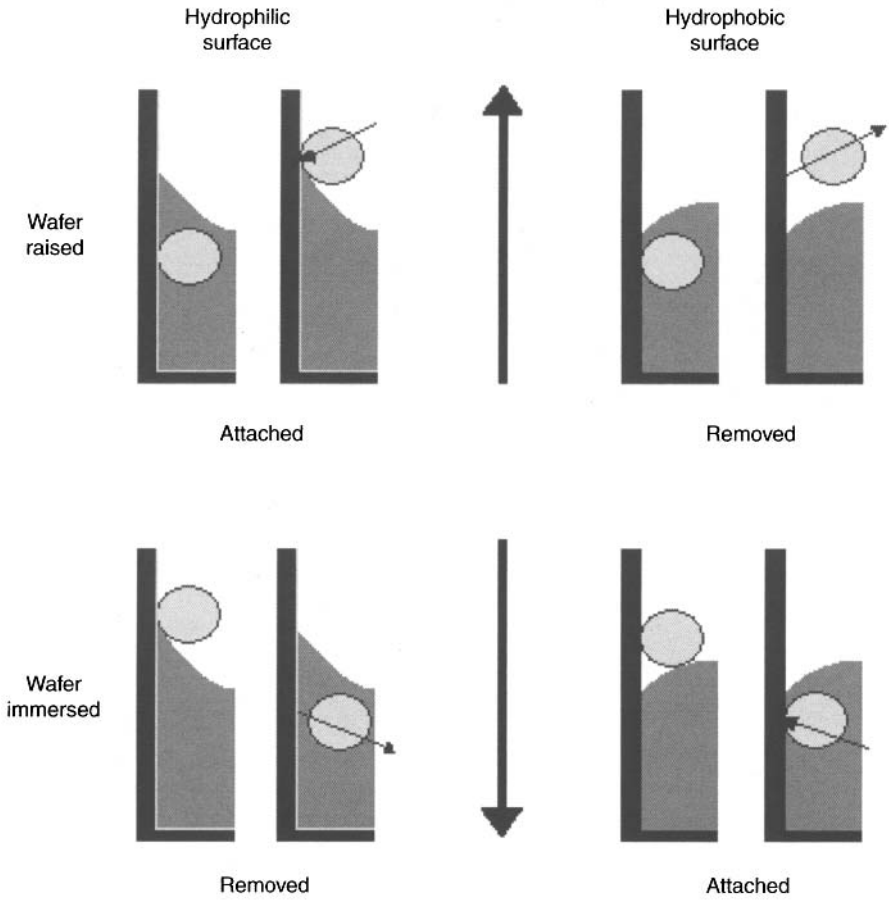


**Figure 4.15.** Schematic shown the effect on a particle for a hydrophilic and hydrophobic surface being immersed into or raised out of a liquid, typically in a Marangoni STG dryer $H_2O$/IPA. Used with permission from the author.

## Acknowledgements

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# Fundamental Design of Chemical Formulations

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*Abstract*
Chemical formulations are used because of the specific properties of the components in the mixture working in a synergistic fashion. Each component plays of role in the overall performance of the formulation. The key components for stripping and cleaning formulations are the base chemicals, additives, and in some cases, water for semi-aqueous cleaners. Design of chemical formulations according to solubility principles is used to tailor the solvents to the solute. Practical considerations are also given for designing a formulation.

*Keywords:* chemical formulations, solubility parameters, fluoride-based chemistry, amine-based chemistry, hydroxylamine, semi-aqueous chemistry, surfactants, passivating agents, buffering agents

## 5.1 Introduction and Overview

The formulations used for stripping photoresist, post-implant and post-etch residue removal (PERR), and post-CMP (chemical mechanical polishing) cleaning and particle removal have a long history. However, designing a chemical formulation to clean integrated circuit devices to accomplish the pre-set process requirements is relatively new. The semiconductor industry has borrowed knowledge from various other industries as it went through its initial growing pains and is now the technology leader in creating specifically formulated chemicals to clean the microstructures of the integrated circuit devices.

Wet chemical processing is an effective method for removing particles, metal ion contaminants, and native oxides from semiconductor devices. To be successful, a chemical formulation used for photoresist stripping and residue removal must be able to:

1. Strip the photoresist, remove the etching or implant residue and, if needed, remove etched or implanted crust.
2. Remove metallic contamination.

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3. Not leave behind any residue or particles.
4. Be easily rinsed, preferably with only water.
5. Be compatible with the materials to be cleaned.
6. Be selective to the films present.
7. Not damage or augment the films to be cleaned.
8. Not corrode.
9. Be compatible with the feature dimensions to be cleaned.
10. Wet the films and the features.
11. Penetrate into the features.
12. Not have undesirable side affects
13. Must not be extremely volatile.
14. Be used on commercially available tools – single wafer and batch and spray tools.
15. Be manufacturable with easily obtained chemicals and be commercially viable.
16. Be cost-effective.

This chapter will give an overview of techniques and processes used in creating unique chemical formulations. Included will be formulation design models and parameters that are important in creating cleaning solutions. The components of the formulations will be outlined. Practical considerations for the choice of chemicals and the mixtures will also be reviewed.

## 5.2 Historical Development of Formulations for the Integrated Circuit Industry

Like so much of the early semiconductor development, the stripping of photoresist with solvents was borrowed from other industries. Early researchers and process engineers gained insight into resin, photoresist, and residue removal from the paint industry and other areas that required removal of organic compounds without damaging the underlying material. Formulated strippers for silicone, paint, and other materials have a long history – usually additives are added to suppress certain undesirable effects, such as poor wetting (adding a surfactant), corrosion (adding a corrosion inhibitor or chelating agent), or poor solubility (adding a co-solvent).

The integrated circuit (IC) industry has evolved, and so has the sophistication of the photoresist stripper, PERR, and CMP cleaners. This section discusses the evolution of these products.

### 5.2.1 Chemical Formulation Generations

The term "generation" defines the succession of chemical mixtures used within the IC industry. Initially, the need for photoresist strippers came about due to the metallization process for FEOL (front end of line) gates and BEOL (back end of line) interconnects. The metal would react with an oxidizing agent, sometimes noxious compounds such as permanganate or sulfonate-based reagents.

Phenol-based strippers are considered first generation, which were replaced by N-methyl pyrrolidone (NMP) formulations, which subsequently evolved into formulations containing a variety of components, each with a specific function. Peters and coworkers have reviewed the various generations and the evolution of cleaners and strippers [1].

Beyond classification with respect to generations, formulations can be classified by their chemical properties and their components. Some of the formulations can fall into more than one classification. Typical chemical formulation classifications are:

1. Solvent
2. Solvent with additive
3. Semi-aqueous solvent
4. Fluoride-based solvent
5. Basic
6. Acidic

Figure 5.1 shows a summary of the different types of BEOL stripping and cleaning formulations and their respective components.

## 5.2.2 First Generation Oxidizing Chemicals

When the semiconductor industry was in its infancy, in the early 1970's, engineers probably used whatever chemical was readily available to remove resist, such as a strong oxidizing agent (KOH or NaOH), a polar solvent, or readily-available photoresist thinner, such as xylene. Since photoresist is composed of hydrocarbons, it naturally led to the use of oxidizing chemicals to remove the material.

Early oxidizing strippers included phenol or similar compounds, such as cresol, to remove photoresist with aluminum present on the wafers [3]. The phenol had the capability of removing the photoresist, but had undesirable side effects such as reacting with the sulfonic acid surface activating component to form an insoluble reaction

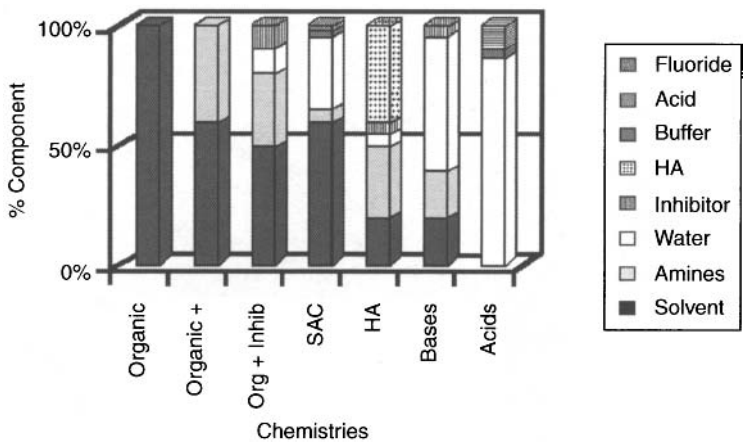


**Figure 5.1.** Chemical compositional summary of the different types of BEOL stripping and cleaning formulations [2]. Used with permission of Robert Small, RS Associates.

product. Additionally, very high temperatures (140–160°C) were needed to facilitate the reaction with the photoresist because of the high melting point of the phenol molecule, which also produced noxious fumes and odors. The addition of a perchloronated solvent, nowadays a known environmental hazard, was used to form a dense protective gaseous layer over the bath to quell the odor and evaporation.

Toward the end of the 1970's the phenol strippers were recognized as being undesirable due to their toxicity as well as their requirement of high working temperatures. At the same time, chlorinated solvents were also being phased out due to issues with safe disposal. Sulfonic acids were the choice to replace these undesirable components [4] and also permitted water rinsing after the stripping process [5], although later work showed a long water rinse gave the best results. During the time they were in use as additives to phenol strippers, the sulfonic acids also were found to have stripping properties. However, due to the high viscosity of the sulfonic acids, a hydrocarbon was used to reduce the viscosity [5]. This type of stripper worked well on many different types of photoresist, including positive and negative tone – Novalac-based resins and vinyl-based resins. With various additives such as fluoride, sulfonic acid-based strippers did not corrode metal [6] and could be used for stripping and cleaning aluminum interconnects, but the fluoride would etch silicon dioxide.

### 5.2.3 Second Generation Solvent-based Formulations

Before being used for photoresist stripping, solvents were used in the electronic industry; for example resin removal during the packaging of IC devices. These solvents, such as NMP, methylene chloride and tetrachloroethylene, were very good at dissolving vinyl polymers, which were the resins for early photoresist compositions. Solvents were chosen for use that had a high boiling point (NMP ~200°C), would not decompose over time, and readily dissolved the photoresist without leaving behind a detrimental residue. N-methyl pyrrolidone was the solvent of choice for many early IC manufacturers using both neat and formulated mixtures for stripping photoresist and residue removal in the presence of metals, and is still in use today – not only for IC, but for micro-electrical mechanics structures (MEMS), light emitting diodes (LED), GaAs devices, wafer-level packaging (WLP), and other microelectronic applications.

Early formulations involved the use of NMP with an oxidizing agent such as inorganic alkali hydroxides, such as substituted ammonium hydroxides, or carbonates [7]. In particular, these solvents were very useful for removing the residue after oxygen plasma stripping, which quickly and inexpensively removed thick photoresist layers with a more environmentally-friendly process than the short-lived phenol-based strippers. Additionally, the NMP solutions were viscous, but not to the extent that they could not penetrate the contact features to clean the residue. Rinsing after NMP processing was complicated by the fact that dilute amounts of water could render the solution basic, forming free $OH^-$ that would readily corrode the aluminum lines. Specialized rinsing after NMP processing was developed; an intermediate rinse in isopropyl alcohol (IPA) before rinsing in water, control of the rinsing water temperature, and assuring the formulation was completely removed from the wafer surface to avoid latent corrosion. Pre-rinsing

has also been shown to assist in maintaining adequate surface tension to allow wetting of the deep features, such as contacts and vias [8].

### 5.2.4 Third Generation Amine-based Formulations

Since amine-based solvent strippers worked very well for removing photoresist, these new cleaning chemistries were augmented with specific functional additives. Researchers at IBM proposed a cleaning solution using NMP combined with an alkanolamine [9], primarily for removing resin and polyimide coatings, but also for removing photoresist. The addition of an alkanolamine to the NMP increased the stripping power of the solution and decreased the processing time, without increasing the bath temperature.

During the 1980's a wide range of stripping and cleaning formulations were introduced, along with improvements of first [10, 11] and second generation strippers [12]. The amines used for the third generation strippers were water miscible [13] allowing a wide range of chemicals and additives to be used. However, reactivity with aluminum metal of the interconnect lines was problematic due their basic nature, as these chemistries promoted corrosion. Additives were soon being included into the formulations, along with non-ionic surfactants and detergents for wetting [14], corrosion inhibitors [11], and pH regulators and buffering agents.

Etching with biased plasma to provide directionality used polymer formation on the sidewall to provide anisotropy along with the directional plasma, which led to a new challenge in residue removal. Analytical tools were used to assess the residue and for the chemical formulation specialists to understand the type of "polymer" encountered. For example early work on aluminum etched with $CCl_4$ had a carbon polymeric residue remained on the surface after etching and that this residue contained not only aluminum, but chlorine that could react with water to form HCl [15] affording the same corrosion that occurred with other chlorine-containing etching gases [16]. Formulations were being developed, and the rinsing and drying processes associated with these cleaning steps were being optimized to remove these residues and prevent corrosion from occurring.

Crust material was also being addressed with specialty formulations. Removing hard-baked crust of photoresist formed by ion bombardment during etching and implant was also being investigated – for example, for heavily ($1 \times 10^{16}$ atoms/cm$^2$) implanted resist [17].

### 5.2.5 Hydroxylamine Photoresist Residue Removers

As IC manufacturing matured into the 1990's, advances in formulations chemistry were widespread. Hydroxylamine free base (HA or HAFB) formulations were introduced to wide acceptance and proved very effective at removing post-aluminum etch residue [18]. Modifications of the initial formulation were made by using additives. Chapter 9 covers the cleaning of aluminum surfaces in detail and thoroughly discusses hydroxylamine ($HO\text{-}HN_2$) formulations and the reaction mechanism that makes the chemical successful for removing post-aluminum etch residue. Hydroxylamine was tried for damascene cleaning, but was unsuccessful due to severe corrosion on copper metal, which was not successfully inhibited.

### 5.2.6 Fluoride-containing Strippers and Post-etch Residue Removers

Fluoride-containing semi-aqueous strippers and post-etch residue removers were introduced as a replacement for hydroxylamine cleaning chemistries at a time when copper was being introduced into IC manufacturing, in the mid and later 1990's [19]. These formulations are called semi-aqueous chemistry (SAC) because $H_2O$ is a major component. Most fluoride-containing formulations are limited in their ability to strip photoresist and are used for residue removal. Although some are formulated with components that can penetrate and swell the resist and the residue, these formulations become too aggressive at higher temperatures needed to remove resist.

The reaction that takes place for cleaning has an end product of low concentrations of HF. In ethylene glycol and water, the reaction is assumed to proceed as follows [19]:

$$NH_4F \rightarrow HF + NH_3 \tag{5.1}$$

Although the reaction is not completely understood, HF or possible $HF_2^-$, which etches $SiO_x$ (Chapter 3), possibly lifts off the residue, for example via etching, by undercutting the oxide. Other components in the semi-aqueous solutions are added to reduce the viscosity and surface tension, and regulate the pH to allow higher solubility of the reaction products.

Fluoride-containing formulations work well with single wafer processing because of their rapid reaction rates and because they can be used at room temperature.

### 5.2.7 Amine Post-etch Residue Removers for Copper

Amine-based chemicals originally targeted aluminum cleaning, but once copper was used for interconnects, these chemical formulations showed success and were modified for their use. The present-day amine-based chemicals that are used for stripping and residue removal in the presence of low-$\kappa$ and copper films have been specifically developed to be compatible with such materials. However, since amines are basic, certain low-$\kappa$ films are not compatible with these chemicals, especially at pH > 11. Additionally, many low-$\kappa$ films are not compatible with an acidic solution with a pH < 3.

One of the most highly successful amine components is an alkanolamine, in particular monoethanolamine, $HOCH_2CH_2NH_2$, similar to hydroxylamine. Many other alkanolamines exist and have been used for integrated circuit cleaning formulations. Alkanolamines are combined in formulations with corrosion inhibitors and passivating agents and also are compatible with and very soluble in water and/or with polar solvents and have been proposed in the same patent as hydroxylamine [18]. Both residue removal and photoresist stripping can be accomplished with these formulations.

With the widespread use of single wafer cleaning, both for CMP and for post-etch stripping, many formulations are designed for use in wet bench immersion, batch spin spray, or single wafer spin spray systems.

## 5.3 Mechanism of Stripping, Cleaning, and Particle Removal

Understanding of the physical mechanism of stripping, cleaning, and particle removal is key to formulating an effective cleaner. Work had previously been performed on photoresist dissolution after exposure, where swelling was an undesirable phenomenon, whereas with photoresist stripping, swelling enhances the removal. Similar approaches have been used to investigate the effectiveness of various chemicals, in particular solvents for photoresist removal after etching and implantation. These concepts are very important when designing a formulated composition.

The mechanism of stripping and removal of photoresist, residue, and surface conditioning has been shown by Obeng and Raghavan [27] to be a combination of:

1. Penetration.
2. Swelling.
3. Dissolution.
4. Passivation.

The stripping chemical must first effectively and rapidly penetrate into the polymeric photoresist film. Any crust of residue that is insoluble in the chemical or mixture may inhibit this step. Once the penetration of the solution is at a steady-state, dissolution starts to occur, and is dependent on rate of penetration of the solute in the photoresist. Researchers have found that the transition layer of solvent penetration is an important dissolution parameter [21], and this layer increases in thickness in the plasticization stage and maintains its thickness until the solution reaches the substrate. Swelling is important for solvents that dissolve the film. Studies on NMP have shown that before dissolution, films swell, producing a rubbery-like material, with linear dependence on the dissolution rate [22].

Reaction of the photoresist with the chemicals is observed with highly aggressive processes, such as sulfuric acid hydrogen peroxide mixture (SPM) or other oxidizing chemicals. Although there is some indication that reaction takes place between specific chemicals in the formulated mixture, for the most part, the photoresist is dissolved by the solution. When considering polymeric residues, a different mechanism is employed. In some cases, the material under the residue is etched, and the residues are lifted and removed, but no dissolution takes place.

Fluoride-containing cleaning agents are used for residue removal without photoresist stripping. Plasma stripping with oxygen and sometimes with forming gas [30] is very effective for removing the bulk photoresist, but leaves behind residues that contain fluorocarbons, metals, and any non-volatile reaction product. Hence, residue removal without photoresist stripping is extensively used for BEOL – both for aluminum and copper interconnect.

Once the photoresist is removed, either with plasma or with wet chemicals, the residue has to be removed. Unfortunately, the remaining residue can be very difficult to remove, and to further the difficulties, very few residues are the same even if the same feature. This is because the combination of photoresist, hardmask, film material, etch stop layer, underlying layer, etching chemistry, the amount of overetch, and stripping chemistry are unique for each particular company. Standards are

set for the industry, for example, the post-via etch residue is compared to Teflon® [24], and post-high-dose implant residue is compared to graphite [25].

To remove residue, various techniques are used; lift-off, where the sidewall or bottom polymer is undercut and the small particles are captured in the solution, but not truly dissolved; complexation, where the metallic species reversibly or non-reversibly react with a complexing agent or a chelating agent; and complete reaction, where the residue reacts directly with the cleaning agent and is dissolved in to the solution. Rarely does the cleaning solution react with the polymer although in some cases this has been theorized.

After the residue removal, there is a potential for some particles generated during the process to adhere to the wafer surface. Additionally, during the photoresist stripping process particles can be generated by the swelling and breaking up of the resist and primarily the crust or the residue. Particle removal is outlined in detail in [26].

Finally after the photoresist and the residue have been removed, the surface of the film must be passivated, whether a metal such as copper or aluminum, it must not corrode during or after the cleaning process. Figure 5.2 shows an example of a hydroxylamine formulation used for cleaning vias with aluminum metal exposed, but because of the electrical connections to the source and drain of the transistor (electrogalvanic corrosion), etching of the tungsten via occurred. Additionally, understanding the difference between the photoresist, the residue, and the particulate contamination is important. With the introduction of low-κ dielectric materials, the film is not much different in nature than the photoresist. Also, the organic bottom anti-reflection coating (BARC) layers can be difficult to remove as they are composed of polyimide that does not react with the solvents that can easily dissolve

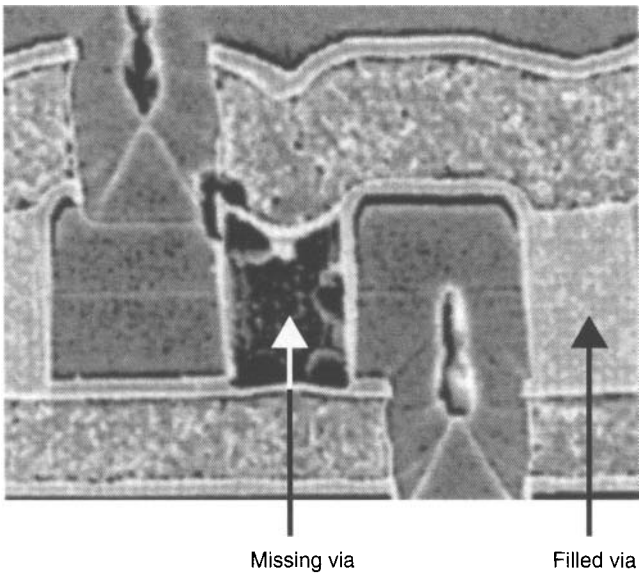


**Figure 5.2.** A scanning electron microscope image cross section of a hydroxylamine formulation-cleaned via with a missing metal in the via [34]. Reproduced with permission of ECS – The Electrochemical Society from Florence, D., Williams, B., Belisle, C., Hatcher, C., and Prasad, J., *Electrochemical Society Transactions*.

photoresist. Plasma etching can create a complex mixture of sputtered metals, fluorocarbon, intermixed film, and halogen species from the etching gas. Removal of these different layers and residues relies on different mechanisms for each.

## 5.4 Components and Additives in Chemical Formulations

Additives are used in chemical formulations to provide specific functions. The success of the formulation is dependent on the interaction of all the components. They must be able to be used in a mixture, not react together during the life of the product, and must be cost effective and available in high purity.

Generic chemical additive classes include:

1. Base chemical (water or other organic-based solvent).
2. One of more chemically active species (can be the same as the base chemical).
3. Buffering agent (pH control).
4. Surfactant for improved wetting.
5. Chelating agent.
6. Oxygen scavenging or passivating agent.

### 5.4.1 Base Chemical and Active Ingredient

The base chemical is chosen as the active chemical that does the actual removal of the photoresist or the residue. It usually is the main component, except for semi-aqueous formulations where water is the main component. For solvent-based systems, for example, this can be NMP. Hydroxylamine or monoethanol amines are other major components.

### 5.4.2 Buffering Agents

A buffering agent is used in chemical formulations to obtain a constant pH throughout the useful lifetime of a cleaning solution. A typical buffering agent used in photoresist strip, residue removal, and post-CMP cleaning does not interact with the active chemicals, but allows the chemicals to maintain their peak performance as the contaminated wafers are cleaned. Buffers are most effective when the pH is at a value within one unit of the $pK_a$ value [28], for very strong acids or bases (at very high or low pH) buffering agents do not perform well.

Using the Henderson-Hasselbalch equation [29, 30] to express the equilibrium between an acid, *HA*, and the conjugate base $A^-$:

$$pH = pK_a + \log\frac{[H^+]}{[HA]} \tag{5.2}$$

where $K_a$ is the dissociation constant of the acid, for the equation:

$$HA + H_2O \rightarrow A^- + H_3O^+ \quad K_a = \frac{[H^+][A^-]}{[HA]} \tag{5.3}$$

The result shows that when there is a high concentration of the conjugate base ($A^- >> HA$), there is little change in the concentration of the acid, and the result is a buffered solution. Since most cleaning formulations are basic, a conjugate base of the component contributing to the alkalinity is used as the buffering agent. The same holds true for buffering basic mixtures, the high concentrations of the conjugate acid, for example, in an amine chemistry:

$$R_3NH^+ + OH^- \rightarrow R_3N + H_2O \quad K_b = \frac{[HR_3N^+][OH^-]}{[R_3N]} \tag{5.4}$$

For semi-aqueous chemistry SAC formulations, Small and co-workers suggest it is critical to maintain a stable pH over time since water is the major component and the active components are in low concentration [31]. A large shift in pH, more than 4 to 5 pH units, can detrimentally lead to corrosion of the metal lines. Fortunately, the researchers found that low concentrations of the water-soluble amine species used for SAC act as pH buffering agents. Figure 5.3 shows the pH variation over time with various dilution levels.

Most formulated semi-aqueous cleaners have been developed with a controlled pH value. Addition of an organic acid helps to lower the pH, even when a solvent is used in addition to the fluoride-containing chemistry [32]. For solvent-based cleaning, a controlled pH value is not relevant for the neat solution, but upon rinsing, the pH value will provide information on the acidity or alkalinity of the solution when exposed to water, as shown by Lin [33].

### 5.4.3 Surfactants

Surfactants are used for decreasing the surface tension of the solutions and increasing the wetting. This is particularly important when high aspect ratio features are to be cleaned, or when hydrophobic material is in contact with the solutions. Surfactants can also be used for micelle formation in which the contaminant is surrounded

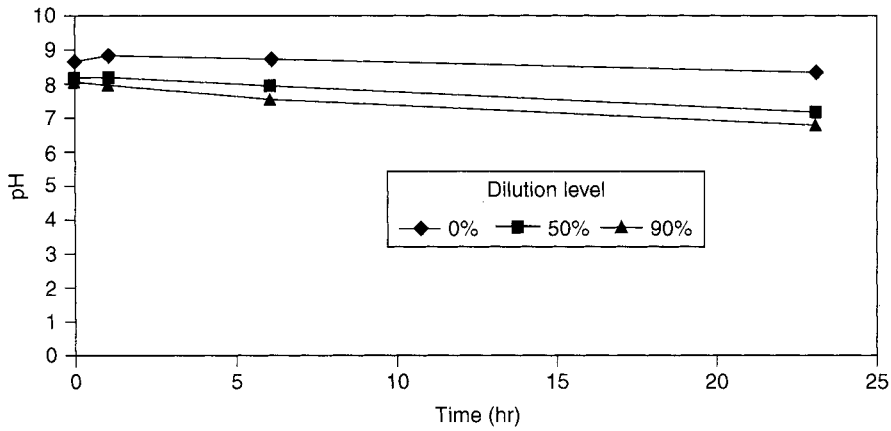


**Figure 5.3.** pH drift *vs.* bath life for semiaqueous chemistry with different dilution levels [31]. Reprinted from *MICRO*. Copyright Tom Cheyney, Los Angeles, CA. Used with permission.

by the surfactant arranged in such a manner to solvate the unwanted impurity. Surfactants that have high solubility in water can be used for semi-aqueous formulations. Surfactants can also be used in solvent-based cleaning formulations; however, organic solvents typically have a lower surface tension than water. There are surfactants that are inert to both acidic and basic cleaning chemistries. A good overview of surfactants and the chemistry and physics associated with their use is given in [34]. Many surfactants have been proposed for use in stripping and cleaning formulated solutions including amphoteric, non-ionic, ionic, both cationic and anionic.

Effectively dispersing the chemical onto the surface is important for cleaning hard-to-wet films. Wetting of the material depends on effectively getting the reactant molecule to the area in need of cleaning. The solution should rapidly spread out onto the surface to immediately initiate the cleaning process. Wetting is important for cleaning BEOL features such as low-$\kappa$ (low dielectric constant) dual damascene structures where the low-$\kappa$ film is hydrophobic. Surfactants can lower the surface tension to improve the wetting and thus the cleaning capability. Hydrocarbon surfactants can obtain a minimum of 26–28 mN/m, but to further lower fluorinated or silicon-based surfactants are needed [34].

One such surfactant class used in cleaning solutions is non-ionic. This type of surfactant has strong temperature dependencies on their solution properties – in most cases the activity increases with increasing temperature. Ionic surfactants can be classified as anionic or cationic depending on their charge. Surfactants are designated by their molecular weight.

Due to the lowering of the surface tension, some solutions, especially those with organic solvents, easily tend to foam and, thus, an anti-foaming agent is needed to suppress this phenomenon. Foaming is caused by holes being formed in the solution, thus creating air bubbles. Both thermal (*e.g.* gas formation) and mechanical effects (*e.g.* agitation) facilitate the formation of foam. Anti-foaming agents are also used in formulations.

Surfactants for the use of particle removal were proposed in the early days of the IC industry [35]. To form a micelle, which are used for particle removal or removal of other unwanted contamination, the surfactant typically has a hydrophobic and hydrophilic moiety taking advantage of the charge on the particle [26]. The backbone of the surfactant contains these functional groups in which the particle binds, allowing the particle to be dispersed.

Surfactants can also assist in the prevention of static friction (stiction) by lowering the surface tension and thus preventing line collapse. In some cases the surfactant also assists in the solubility of the solvent into the water solution.

Examples of surfactants used in chemical formulations are dimethyl hexynol (Surfynol-61), ethoxylated tetramethyl decynediol (Surfynol-465), polytetrafluoroethylene cetoxypropylbetaine (Zonyl FSK, Zonyl FSH), or simple long chain polymeric molecules, such as polyoxyalkylene ether, ethoxylated alcohol, polyoxyethylene butylphenyl ether, or polyxoyethylene, or long chian ionic species such as alkylphenyl sulphate or simple quarternary ammonium salts.

Surfactants can be effective at concentrations as low at 0.1 wt% up to approximately 5 wt% where solubility limits are reached or when foaming becomes out of control. Surfactant additions of up to 20% or as low as 100 ppm have been found in the literature.

### 5.4.4 Chelating Agents

Chelating agents can be used for a variety of reasons – the most critical is metal removal from the solution to prevent redeposition. Additionally, metal passivation by the chelating agent can prevent corrosion. Although chelating agents are defined as having multiple sites to bind with a metal ion, sometimes irreversibly, the disposal of these metal-containing organic compounds is difficult due to local laws. Therefore, most solutions use a complexing agent that acts like a chelating agent: for example, 1,2-dihydroxybenzene as a complexing/chelating agent added to hydroxylamine [36].

### 5.4.5 Oxygen Scavenging or Passivating Agent

This area is so important that it has its own chapter devoted to this subject for copper: Chapter 11, which discusses in details the difference between an oxygen scavenger, a complexing agent, and a passivating agent.

Aluminum also is prone to corrosion. A thorough study of aluminum corrosion is presented in [37]. Chapter 10 also covers the stable regime of aluminum in aqueous solutions. After etching with chlorine-based plasma to delineate the aluminum interconnects, residual moisture in the air is enough to react with the chlorine embedded in the post-etch residue and form HCl [16] that reacts with the metal to form pits. The use of certain solutions for cleaning also exacerbate the situation; research into corrosion of aluminum on aged aerospace equipment has yielded data on aluminum stability with respect to pH, both high and low pH solutions corroded aluminum [38]. However, the aluminum surface that is passivated with an oxide film is relatively stable in the range from pH ~4 to ~9, as discussed in Chapter 10. When aggressive reactants are in the solutions that can breakdown the oxide layer, even in this pH range, corrosion and pitting can occur [39]. Most aluminum cleaning formulations chose to limit corrosion by controlling pH, *vs.* adding a complexing or passivating agent, unlike copper corrosion prevention. Corrosion inhibitors in aluminum cleaners are added to control titanium corrosion, for example, in an hydroxylamine-based formulation [36].

## 5.5 Creating Chemical Formulations

Knowledge about the physiochemistry of the individual components and their interaction is a key to formulating a successful mixture. Mixing successful formulations was more of an art than a science in the early days; scientists who were familiar with the interactions would take similar solvent molecules and try to make them work. To introduce science, modeling was used and was taken advantage of not only for integrated circuit formulations, but for anti-corrosion, oil and grease clean-up and a variety of other surface-dependent applications.

Evaluation of the performance of chemicals formulations and modeling of these performances are being assessed by various researchers. Specifications of chemical and physical metrics that the chemical formulation must meet are defined, an example is shown in Table 5.1. However, the actual performance results are the basis by which the final product is judged.

**Table 5.1.** Typical properties specified for formulations used in the integrated circuit manufacturing industry.

| Property | Specification |
|---|---|
| pH | Dependent on solution; in water, solvents will not have pH value |
| Flash Point (°C) | Pensky-Martens Closed Cup |
| Vapor Pressure (mm Hg) | Typically at 77°F (25°C) and at operating temperature |
| Odor | None |
| Specific Gravity (g/cm3) | Typically at 77°F (25°C) and at operating temperature |
| Surface Tension (cP or dynes) | at 77°F (25°C) |
| Viscosity | at 77°F (25°C) |
| Other | Biodegradability |

### 5.5.1 Overview of Techniques Used in Creating Chemical Formulations

The first step in creating a chemical formulation is to determine the need for a solution to an existing problem. For new applications, the definition of the problem and the past approaches that worked and did not work are outlined and for similar integration schemes, films, and layer. Most companies have a thorough knowledge of the current state-of-the-art of formulated chemicals – their strengths and weaknesses. The process steps involved, before and after the chemical cleaning step should be thoroughly understood, and both the effect on the transistor level and the interconnect level must be taken into account. Once the metrics and success criteria are defined, then the formulation work takes place.

### 5.5.2 Formulation Design Models and Parameters

Once the formulation design process initiates, the formulation chemist plans his/her selection of chemicals based on the some of the parameters below (an example is for a photoresist stripping formulation):

1. Permeation rates and etching rates of the solution for photoresist.
2. Breakthrough rates of the solution through implanted crust, post-etched residue, or hard baked photoresist.
3. Etch rates and selectivity to other materials present.

The selection of the components starts with the knowledge of the miscibility of the various components and the solubility of the polymers to be dissolved. This is intrinsic to the development of new formulations and understanding legacy

products. To assist in choosing and designing a chemical formulation the following are considered:

1. Determine possible combinations of components.
2. Determine the compatibility of chemicals with photoresist.
3. Determine the solubility of the photoresist in the mixture, both high and low concentrations.
4. Determine the wettability of the feature and films.
5. Determine corrosion potential and electrochemical affects of the solution with the films.
6. Assess the thermodynamics of the reaction vs. the kinetics (i.e. is the reaction diffusion limited).
7. Other additives; for example, surfactants, passivating/inhibiting/chelating agents, stabilizers, pH buffers and controlling agents.

Once the basic formulation is determined, other factors come into play:

1. Optimize the formulation mixture.
2. Assess reaction with the environment.
3. Assess evaporation rate.
4. Assess water condensation or oxygen incorporation.
5. Assess and understanding environmental effects.

Once the formulation is ready for product testing, the following criteria must be determined:

1. Testing with respect to product specifications (*i.e.* photoresist and residue removal capability).
2. Testing at different process conditions: time, temperature, and tool (single wafer or batch).
3. Assess rinsing conditions and the ability to completely remove the chemicals.
4. Assess pot life and chemical lifetime.

Finally, the chemical is tested at a customer site and the device yield and electrical performance is assessed long with any long term effects on the packaged devices. Figure 5.4 shows a graph of the water content in hydroxylamine chemistry over the bath life.

Developing each new chemical formulation from scratch is very time consuming. However, there is a vast knowledge base to aid in the development and testing of the components; various forms of modeling and known physical performance factors are used. Lin was one of the first to use solubility parameters to show novelty in his patent [33].

#### *5.5.2.1 Solubility Parameters*

A solvent is any liquid, organic or not, that can be used to dissolve another material. The solute is the material to be dissolved, in this case photoresist

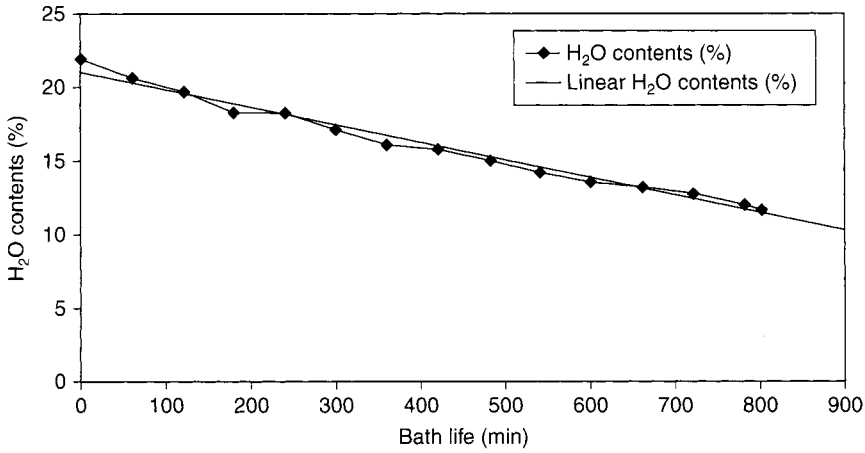


**Figure 5.4.** The decrease of the water content in hydroxylamine chemistry over the bath life [40]. Reprinted from *MICRO*. Copyright Tom Cheyney, Los Angeles, CA. Used with permission.

or polymeric residue. By combining the solvent with the solute, a solution is formed – the dissolved photoresist in the solvent. But it is not so simple – for example, the photoresist resin has limited solubility, more than one component is in the photoresist, undesirable side reactions occur with the metal films, and the solution must be able to be rinsed. Also, polymers such as photoresist have solubility parameters just like solvents.

To assist in choosing the right solvents, modeling of the solvent properties is used. Two widely known are the Hildebrand [41] and Hansen [42] solubility parameters. Both solubility parameters models are beneficial for predicting the results when formulations are developed.

In 1916 Hildebrand noticed that the solubility of solids or gases in liquids were not adequately expressed by the theories proposed by many scientists and devised his own expression for solubility ($\delta$), based on the heat of vaporization ($\triangle H_v$), which is the square root of the cohesive energy density:

$$\delta = \sqrt{((\Delta H_v - RT)/V_m)} \tag{5.5}$$

where $R$ is the idea gas constant, $T$ is the absolute temperature, and $V_m$ is the molar volume. The cohesive energy density is defined as the energy needed to infinitely separate a unit volume of molecules from their neighboring molecules. Compounds with similar $\delta$ values will similarly dissolve the same solid including the same amount of swelling. Also, compounds with similar $\delta$ values will be miscible with one another. Hildebrand solubility parameters are particularly useful for predicting solubility of polymers in solvents, and hence have been adapted by the manufactures of photoresist strippers and post-etch residue removers. However, this parameter does not work well for non-polar, non-hydrogen-bonding solvents. A review of solubility and the Hildebrand solubility parameters is given in [43].

For polar molecules, the Hansen solubility parameter is useful for estimating miscibility, molecular affinities, and other phenomena, such as phase segregation. Hansen solubility models use three energy parameters [42]:

$\delta_d$ – dispersion bonding between molecules.
$\delta_p$ – dipolar intermolecular force.
$\delta_h$ – hydrogen bonding.

These parameters are modeled in a three-dimensional (3D) space to compare values between different solvents:

$$R_a = \sqrt{4(\delta_{d2} - \delta_{d1})^2 + (\delta_{p2} - \delta_{p1})^2 + (\delta_{h2} - \delta_{h1})^2} \tag{5.6}$$

where $R_a$ is the distance between the parameters in the 3D space. This parameter is compared to the radius of a sphere, $R_o$, with the resulting number being the relative energy differences (*RED*) between the values:

$$\frac{R_a}{R_o} = RED \tag{5.7}$$

Defined as:

RED = 0 – no energy difference
RED < 1 – high affinity, the molecules and will dissolve.
RED = ~1 – boundary condition, the molecules will partially dissolve.
RED > 1 – low affinity, the molecules will not dissolve.

Factors such as the temperature of the solvent, the electrostatic interactions, and the size of the molecules all play a role in the predictability of the Hansen solubility parameters. Nevertheless, knowledge of these parameters assists in understanding the molecular-level interaction of the solvent and the solute and optimizing the envelope of conditions best suited for these chemicals.

Although the solubility parameters do not always work (there are always solvents that do not obey the equations set forth), they are guidelines that assist in the formulation of mixtures. Various researchers have attempted to explain solubility in terms of various physical or chemical constraints. Surface energy has been suggested as one such metric to remove BARC from etched via structures [44].

### 5.5.2.2 *Selective Solvency*

Based on the Hidebrand solubility that like molecules can dissolve in one another, selective solvency is used to assess their miscibility in one another. For materials to dissolve, interactions between the molecules must be overcome as the molecules separate allowing for the solute to closely interact, thus dissolve, in the solvent. Therefore, materials with similar solubility parameters will be able to solvate one another. Although the basis is made for one liquid to another, this can apply to photoresist and residue. This is especially helpful for solutions that may separate

over time into distinct layers, where one component is slightly soluble in another such as an addition of a surfactant.

#### 5.5.2.3 *Kinetic Salt Effects*

The kinetic salt effect changes the rate of the reaction of salts present in the solution [45]. The salt affects the reaction through stabilization, also called kinetic electrolyte effect (kinetic ionic-strength effect). Rate constants vary with ionic strength, increasing or decreasing depending on the charge of the species. Ionic strength is given by:

$$I = \sum \left(\tfrac{1}{2}\right) m_i z_i^2 \tag{5.8}$$

where $m$ is the molarity and $z$ is the charge of the ion, for the chemical reaction:

$$\mathrm{A} + \mathrm{B} \rightarrow \mathrm{X}^* \rightarrow \text{Products} \tag{5.9}$$

where $A$ and $B$ are the reactants and $X^*$ is the activated species before forming the final products. The Brøndsted equation describes the effect of the ionic strength in the rate constant, $k$:

$$\log k = \log k_o + 1.02 z_a z_b I^{1/2} \tag{5.10}$$

The final effect is the stabilization of the reaction when the appropriate salts are added to the solution.

### 5.5.3 Practical Considerations

When a chemical formulation is developed, extensive testing ensues to insure the mixtures can meet the stringent demands of high volume IC manufacturing. These requirements include: a long bath life, the ability to perform optimally over time and with small variations in the product, (*i.e.*, thickness, residue), and use in a high volume manufacturing tool, whether a single wafer or batch immersion. Above all, the formulation must be cost effective, and meet the cost of ownership demands for the individual process step, such as having a short processing time and being a simple process (*i.e.* no intermediate rinsing, one-step process).

#### 5.5.3.1 *Bath Life and Bath Life Extension*

The bath life, also known as pot life, is a strong function of temperature and number of wafers processed. After many hours of use at high temperature, the chemicals in the mixture can decompose and thus cause undesirable side reactions – volatile solvents can evaporate, and hygroscopic materials attract water and dilute the mixture. For a batch process, the pot life of the bath should be at least 24 hours. For single wafer processing, where some chemistries are used only once, the formulation must be able to be stable in the bottle and not form a precipitate or side reaction.

The build-up of particles and metallic contamination over time is an important consideration. A recirculation filter for batch tools is capable of removing particles. Filtering of the liquid at point of use can use useful for single wafer tools.

When first generation stripping chemicals were introduced into high volume manufacturing, the temperatures used were very high, in some cases, greater than 150°C. With the current generation of chemical formulations, the process temperatures are typically between 45–85°C, and the trend is to use lower temperatures with single wafer tools. This alleviates some of the problems with decomposition, but the lower temperature also reduces potential chemical reactivity making the process time longer. This is especially true for single wafer processing that employ point of use heating where the process time should be less than 1 minute. For stripping, at reasonable process times, batch tools require <30 min with 5–20 min being typical, and more time for stripping photoresist and residue removal than residue removal alone.

Water in semi-aqueous PERR is the most critical component, thus, maintenance of a constant concentration is key. Figure 5.2 demonstrates the results of water absorption a hydroxylamine solution – uncontrollable corrosion of the metal, completely removing a contact interconnect. Water should not be allowed to be carried over or in any way come into an amine chemistry bath.

In the drive to lower costs and to reduce chemical consumption, IC manufacturers have made some modifications in normal wet bench cleaning protocols. Figure 5.5a shows a typical wet clean process flow. A cassette of wafers is immersed in the chemical cleaner for a set amount of time, then transported to an intermediate rinse (in some cases), and finally a DIW rinse and $N_2$ dry step.

When a high operating temperature cleaner/photoresist remover is used (typically 65–85°C), a common problem is that the bath evaporates very quickly. One method of correcting this is to regularly spike the cleaning bath with an aliquot

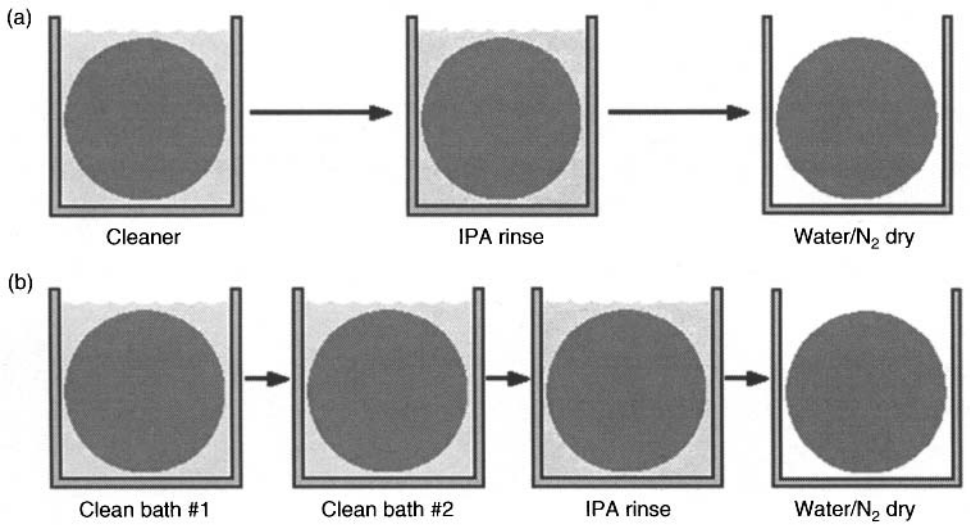


**Figure 5.5.** Increase in bath life by using additional chemical baths; a) standard process flow with one cleaning bath and b) process flow with two cleaning baths, the first which is more contaminated than the second, allowing the wafers to experience a clean solution before rinsing. Used with permission from the author.

of the major component that is lost to evaporation. In many cases, the bath can be readily chemically monitored and easily brought back to proper specifications. This process can often be completely automated. In this way, a variety of organic solvents, and even water, can be accurately added.

A second method to recharge a depleted solution is to add a replenishment mixture of the lost active components of the cleaner. This method is a little more difficult to set up and requires some trial and error to determine the correct volumes to add, but can prove highly efficient in high volume manufacturing. One drawback is that the replenishment solution may cost nearly as much as the initial cleaner, so significant cost savings are not always achieved.

A third method simply involves a bleed and feed procedure. The first bath is filled, and as wafers are processed, fresh chemical is fed into the bath at a rate that is equal to or slightly greater than the evaporation rate. In this way the bath is maintained at a constant volume with a very small overflow. Component evaporation is greatly reduced resulting in a longer bath life for a minimal increase in cost.

Another problem affecting bath life, particularly for thick resist removal steps, is the accumulation of excess resist in the cleaning bath. When this occurs, redeposition of undissolved or partially dissolved resist is observed. This results in contaminated wafers that are only partially clean. Further, redeposited photoresist is often more difficult to remove from the wafers resulting in significant rework time. One solution for this problem is the addition of a second cleaning bath (Figure 5.5b). As bath #1 becomes loaded with dissolved resist, it is drained and replaced with the less contaminated bath #2. This second bath is then refilled with fresh cleaner. In this way the wafers are always exposed to a relatively clean bath before proceeding to rinse baths. In addition to minimizing wafer rework, this method can also result in reduced chemical usage. Many chemical formulations have been designed with this in mind.

Although these techniques have mostly been used for wet bench cleaning, they may be modified for use in spray tools. In particular, the bleed and feed replenishment method is routinely used in spray tools to keep cleaning formulations within the proper specification. However, these methods are not as well suited for use in a single wafer cleaning tool. These tools often use inexpensive "one pass" chemical mixtures, which then go straight to the chemical drain. Additionally, single wafer tools are generally not designed for thick resist removal due to required high temperatures and long process times, which result in lower throughput.

Most IC manufacturing facilities now contain highly automated cleaning tools and wafer handling equipment. The above processes, when properly introduced, can be run completely hands free in a high throughput setting. This results in savings from lower labor costs, lower chemical costs and higher yielding wafers from reduced rework.

### *5.5.3.2 Materials Compatibility*

Lists of materials that are considered safe for use in wet processing tools are given in SEMI spec S14. These are also the materials that the chemical should be compatible, such as o-rings, the exhaust system, and any other material the chemical could come into contact with.

#### 5.5.3.3 *Tool Configuration – Single Wafer vs. Batch Processing*

The chemical formulation must work on the tool it is being used. Single wafer spin tools must meet the throughput of a batch processing system. The single wafer process modules are usually exposed to atmosphere, unlike batch spin spray tools. Batch immersion tools can control the temperature and can immediately quench the process by transferring the wafers to the rinsing tank.

#### 5.5.3.4 *Rinsability*

The ability to rinse the chemical off the wafers easily with a simple water rinse is the optimal for cost constraints. However, some chemicals require a complex series of rinses because of the corrosive nature of the chemical formulation once diluted. In fact, it has been shown that corrosion does not take place, in some cases, until the wafer is moved into the rinsing cycle. Methods used to avoid corrosion employ intermediate rinses with solvents such as IPA. In some cases cleaning chemical formulations have specific post-chemical cleaning rinsing formulations.

#### 5.5.3.5 *Shipping and Shelf Life*

Shelf life is the time period the chemicals are assumed to be usable at approximately the same effectiveness as the new chemical. The shelf life of chemical, both for mixing the formulations and for the mixed formulation, is important for optimum processing; particles should not form, precipitation should not occur, segregation should not occur, and the chemicals should not decompose or react with the environment. Sometimes to lengthen lifetime of the chemical, it is shipped under an inert environment such as argon. In some cases the lifetime of the chemical is indefinite, but in other cases it is short due to reaction with the atmosphere, photo decomposition, or other detrimental effects.

#### 5.5.3.6 *Purity Level*

Not all effective chemicals that the formulation chemist wants to use can be found cost-effectively in semiconductor grade. The highest purity material in the semiconductor fab is water. Typically, measurement of approximately 50 species, metals, mobile ions, anions and cations by numerous analytical techniques such as atomic absorption spectroscopy (AAS), inductively coupled mass spectroscopy (ICP-MS) at levels less than 100 ppt are required to assess the highest level of purity. Compared to water, the chemicals are rather impure, an example of a solvent-based chemical purity is Shipley 1165, with levels for some of the maximum impurities: chloride 5.0 ppm, sodium 1.0 ppm, and iron 1.0 ppm. Achieving the highest purity at the lowest cost, for large volumes of chemicals is an important consideration for choosing the chemical for use in formulations.

## 5.6 Environmental, Safety, and Health Aspects

Many noxious and environmentally unfriendly chemicals have been used over the years for photoresist stripping and cleaning. The semiconductor industry has, for

the most, part, embraced the use of low-environmentally hazardous chemicals and practices sound disposal and abatement techniques. Only a small number of the many chemicals used by the semiconductor industry are classified as substances of very high concern (SVHC) under the 2006 EU Reach regulation [46].

Environmental issues resulting from process steps is only apparent once the production process is well under way. Because they are not routinely considered when initially implementing these processes, the environmental impact on cost, yield, and cycle time is not realized until the process is well underway and production [47]. Many wet cleaning solutions in use contain hazardous air pollutants (HAP), which are banned in some manufacturing fabs, and other cleaners, which exceed the local disposal standard, are also not acceptable. Therefore, evaluating and mitigating the environmental impacts of the chemicals and processes at the earliest possible stages of designing formulations is very important to prevent potential environmental health and safety (EHS) showstoppers, plus optimizing the balance between environmental priorities and factors such as cost, yield, cycle time, performance, *etc.*

Manufacturers have focused on the assessment of the chemicals used in wet cleaning steps, reduction of the amount of chemical uses, and reduction of water. However, it sometimes takes a long time to qualify an existing chemical, even if the environmental impact is large.

The formulation design process has focused on these areas taking into account the environment impact for the next generation of cleaning solutions without sacrificing the quality of results, including:

1. Using sustainable, recyclable, or reusable materials.
2. Using materials with a low generation of waste including easily rinsed materials.
3. Using low chemical consumption
4. Using low temperature wafer processing.
5. Using high efficiency processes, where the wafer is only exposed to one chemical process.
6. Using high efficiency rinses to minimize water usage.

Designing cleaning formulations by incorporating the Twelve Principles of Green Chemistry [48] is one important aspect new product development. An example for reclaim chemicals, Chapter 13, is the goal of reducing potentially hazardous by-products and increasing the low reclaim yield because the process itself can damage the underlying silicon. Thus a solution is needed that yields better process results with less impact on the environment and helps semiconductor manufacturers effectively recycle their existing test silicon wafers.

For formulated solutions, some of the highest impact chemicals are organic solvents. Solvent recycling is a common practice in the IC industry, but use of solvents is still prevalent. For example, 51% of the industrial waste at one semiconductor plant is composed of organic solvents [49]. Selection of solvents that have low environmental impact is being addressed, and not only by the semiconductor industry [50]. The United States Government Environmental Protection Agency (EPA) lists environmentally friendly semi-aqueous components, now somewhat out of date [51].

In the semiconductor industry, many papers have investigated the use of low-environmental impact solvents. Kesters and co-workers at IMEC have evaluated 9 solvents and 50 solvent mixtures, whose selection was based on EHS criteria, for dissolving deep ultraviolet (DUV) photoresist [52]. They found that a large domain of safe solvents exists; most of the solvents and mixtures stripped the photoresist in < 10 min, with some as fast as 30 sec. Specific chemicals have been proposed that are on the EPA and European Union REACH list of safe chemicals – for example dimethyl suloxide (DMSO) [53]. Unfortunately, sometimes there is no non-hazardous alternative to a chemical, but these cases are rare. Classes of chemicals that are still being understood are being researched, such as hydrofluoroethers (HFE), not only for dyeing, but for their solvent properties [54].

Besides modifying the chemical formulations to use green solvents, other areas of interest from an EHS standpoint are improving the longevity of the chemicals. Due to the fact that even trace amounts of metallic or particulate contamination can adversely affect the cleaning process, most chemicals are used for a short period; some cleaning applications mix and reuse the chemical only once then dispose. Solvent reclaim has been set up at some sites for NMP [55], for example, but due to the low quantities of solvent in semi-aqueous formulations, it is not always cost effective to recycle small quantities onsite. For most companies it is quite expensive to dispose of solvents, many chemical formulation companies have taken it upon themselves to provide collection and recycling of the spent chemicals. Fluoride-containing formulations have special considerations for their disposal.

Other areas of improvement are chemical stability; due to the unstable nature of some inorganic acids at elevated temperatures these decompose and/or evaporate quickly leading to shorter bath life. The ability to rinse off the chemicals quickly also is important: the easier to rinse, the less water is consumed. Using the reclaim as an example, the traditional process requires 72 gallons of chemistry and 60 gallons of rinse water. The new formulation developed RegenSi™ consumes 36 gallons of chemistry and 24 gallons of rinse water.

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# 6

# Filtering, Recirculating, Reuse, and Recycling of Chemicals

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*Abstract*
Filtration is a key aspect of contamination control for the manufacturing of integrated circuits. Particulate contaminants can be found in cleaning chemistries – both in bulk distribution as well as in the tools. Particles are also generated from etching and cleaning processes within the tools. Proper choice of filtration materials and design is complex and dependent on the application and tool design with careful consideration of the process. For example, filters can be optimized for single pass or recirculation efficiencies, intended for single wafer spray tools or chemical recirculation batch immersion tools, respectively. Particle metrology is integral to confirmation of particle control, and in combination with proper filtration, will provide high confidence in minimization of particle related contamination. Utilization of chemical management and chemical reuse will reduce the chemicals cost in the fab.

*Keywords:* filters, filtration, contamination control, point-of-use, recirculation, chemical recycling, chemical reuse, chemical distribution, chemical management, particle counters, bulk chemical delivery, filtration mechanisms, chemical blending

## 6.1 Overview of Wet Chemical Contamination Control

Wet cleaning removes surface contamination from the wafer and prepares the surface for subsequent processes. A number of process requirements and challenges affect the choice of the process and design of the tools used to provide the wet cleaning. Contamination control is critical to these processes to prevent particle deposition due to the chemistry or due to particles removed from the wafer surface. Filtration is utilized to remove particles from bulk chemicals prior to distribution through point-of-use in the tool. Recirculating chemicals enhances particle control *via* multiple passes through filtration, as well as conserves chemical usage. Recycling, where possible, further reduces the cost and volume of chemicals used.

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### 6.1.1 Contamination Control Challenges Relating to Chemical Distribution

Particulate and chemical purity control are critical for effective wet cleaning processes. While the latter is controlled *via* assay of incoming chemicals (or certification of chemical purity by the supplier) and carefully controlled blending in the fab, there are many opportunities for subsequent contamination from wetted components and equipment including those that do not have direct contact with the wafer surface. Furthermore, particles can be generated by chemical reactions, by movement of chemicals and friction from components in the distribution system, and from other places in the processing tool that make their way into the fluid system. Metrology and detection of particles are also difficult. While real-time particle counting is possible in distribution systems, this is virtually impossible in the tool itself. Particles added onto a wafer surface typically are detected after a series of processing steps including cleaning, rinsing, and drying making the source of the particle contamination difficult to isolate. Additionally, metallic and organic contamination including bacterial growth must be controlled in the chemical baths and recirculating systems. Detection of these contaminants will be briefly reviewed in subsequent sections.

### 6.1.2 Use of Filtration to Control Particle Contamination

Properly designed filtration will minimize particle contamination in distribution systems as well as point-of-use (POU) in the tool. Although chemicals are purchased with very low particulate concentrations, pumps, valves, and other components will contribute particles to the fluids. This is of concern for both the chemical distribution system and the cleaning tool. Additionally, filtration is vital in the tool to remove wet cleaning-generated particles from the wafer surface. This prevents redeposition of these particles onto the wafer surface, and maintains the cleanliness of an immersion bath for each subsequent boatload of wafers.

### 6.1.3 Metrology Techniques for Particles

Particles in fluids are typically measured by laser light scattering particle counters. An overview of particle detection is found in Chapter 8 of the *Handbook of Silicon Wafer Cleaning Technology* [1]. These counters effectively determine particle trends and can provide immediate notification when particle count excursions occur. The current generation of particle counters is limited to 65-nm particle size resolution, which is larger than the critical particle size control needed for processes.

While there is the promise of improvement in the near future, the minimum size detection will be greater than the size detection needed, and this gap continues. Further, the typical sensitivity of particles in the smallest detection channel can be as low as 1–5% further making detection of particles in fluids with low particle concentrations difficult. This gap in measurement capability for evaluating filtration performance is critical to address in the near future since pore size is smaller than size detection of current particle counter technology.

### 6.1.4 Metrology Techniques for Dissolved Contaminants

Metals are detected using inductively coupled plasma mass spectroscopy (ICP-MS). This is a highly sensitive technique capable of detection to parts per trillion (ppt) depending on the chemistry. While the instrumentation is extremely sensitive, it is an off-line technique and, therefore, not real time. Sampling must be done in an extremely careful manner to prevent inadvertent contamination, and sample bottles must be of the appropriate material and properly pre-cleaned. This is currently the best known method for metal detection.

## 6.2 Bulk Chemical Distribution for Wet Cleaning Tools

Chemical distribution has evolved from out-of-the-bottle pouring to fab-wide chemical distribution systems that directly provide processing equipment with the chemistry blended on-board or prior to use on the tool. The complexity of these systems has increased to minimize contamination and provide proper safety. Additionally, the bulk chemical distribution (BCD) systems have evolved to provide faster throughputs, improved yields, and reduced contamination levels.

### 6.2.1 Bulk Chemical Delivery Systems

Wafer manufacturing processes utilize a variety of liquid chemicals to provide cleaning, etching, surface conditioning, and photoresist stripping on a wafer [2]. Many of the chemicals used are toxic and must be properly handled to prevent operator exposure. Many are also reactive or flammable and present fire and other safety hazards while others are corrosive, have high vapor pressures, and can degrade process equipment. Chemical delivery systems are designed to safely and reliably transport pressurized chemicals through distribution tubing to points-of-use within a wafer fab. The purity of these chemicals must be maintained or even enhanced as they pass through the bulk chemical delivery system. Contaminants in the form of particles, dissolved metals, and dissolved organic molecules can all reduce manufacturing yield and reliability of integrated circuit (IC) devices. Chemical purity becomes more critical as IC feature sizes become smaller and device layout becomes more complicated.

During the early years of semiconductor device manufacturing, process chemicals were stored in glass or plastic bottles. These bottles were transported to the processing equipment and manually poured into the tanks by operators. This method presents potential hazards during transportation and use because glass bottles are easily broken potentially exposing operators to toxic materials. The chemicals can be spilled or splashed when they are poured into processing tanks, baths, or other containers. Chemicals with high vapor pressures are released into the environment each time the bottle is opened. Finally, the bottles must be thoroughly rinsed prior to disposal or recycling. Again, any spilled liquids or vapors can expose operators to hazardous chemicals. Moreover, the sheer volume of chemicals used in large manufacturing fabs makes bottle handling highly impractical.

Chemical delivery systems were introduced into semiconductor manufacturing facilities to eliminate the hazards associated with bottled chemical delivery. In these

systems, the chemical is pressurized and transported to POU within the fab through distribution tubing. Safe operation is achieved by enclosing all of the pressurized components in the system in either stainless steel lines (for solvent chemicals) or plastic tubing with secondary containment (for aqueous chemicals) to provide protection against leaks. Other than the distribution lines of tubing, all components in the system are enclosed in cabinets or junction boxes. Leak detectors are installed in the cabinets and junction boxes that depressurize the system in event of a leak averting possible dangerous conditions from developing.

### 6.2.2 Bulk Chemical Delivery System Design

Table 6.1 shows the typical stages of most chemical delivery systems. For the delivery train, chemicals can be pressurized to the distribution system by use of pumps or by pressure vessels. If pressure vessels are used, they can be filled using pumps or vacuum. To ensure uninterrupted delivery of chemicals to POU, redundant components are always used at key locations in the system that have the potential for failure or require periodic maintenance such as pumps, pressure vessels, and filters.

**Table 6.1.** Bulk chemical delivery system stages.

| Stage | Apparatus | Use |
|---|---|---|
| 1 | Supply chemical container – drum (typically 30–55 gallons), intermediate bulk container (typically 220–550 gallons), or tanker truck (typically 2500 gallons) | Often redundant feeds to achieve uninterrupted supply of incoming chemicals |
| 2 | Fluid transfer device (pump or vacuum) | Transfer chemicals from a supply container to a storage tank |
| 3 | Storage tank (typically 50 gallon or larger) | Local supply for the delivery engine |
| 4 | Delivery train options | Provides pressurized feed to the distribution system, usually includes filtration |
| | a. Pumped chemical delivery | As shown in Figure 6.1a |
| | b. Pressure vessel chemical delivery options | As shown in Figure 6.1b |
| | 1. Pressure vessel filled by vacuum | |
| | 2. Pressure vessel filled by a pump | As shown in Figure 6.1c |
| 5 | Distribution system – main line tubing, valve manifold boxes, leak sensing, branch line tubing, secondary containment | Supplies chemical to the POU in the wafer fab |

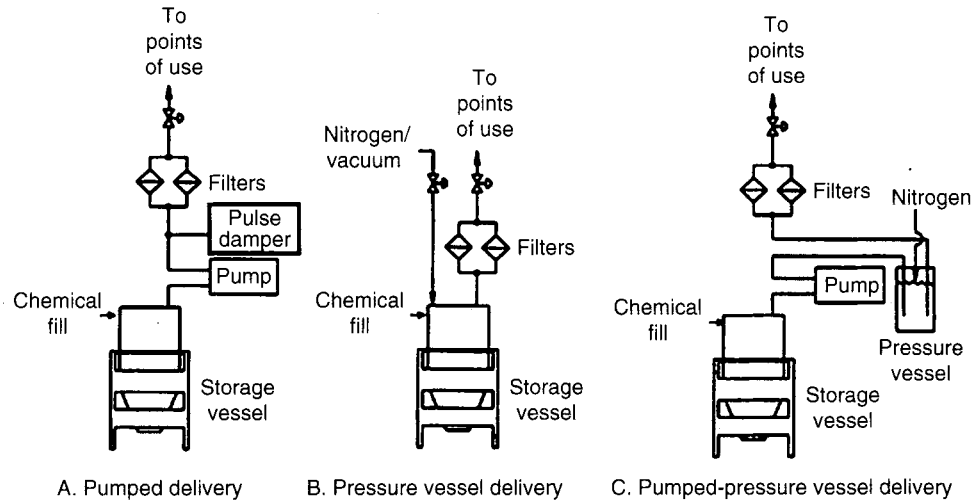


**Figure 6.1.** Schematics of different types of bulk chemical delivery train designs. Used with permission from CT Associates, Inc.

Since most chemicals are hazardous (corrosive, oxidizing, flammable, or water reactive), chemical delivery systems must be enclosed in hazardous production material (HPM) rooms. These rooms must comply with strict design requirements as defined by the international building code (IBC) and international fire code (IFC) [3]. Key requirements of HPM rooms consist of spill containment and detection, segregation between chemicals of different hazard class, ventilation, and fire detection.

### 6.2.3 Particulate Purity Control for Bulk Chemical Delivery Systems

Properly designed chemical delivery systems can supply chemicals that contain particulate concentrations well below those found in bottled chemicals. The key to delivering chemicals with low particulate contamination levels to fab POU is using a chemical delivery system that minimizes the addition of particles into the fluid stream and removes particles that enter the system from the incoming chemical or generated from the delivery system.

Filtration is used to remove particles from the fluid stream. It has been found that continuously flowing fluid through the filters reduces particle shedding compared with stopping the fluid flow when there are no demands for chemicals [4]. Stopping and then restarting flow through a filter can cause a significant hydraulic shock resulting in particle spikes that take a considerable time to recover, and these additional particles can travel to the POU. Recirculation flow within the chemical delivery module and the fab-wide distribution system can achieve improved particle removal performance [4]. Figure 6.2 details the flow schematics for different methods of recirculation. It is common practice that fab-wide recirculation is typically not employed since the relative particle improvement over internal recirculation is usually small assuming proper downstream distribution system design and high purity components are used.

Implementation of constant flow through the delivery system filters requires a complex control system because fab chemical demands are intermittent and variable.

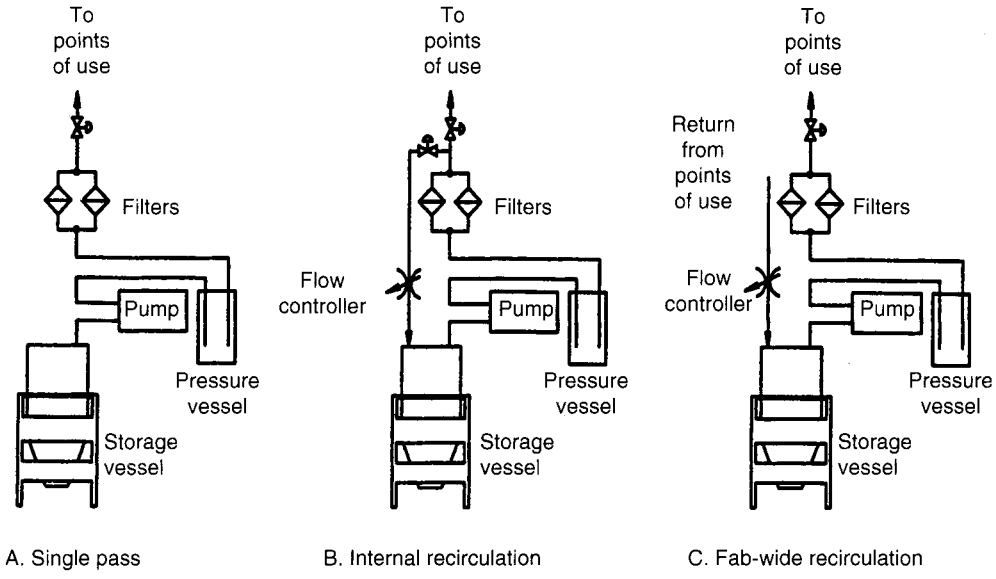


**Figure 6.2.** Bulk chemical delivery system designs with recirculation for improved particle performance. Used with permission from CT Associates, Inc.

Although maintaining constant flow may not be practical, it is relatively easy to maintain a constant recirculating flow through the filters. Under these conditions, the total flow rate through the filters is the recirculating flow plus the fab demand. This mode of operation does not eliminate hydraulic shocks to the filter, but reduces them considerably. Figure 6.3 shows the benefit of recirculation on particle performance compared with no recirculation.

The components used to assemble a chemical delivery system must also be free of particles so that they do not contaminate the pure process chemicals. In recognition of the need for particle cleanliness, many component manufacturers sell pre-cleaned parts in carefully sealed packaging. Strict attention to chemical compatibility is also necessary because degraded parts can release large numbers of particles during system operation. Selection of high purity components are necessary to minimize the number of particles added. The components must have a smooth surface finish, minimal dead spaces where particles can collect and then be released, and minimal abrading surfaces. An example of such a component choice is the preponderant use of diaphragm valves instead of ball valves in delivery systems.

Pumps can shed particles by imparting flow pulses upon the filter media. Pulsation dampeners are used to reduce the magnitude of the pulsations. These devices are comprised of a small vessel downstream of the pump that has an internal chemically resistant bladder with pressurized chemical on one side and pressurized gas on the other side. Vessels using filtered pressurized inert gas to deliver chemicals to the distribution system can provide superior particle performance because they impart minimal pulsation upon the filters. Filling of the pressure vessels from the storage tank or supply container can be accomplished by pumps or by evacuating the off-line pressure vessel (vacuum-filling). Pumps have a lifetime based on their wear and

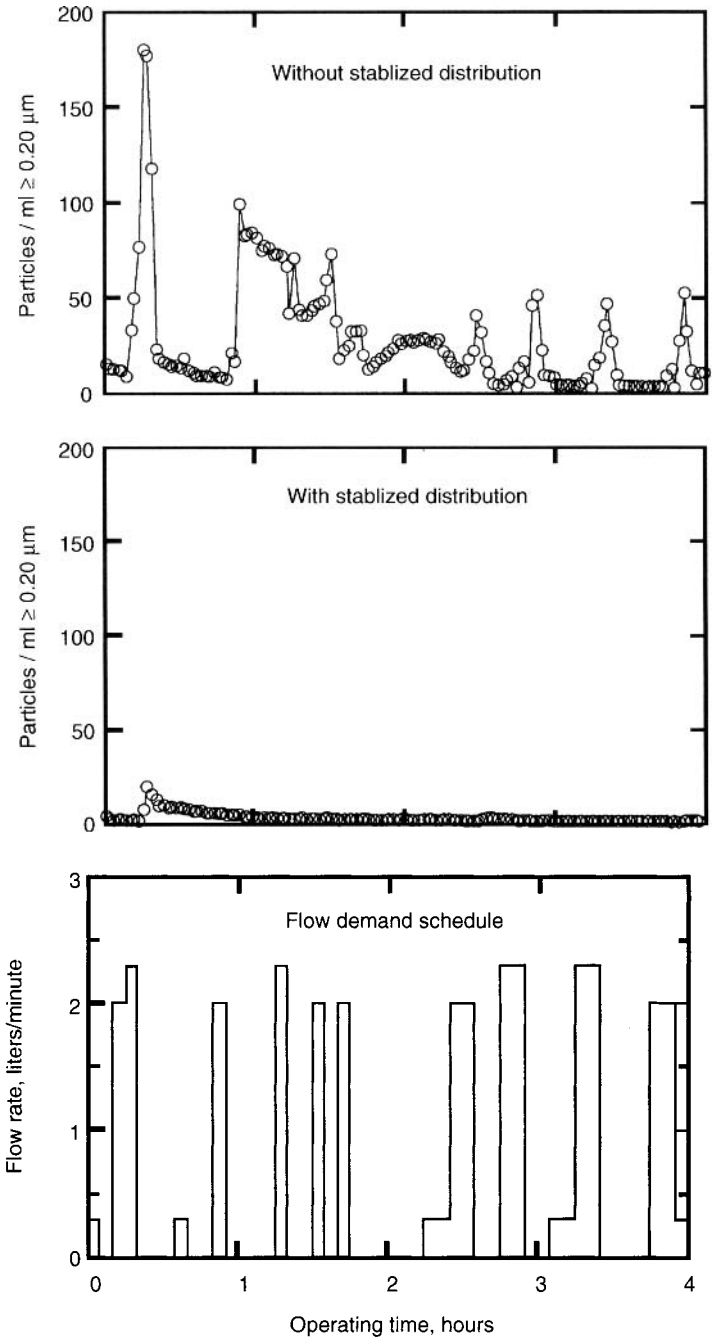


**Figure 6.3.** Graphs show the results of bulk chemical delivery system particle performance over time without and with recirculation [2]. Reproduced with permission of ECS – The Electrochemical Society from Deal, D. B. and Grant, D. C., *Contamination Control and Defect Reduction in Semiconductor Manufacturing III.*

must be rebuilt periodically. A pump designed for vacuum-filling will require less maintenance if a gas driven Venturi effect is used to generate the vacuum in the delivery vessel. Some process chemicals are sensitive to dissolved gases; therefore, using a pressure vessel delivery method can generate gas bubbles on the wafer surface that in turn can cause particle-like defects [5]. When these bubbles collapse, they leave empty voids in the substrate that act as defects.

The ideal technique would deliver chemicals at elevated pressures with minimal fluctuations in pressure and flow rate while minimizing contact with the pressurized gas. The selection of the optimum delivery technique for any individual application must balance the required chemical purity with system complexity and cost. See Figure 6.4 for an example of an optimized bulk chemical delivery equipment design.

### 6.2.4 Metallic Ion Purity Control for Bulk Chemical Delivery Systems

Because there is currently no in-line technique to remove metallic impurities from chemicals, it is critical that chemical delivery systems do not add impurities. Extraction of metallic impurities from chemical delivery systems is controlled through careful selection of construction materials and the use of certified clean components developed for microelectronics equipment [6]. For aqueous chemical

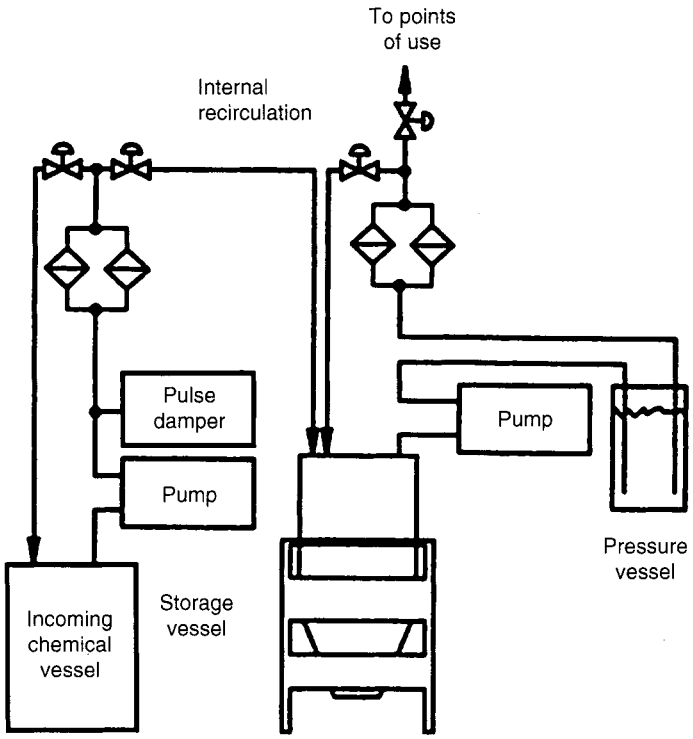


**Figure 6.4.** Optimized bulk chemical delivery equipment design. Used with permission from CT Associates, Inc.

systems, fluoropolymers, such as perfluoroalkoxy (PFA) and polytetrafluoroethylene (PTFE), are commonly used because of their low metallic extractable levels and high chemical compatibility. For solvent chemical systems, electropolished and passivated 316L stainless steel tubing and components are used.

Qualification of newly installed aqueous chemical delivery systems is necessary to guarantee that the systems do not add metallic impurities to the chemicals delivered to the POU. Solvent chemical delivery systems are typically not qualified other than for organic contamination due to their use of organic chemicals. Extraction of metallic impurities from chemical delivery systems is usually measured by taking simultaneous samples of the chemical entering the system and at various locations throughout the system. The samples are analyzed for metallic impurity concentrations. The change in concentration between the various sample points is assumed to be caused by extraction from the delivery system. Because the impurity levels in chemicals are very low, careful sample collection, preparation, and analysis are crucial.

Perhaps the largest source of error in measuring metallic extractables from chemical delivery systems is related to the system holdup volume, or internal liquid volume of the system, and the variability of the incoming chemical. Samples taken from different parts of the delivery system may have come from different lots of an incoming chemical. Because there can be wide variation in the quality of the incoming chemical, comparing metal ion concentrations in samples taken simultaneously from different parts of the system can be misleading. One way to eliminate this source of error in determining the cleanliness of the delivery system is to fill the system with a chemical, then circulate the chemical and monitor contaminant concentrations over time with no chemical addition or usage [7].

It is possible to deliver chemicals with extremely low addition of metallic impurities – at sub-ppb to ppt levels depending on the chemical. Efforts to control metallic impurities in high purity chemicals process chemicals are also being focused on by formulation manufacturers, discussed in Chapter 5. Only the cleanest chemicals available should be used in semiconductor fabs because the purity of an incoming chemical is directly related to the purity of the chemical delivered to the POU.

### 6.2.5 Organic Purity Control for Bulk Chemical Delivery Systems

Chemical suppliers generally control organic contamination by using high-grade feed stocks and lubricant-free pumps and valves in their manufacturing operations. Ion exchange resins and activated carbon have been used to reduce organic contamination from the product chemical. Cleaning shipping containers can prevent organic addition from prior stored chemicals or from the container itself.

Organic contamination internal to the fab chemical delivery system can come from a variety of sources: oils and lubricants used in the manufacture or operation of the components; oil vapor from compressed gas used for purging the chemical delivery system during assembly or maintenance; or contamination from human contact (skin oil). Contamination can be prevented by using high purity components that have been thoroughly cleaned with high purity solvents and hot deionized water (DIW) and enclosed in packaging that have low plasticizer contents. Oil-free compressed gases are used for system purging and for welding. Oil

contamination from human contact is prevented by wearing latex rubber or other contamination-resistant gloves when handling any system components during fabrication or maintenance.

### 6.2.6 Chemical Delivery Sub-systems

On-site blending of chemicals is often performed to maximize cost effectiveness. Purchasing concentrated feed chemicals and then diluting to the required concentration can greatly reduce the number of containers transported from the chemical suppliers and handled on-site. In addition, receiving concentrated chemicals can reduce shipping expenses and decrease the number of empty containers to be recycled or disposed.

Semiconductor fabs have ultrapure DIW (UPW) on-site for use in various processing steps such as post-chemical rinsing. Blending UPW with a concentrated chemical can achieve higher purity than a dilute chemical received from suppliers that can be contaminated by metallic and organic extraction from the chemical container. The added space requirements, operational complexity, and process control sensitivities for the blending equipment must be factored into the overall decision an IC fab must make on whether to do on-site blending.

The chemical feedstocks are adequately filtered so blended chemistry has low particle levels. However, filtration in blending systems typically is required to prevent particles added from the blending system components, as is the case for chemical delivery systems.

## 6.3 Chemical Distribution, Filtering, and Recirculation Requirements for Wet Cleaning Tools

The equipment used for wet cleaning of semiconductor wafers must be capable of supplying numerous chemicals and chemical mixtures to the wafer surface in a defined sequence. The equipment also must be capable of rinsing to prevent chemical cross-contamination and of drying the wafers following the cleaning sequence. Reference [8] discusses the various cleaning tools.

The tools used in wafer cleaning have different requirements for chemical distribution, filtering and recirculating, plus are different with respect to chemical reuse. They can be divided into two categories: batch and single wafer tools. Batch tools can be further divided into immersion and spray tools. In batch immersion tools or wet benches, wafers are sequentially immersed into cleaning solutions in separate baths. In batch spray tools, batches of wafers contained in cassettes are rotated past stationary spray posts that dispense the cleaning chemicals onto the wafer surface. In typical single wafer processors, the wafer is mounted on a rotating chuck, and the cleaning chemicals are dispensed onto the wafer surfaces through nozzles.

### 6.3.1 Recirculating Immersion Tools

Recirculating immersion tools have been a mainstay for wet cleaning for many years. In a typical cleaning operation, cassettes of wafers are immersed sequentially

in multiple baths containing cleaning solutions followed by rinses after each bath. The rinses terminate the reactions taking place in each chemical bath. Rinsing must ensure that the reaction is terminated at the proper time and that chemicals from the previous cleaning step do not contaminate the subsequent step. After a final rinse, the wafers are dried.

The baths in immersion tools are continuously recirculated to maintain chemical concentration uniformity and to remove particles from the cleaning solution. The chemicals added to the bath are typically supplied from bulk chemical delivery systems and contain low particulate concentrations. However, particles are introduced to the bath when the wafers are immersed, and particles are often produced during the etching or cleaning processes. Hence, particle removal is necessary to prevent wafer contamination.

Particle removal is accomplished *via* filtration. The chemicals in each bath are removed from the bath, filtered, and returned to the baths as shown in Figure 6.5. Because the particles are generated in the bath, the bath must be recirculated rapidly ("turned-over" quickly) if low concentrations are to be achieved. However, centrifugal pumps are typically used to recirculate the baths, and filter particle removal efficiency and pressure drop are often inversely related. Therefore, if highly retentive filters are used, the filter is often restrictive, and the circulation rate is decreased.

The optimum filter used in a recirculating immersion bath should have both high retention and low pressure drop. Optimum performance is not always easily obtained with a highly retentive filter because of the restricted flow. For example, Figure 6.6 compares model predictions of particle concentrations of particles $\geq 0.1$ μm in a typical bath circulated through polyvinylidene difluoride (PVDF) filters with pore sizes of 0.45, 0.20, and 0.10 μm [9]. The filter that obtained the most rapid particle removal had 0.20 μm pores. Filters have been developed for some specific baths that have both high retention and low pressure drop [10]. Filters such as these offer optimum performance in specific chemical baths.

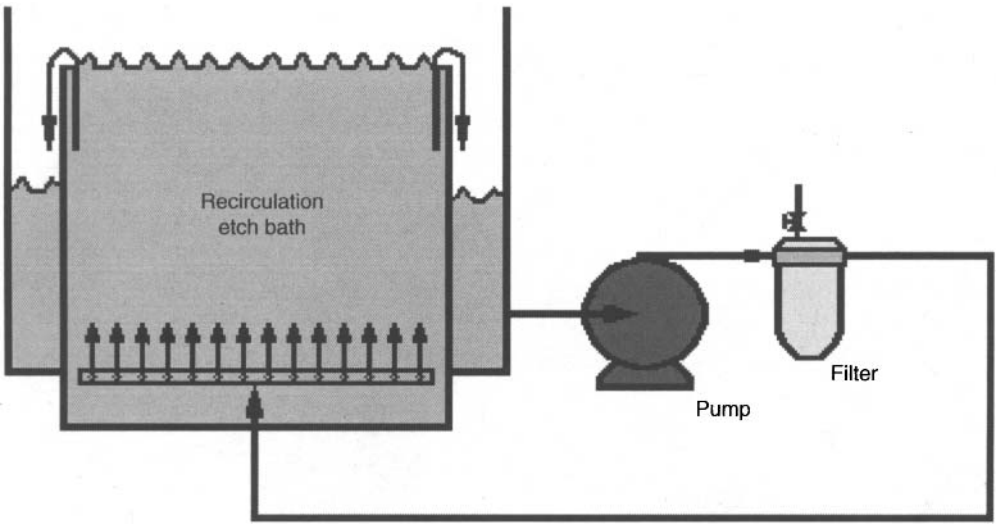


**Figure 6.5.** Schematic of a recirculating etch bath. Used with permission from CT Associates, Inc.

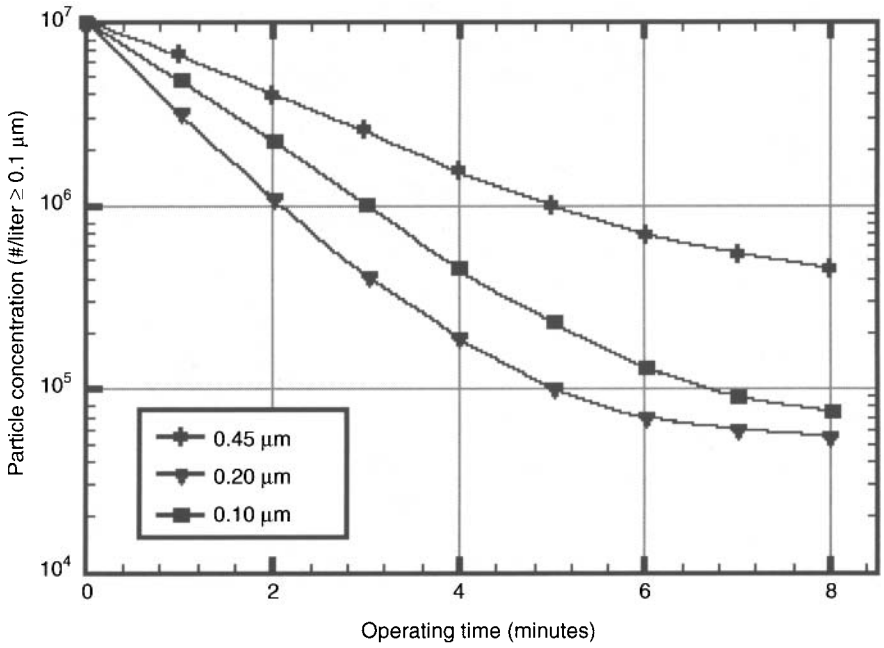


**Figure 6.6.** Model predictions comparing PVDF filter performance in a recirculating etch bath. Used with permission of CT Associates, Inc.

Some of the cleaning processes performed in recirculating etching baths result in decreased concentrations of cleaning constituents after multiple batches due to either reaction with contaminants or degradation. Examples include hydrogen peroxide in SC-1 (standard clean-1) and SC-2 (standard clean-2) the chemistry of which is outlined in [8]. In addition, concentrations of contaminants in the baths increase as the contaminants are removed from the processed wafers. The increased contaminant concentrations can result in reduced cleaning efficiency or even deposition of contaminants onto relatively clean wafers. For these reasons, baths are sometimes periodically spiked with fresh chemicals with the overflow to drain (bleed-and-feed), or are completely replaced based on time or the number of wafers processed.

The components (tanks, pumps, valves, tubing, *etc.*) used to assemble these systems must be properly selected to ensure that they do not add contamination to the baths. Contamination can take the form of particulate, metallic, or organic contamination all of which can negatively impact wafer yield and performance. Components are typically constructed from materials similar to those used in BCD systems to prevent contaminant extraction. Component qualification procedures are also similar [2, 11].

## 6.3.2 Single Wafer Tools

Single wafer tools are relatively new to wafer cleaning and are finding widespread acceptance. The driving force for their use has been the ability to allow individual wafer control of both front surface and back surface cleaning. Equipment of this type is able to perform many of the cleaning procedures achieved in recirculating immersion baths including physical processes such as particle removal using

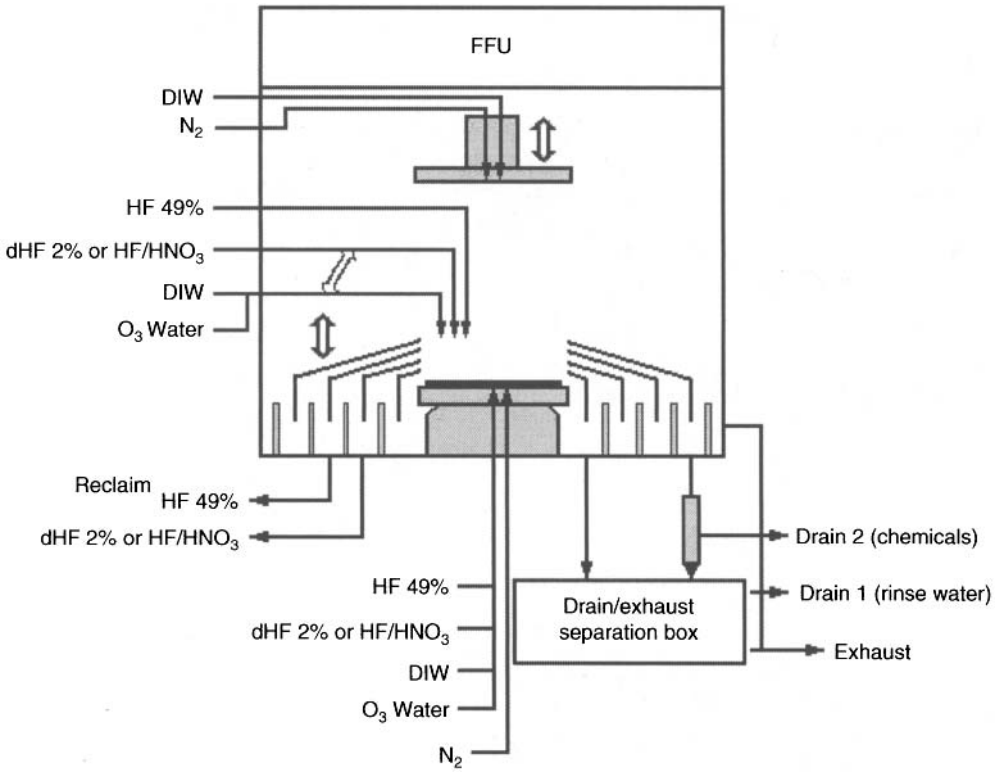


**Figure 6.7.** Schematic diagram of a single wafer cleaning tool. FFU is the filter fan unit. Used with permission of CT Associates, Inc.

megasonic energy. A schematic diagram of a single wafer cleaning tool that allows independent cleaning of both sides of a wafer is shown in Figure 6.7.

The chemicals used in these systems are typically dispensed onto the wafer surface residing there for only a short period of time and then are sent to reclaim or to drain. Hence, unlike recirculating immersion tools, any contaminants released from the wafer are swept away and do not need to be removed from the chemical in the tool. Particle concentrations in the chemicals can be controlled by supplying the chemicals from properly designed bulk chemical delivery systems and proper selection of system components. Extraction of dissolved contaminants (both metallic and organic) can be controlled by proper selection of system components. Components are constructed of materials and qualified using procedures that are similar to those for recirculating etch baths. However, because these systems use a chemical in a single pass, the contact time between the chemical and the hardware components is reduced and contaminant extraction is less likely than their bath counterparts. Particle concentrations are usually controlled by using chemicals supplied from high purity BCD systems. At the point-of-use filters can be used for additional particle control.

Recirculating batch spray tools are also used in wafer cleaning. Their requirements are similar to single wafer tools. Filters may be optimized for recirculation tools by taking advantage of multiple pass efficiencies versus single pass filters

used for spray and single wafer tools where the efficiency must be higher since there is only single pass of the chemical.

### 6.3.3 Wafer Drying

Wafers must be dried following the final rinse before subsequent processes can be performed. Two technologies are commonly used: rotational-drying and isopropyl alcohol (IPA)-assisted drying. Once again, proper chamber design and component selection are important in controlling contamination during drying. To prevent carryover of particles by the IPA vapor, the IPA is typically filtered as a liquid prior to vaporization into the nitrogen. In addition, filters can be utilized in the IPA saturated nitrogen gas to prevent particle deposition on the wafer to be dried.

## 6.4 Contamination Control Metrology

Contamination control continues to be a challenge with more stringent requirements for particle and metals. Consequently, the methods to minimize these contaminants and measure ever lower levels of the contaminants continue to push the state-of-the-art capabilities. These contaminants can have serious effects on devices causing electrical faults and patterning failures. It is therefore important to have the metrology tools and methods available for on-line or off-line measurement when higher level of contamination is detected so that diagnosis of the source of the contamination in a timely manner is possible to minimize the impact of the excursion on the manufacturing wafer yield.

### 6.4.1 Particle Measurement for Chemical Fluids

Of all the types of contaminants found within high purity chemical blending and delivery systems, particles have the highest potential for being introduced from the components within the system. For example, degradation of components or particulate-generating components such as pulsating pumps and valves with internal abrading surfaces (*e.g.* ball valves) can add particles to the chemical fluid. Filtration can greatly reduce the particle level within a chemical. Liquid-borne particle measurement analyzers within the chemical system can be used to measure the particle concentration in the chemical as it travels through the chemical delivery system to the point-of-use. Particle measurement is also used to monitor the efficiency of the filtration steps and to detect when filter breakthrough occurs.

#### *6.4.1.1 Particle Measurement Methods*

There are two liquid particle measurement methods that are used in the industry – optical particle counting (OPC) and scanning electron microscopy (SEM) particle counting. The particle measurement method used will depend on the nature of the chemical monitored and the type of information desired. Particle counting and defect metrology is thoroughly discussed in [1].

*Optical particle counting*: Monitors have been used to determine the concentration of particles in liquids for some time [12]. Optical particle counters detect and size particles by measuring the amount of light scattered by individual particles as they pass through a beam of light. The intensity of the scattered light is proportional to the size of the particle – smaller particles scatter less light [13]. See Figure 6.8 for a graphical illustration of how an OPC functions. Optical particle counting monitors are commercially available and can be installed in BCD systems to monitor the particulate level of the liquid. Two types can be used: an OPC with a vacuum-pressure sampler to draw a chemical from an atmospheric source (such as a drum or a bath) and then pressurize the chemical through an OPC to measure the particulate level in the chemical; and an OPC which is installed on a pressurized BCD sample port to measure the liquid particulate level directly. The number of particles detected over a period of time divided by the volume of chemical flowed through the measurement area of the light beam during the monitoring time yields the particle concentration in the fluid. Figure 6.9 shows typical particle size distributions (PSD) for different high purity chemicals measured by OPC. The slope of the distribution can be an indicator of the effectiveness of the filtration across the particle size distribution or the presence of microbubbles. A steeper slope in the PSD for the smaller size particles on the log-log chart would indicate less filtration of the smaller particles. A flattening of the slope in the PSD in the larger sizes could indicate presence of microbubbles, differentiated from the expected slope due to normal

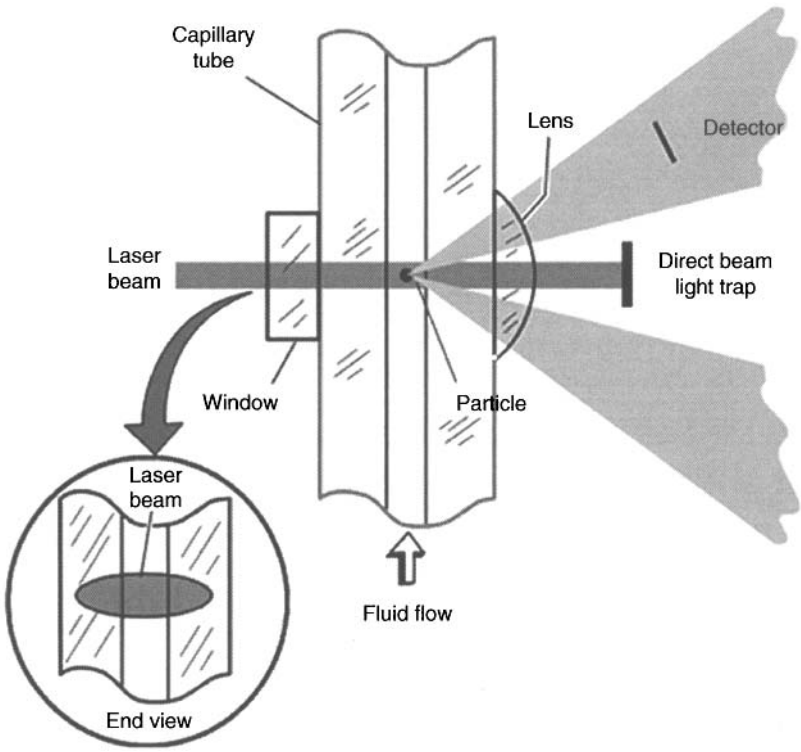


**Figure 6.8.** Graphical illustration of how an optical particle counter functions. Used with permission from Particle Measuring Systems.

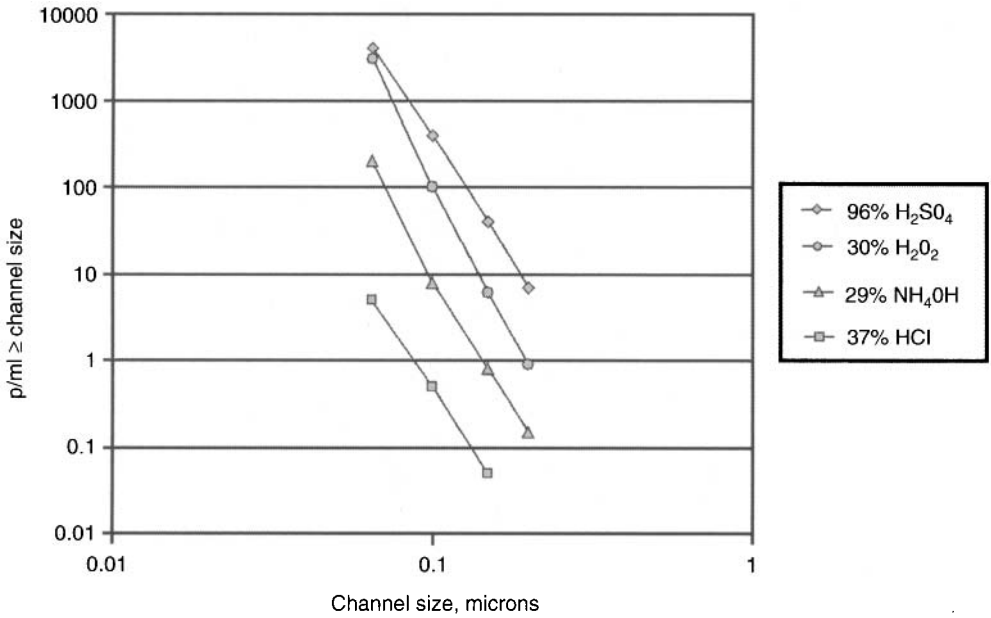


**Figure 6.9.** Typical production-line particle size distribution for various high purity chemicals. Used with permission from Intel Corporation.

particle distributions. Microbubbles can occur from the evolution of oxygen gas in 30 wt% $H_2O_2$, ammonia gas in 29 wt% $NH_4OH$, hydrochloride gas in 37 wt% HCl, or in liquids where dissolved gas becomes super-saturated upon depressurization.

*Scanning Electron Microscopy*: SEM particle counting consists of installing a disk filter on a pressurized BCD sample port and then directing the chemical flow through the filter to collect particles on the filter surface [14]. The disk filter media is a flat surface designed to collect the particles so that they can be seen by SEM analysis. A depth-type filter media cannot be used since the particles can be embedded in the pores and therefore not visible on the filter surface. The pore size of the disk filter must be chosen to trap the size particles of interest, for example, particles close to the pore size of the filters in the BCD system are used to check the filtration efficiency. For example, if a 0.5 μm "absolute" filter is being used in the BCD system, then the desired pore size for the SEM disk filter should be near 0.05 μm to be able to effectively monitor BCD system filtration performance. After sufficient chemical has flowed through the disk filter, the filter is then removed and analyzed by SEM to count the number of particles of a certain size range on the filter surface. The background level of particles on a new filter must be subtracted to determine the net particles added from the fluid. The number of particles divided by the volume of fluid flowed through the filter media yields the particle concentration in the fluid. Figure 6.10 shows a typical SEM photo – note the uniform sized pores in the filter media.

An advantage of OPC is that it provides real-time, continuous particle-level monitoring of the operating BCD system and is less subject to background contamination by the sampling method. Advantages of SEM are that it is not prone to interference by microbubbles. Optical particle counters cannot differentiate

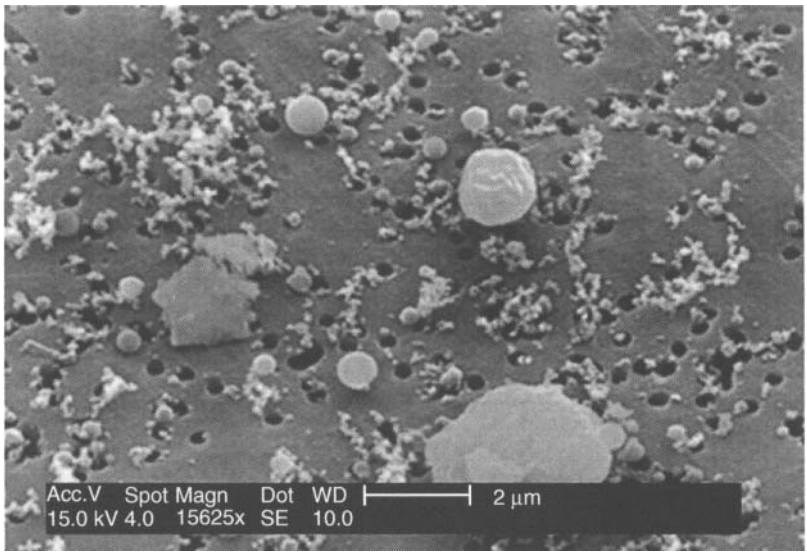


**Figure 6.10.** Scanning electron micrograph photo of disk filter surface showing collected particles [14]. Hugo M. Ortner, *Journal of Environmental Monitoring*, 1999, (4), 273–283 – Reproduced by permission of The Royal Society of Chemistry (RSC).

between a microbubble and a particle. Although it is possible to evaluate the distribution for evidence of microbubbles, the individual counts will not indicate if the count is due to a microbubble and therefore can lead to incorrect high counts even though particle concentrations are lower. In addition, the SEM can be coupled with energy dispersive x-ray (EDX) to provide elemental analysis of the particles collected on the filter surface. However, SEM usually requires a longer time to collect a sufficient number of particles on the filter surface and, therefore, is not as useful for detecting excursions. Hence, OPC is the method that is predominantly used in the semiconductor industry unless additional information on the particle morphology (shape) or composition is desired in which cases SEM is employed.

There is an issue with OPC – the particle monitoring sensor is typically calibrated with polystyrene latex (PSL) beads of particular spherical size to adjust the sensitivity of the detection circuit. However, since the refractive indices of real life particles are different than PSL and particles are not typically spherical in shape, sizing of the real life particles may be distorted. In addition, differing calibration methods for different OPC models and manufacturers can result in inconsistent particle readings in the same fluid. Therefore, development of chemical purity specifications must be established using only one type of OPC detector and sampling method, and this will lead to a repeatable and consistent chemical particle-level baseline and process of record for particle monitoring.

The selection of the right OPC for the application is critical. Usually, the level of sensitivity of the OPC is desired to be just above the size rating of the filters. This enables the OPC to detect defective filters and filter breakthrough. Due to the advancement in filtration technology, the sensitivity of OPC systems available on the market may not be sufficient to detect particles as small as the filter's removal rating. The OPC then becomes a gross filtration performance monitor useful for detection

of larger, more concentrated incoming particle contamination that encroaches into the distribution system and for detection of other component degradation in the BCD system.

Due to the relatively low sample volume of high-sensitivity OPC systems, longer sample times are often necessary to gather data for very high-purity (low particle-concentration) chemicals. It is important to generate sufficient "real" particle detection data above the electronic noise background of the OPC to generate statistically meaningful particle data. This can reduce the "real-time" aspect of the in-line OPC to detect particle excursions in the BCD system such as filter breakthrough.

#### *6.4.1.2 Particle Sampling Locations*

Table 6.2 shows particle sampling locations through the chemical system and the relative value of the information from each sample location. Cost generally limits the application of OPC systems to the most informative sample locations. The most common location for particle monitoring in the BCD system is at the post-filter/tool outlet which indicates the cleanliness of the chemical after filtration is performed. If high purity components are used with proper system design, the BCD distribution system adds relatively few particles to the chemical on its way to the fab tool. Particle monitoring is usually limited to bulk chemicals used for the most particle sensitive wafer processing steps such as gate pre-clean and lithography chemicals. Chemical producers typically measure the particulate contamination level of the chemical as it is being packaged although the particulate level in the chemical upon use will be higher due to particle generation from the container over time. Also, particulate concentration on the wafer is often measured as an off-line wafer metrology test and is related to process bath purity, along with other particle sources.

### 6.4.2 Chemical Purity of Chemical Fluids

Like particles, dissolved contaminants in chemicals must be controlled. Dissolved contaminants can be divided into two categories: inorganic and organic. Inorganic contaminants can be further divided into elemental and ionic [15]. Although both inorganic and organic contaminants can be detrimental, control of inorganic contaminants is considered more critical [16].

Historically, specifications for chemical purity have required increasingly lower concentrations of critical inorganic contaminants. Present specifications require that concentrations of critical contaminants be less than 150 ppt [17]. The list of critical contaminants varies with chemical type. This level of cleanliness is believed to be sufficient through 2015 [17]. However, there is a trend toward specifying contaminant concentrations within a specified set of limits rather than just below a maximum to improve process consistency [16].

Unlike particle contamination that can be reduced in delivery and process equipment by filtration, few options are available for reducing dissolved contaminants. Hence, the equipment must be designed to add little, if any, contamination. In addition, in-line instrumentation to monitor contaminant concentrations

**Table 6.2.** Liquid particle sampling locations in a BCD system.

| Particle Sample Location | Purpose |
|---|---|
| Feed chemical | Measure incoming particulate contamination level; detect high particle concentrations due to elevated contamination for different lot or feed containers. |
| BCD tool pre-filter | Measure particulate contamination level before filtration; indicates particulate load on filter. |
| BCD tool post-filter/tool outlet | Measure particulate contamination level after filtration/outlet of BCD tool; post-filter *vs.* pre-filter particle level indicates particle removal efficiency of the filter. |
| Fab tool point-of-connection | Measure particulate contamination level after chemical has traveled through most of the BCD distribution system; at the point the chemicals enter the process equipment. |
| Fab tool point-of-use/chemical bath | Measure particulate contamination level within the wafer bath after the chemical has traveled through the fab tool plumbing; bath particulate contamination level is affected by particle contribution of other the chemical constituents, chamber and plumbing particle contribution, and wafer carrier particle contribution. |
| Fab tool pre-filter | Measure particulate contamination level before filtration; indicates particulate load on filter. |
| Fab tool post-filter | Measure particulate contamination level after filtration; post-filter *vs.* pre-filter, indicating particle removal efficiency of the filter. |

in chemicals, other than UPW, has limited availability, further amplifying the need for the equipment to add minimal contamination.

### *6.4.2.1 Inorganic Contaminant Measurement Methods*

Inorganic contaminants in chemicals are typically measured using a combination of high resolution ICP-MS and ion chromatography [18]. ICP-MS is used to measure concentrations of individual elemental species while ion chromatography is used to measure ionic species. In ICP-MS, inductively-coupled plasma is used to produce ions that are then separated and detected using a mass spectrometer. In ion chromatography, molecules are separated based on their charge

characteristics. These techniques are capable of measuring concentrations from 50 to <1 ppt depending upon the contaminant and chemical being tested [18].

#### 6.4.2.2 *Inorganic Contaminant Sampling*

Since in-line measurement of inorganic contaminants is generally not available, grab samples are taken and sent to a laboratory (either on- or off-site) for analysis. Care must be taken to ensure that the sampling method does not contaminate the samples prior to analysis. In particular, sample bottles that exhibit very low extraction rates must be used. Bottles constructed of PFA that have been cleaned using either nitric acid or hydrogen peroxide typically are used.

Sampling locations in the chemical handling and cleaning equipment are similar to the particle counting locations as described in Table 6.3. In general, only limited sampling is performed due to cost constraints. Incoming chemical quality is typically measured by the chemical manufacturer and certified that it meets specifications, thus it may not be monitored at the fab. Also, only the chemicals used in processes that are deemed most critical (*e.g.* pre-gate clean or via clean) are routinely monitored and only at selected locations. However, monitoring all of the sample locations as listed in Table 6.3 can be useful in determining the source of contamination if system upsets occur.

### 6.4.3 Chemical Handling System Component Purity

Since chemical handling equipment cannot remove dissolved contamination, it is critical to properly select the components used in the assembly of the chemical systems to minimize additional contamination. Since many of the critical contaminants of concern are metals, components that do not use metallic sub-components are highly desirable. In components (*e.g.* valves and pumps) where the use of

**Table 6.3.** Contamination sampling locations in chemical handling systems.

| Sampling location | Purpose |
|---|---|
| Feed chemical | Measure incoming contamination concentrations; identify high incoming concentrations before the chemical enters the BCD system. |
| BCD tool outlet | Determine if the BCD tool is adding contamination and subsequently identify and eliminate contamination source. |
| Fab tool point of connection | Determine if the BCD distribution plumbing is adding contamination and subsequently identify and eliminate contamination source. |
| Fab tool point-of-use chemical bath | Determine contamination concentrations to which the wafers are exposed during processing; bath concentrations are effected by incoming concentrations as well as wafer/carrier contributions. |

metals may be necessary, such as valve stems or pump shafts, components should be selected that require two or three levels of internal failure before contamination of the chemical from exposure to the metallic sub-component can occcur. Leak ports that allow detection of failure prior to chemical contamination from these sub-components are desirable.

Components are often tested to ensure that they have sufficiently low contaminant extraction rates [11]. In addition, assembled systems can be qualified by filling the system with chemical, circulating the chemical and monitoring contamination concentrations over time to determine contaminant extraction rates [19].

## 6.5 Effects of Contamination

Delivering absolutely pure chemical to the wafer processing equipment is impossible since some levels of contamination will always be present. The goal is to minimize the concentration of critical contaminants to levels that do not significantly affect the wafer process. The role of contaminants in wafer processing can be broken down as follows:

1. Contaminants in the process fluid being transferred to the surface of the wafer;
2. Contaminants removed from the wafer surface in subsequent cleaning steps in the wafer process; and
3. The effects of the remaining contaminants on wafer yield and circuit reliability.

Contaminants deposited on wafer surfaces can affect electrical integrity, patterning, adhesion, and surface roughness. These will cause defects in subsequent processing steps, and could also have long term effects on final device integrity.

These three categories are discussed by type of contaminant; particle, ionic/metallic, and organic, in the following sections.

### 6.5.1 Particulate Contamination

Surface particulate contamination is one of the primary reasons for yield problems in the IC industry. The adhesion forces of small particles are greatly affected by the charged nature of the wafer surface (*i.e.* how strongly the particles "stick" to the wafer surface by van der Waals forces). Bakhtari, Park, and Busnaina summarize the deposition and adhesion processes of particles on wafer surfaces [20]. Through electrostatic forces, particles can be attracted to the wafer, and once adsorbed, are difficult to remove in subsequent cleaning steps. Therefore, it is critical to minimize the particle concentration in the process chemical so that the wafer is exposed to as few particles in solution as possible during wet processing. Figure 6.11 shows an example of an integrated circuit feature with particulate contamination. Clearly the presence of the particle can interfere with the electrical performance of the circuitry.

Table 6.4 shows the International Technology Roadmap for Semiconductors (ITRS) 2008 liquid chemicals particulate level purity targets [17] for the key

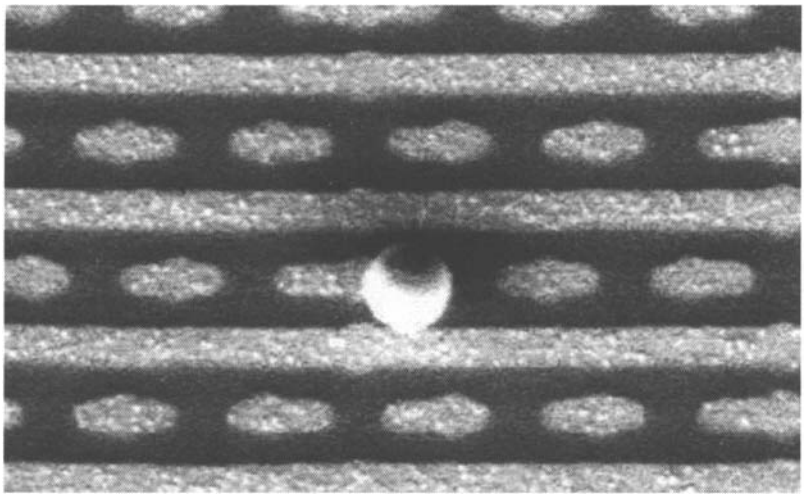

**Figure 6.11.** Scanning electron micrograph photo shows a wafer surface with particulate contamination that may adversely affect the electrical conductivity. Used with permission from Intel Corporation.

**Table 6.4.** ITRS 2008 liquid chemicals particulate level purity targets [17].

| Liquid chemical | Particles/ml > 0.065 μm |
|---|---|
| 49 wt% HF | 10 |
| 37 wt% HCl | 10 |
| 30 wt% $H_2O_2$ | 10 |
| 29% $NH_4OH$ | 1000 |
| 100% IPA | 1000 |

chemicals typically used in the gate pre-clean process – acidic, basic, and oxidizing chemicals. The wafer surface in an acidic environment develops a positive surface charge due to adsorption of hydronium ions ($H_3O^+$). Since small particles in solution tend to have a negative surface charge [21], they will be attracted to the positively charged wafer surface and be more inclined to adsorb onto that surface. Therefore, the tightest particle limits for cleaning chemistries are for HF, HCl, and $H_2O_2$ that are used in the acidic cleaning solutions. The wafer surface in a basic environment develops a negative surface charge due to the adsorption of hydroxyl ions repelling the negatively charged particles in solution, keeping them in solution, and preventing their adsorption onto the wafer surface, described in [20]. Particles in an IPA vapor or surface tension dryer remain in the chemical delivery canister and not in the vapor where the wafer is located.

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# PART 2
# APPLICATIONS

7

# Cleaning Challenges of High-κ/Metal Gate Structures

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*Abstract*

High-κ/metal gates are used as transistors for advanced logic applications to improve speed and eliminate electrical issues associated with polySi and $SiO_2$ gates. Various integration schemes are possible and will be discussed, such as dual gate, gate-first, and gate-last, both of which require specialized cleaning and etching steps. Specific areas of discussion will include cleaning and conditioning of the silicon surface, forming a high-quality chemical oxide, removal of the high-κ dielectric with selectivity to the $SiO_2$ layer, cleaning and residue removal after etching, and prevention of galvanic corrosion during cleaning.

*Keywords:* high-κ/metal gate, metal gate electrode, dual metal gate, high-κ gate dielectrics, gate-first, gate-last, high-κ removal, interfacial oxide, chemical oxide, galvanic corrosion

## 7.1 Introduction and Overview of High-κ/Metal Gate Surface Preparation

Reducing dimensions of a metal oxide semiconductor field effect transistor (MOSFET) requires a dielectric to replace conventional $SiO_2$ to accommodate the low voltage with low leakage current. The need to maintain electrical synergy between the gate and channel is an indirect motivation for the development of metal gate electrodes. Additionally, a tunable work function gate material is needed to replace the conventional poly crystalline silicon (poly-Si) gates – that are so highly doped they are almost as conductive as metal – to provide the necessary threshold voltage. Thus, high-κ/metal gate (HKMG) structures were developed to meet these needs.

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### 7.1.1 High-κ Dielectric Evolution

For years, silicon dioxide, with a dielectric constant (κ) of 4.2, was the mainstay gate dielectric material of the integrated circuit (IC) in MOSFET devices. The integration of $SiO_2$ was simple – grow an oxide from the already existing silicon substrate and make sure it was clean and defect-free before an oxidation step. As the thickness of the gate insulator shrank to maintain the required capacitance needed to meet lower voltage, high driving capability and produce faster circuits, the $SiO_2$ thickness was approaching the physical limit of a monolayer. Growing a very thin thermal oxide (<1.0 nm) is extremely challenging and as the gate layer thins, the reliability degrades exhibiting pinholes and electrical leakage, even with optimized processes.

Early researchers recognized that next-generation devices, starting at about 65 nm, would have serious issues that must be addressed such as: high gate leakage current, increased power consumption, poor time-dependent dielectric breakdown, reduced drive current, polySi-gate depletion, boron penetration, reliability degradation, and plasma process-induced damage [1, 2]. As the gate dielectric thickness decreases further for smaller than 50-nm devices, additional problems arise due to high tunneling current and reduced drive current. Green and coworkers suggested that these issues would prevent further scaling. They and others proposed that alternate gate dielectrics beyond $SiO_2$ were needed [1, 2]. By increasing the permittivity of the gate dielectric, the physical thickness of the gate may be increased providing reduced gate leakage current and enhanced transistor device characteristics with comparable device capacitance [3]. Various choices of dielectrics that could yield the requisite equivalent oxide thickness (EOT) are available, including $SiO_2$, $Si_3N_4$, Hf- and Zr-based compounds, and summarized in reference [4].

The EOT is calculated by the following equation:

$$\text{EOT} = 3.9/\kappa \tag{7.1}$$

where κ represents the physical thickness of the dielectric and interfacial layer. The required EOT for <50 nm devices is ≤1.0 nm; however, if the interfacial oxide is already 1.0-nm thick, there is no more thickness margin for high-κ layers.

Nitrided-gates, with a dielectric constant of approximately 6.5–7.2, although short-lived in the 1990's, provided a segue into high-κ dielectric films. They have been recognized as a film that prevents boron diffusion [5], can be formed with high reliability at a low thermal budget [1, 6], and lower gate leakage. However, tunneling occurs at the thicknesses required and leads to electrical issues. Several techniques exist to form oxynitride films, such as: thermally-grown oxynitride [5], nitridization with NO [7], rapid thermal processing (RTP) with a N-containing additive such as $N_2O$ [6] or $NH_3$, chemical vapor deposited (CVD) nitrides, silicon nitride grown with atomic layer deposition (ALD) [8], and other alternative processes that can also improve gate oxide reliabilities [1].

The evolution to high-κ dielectric materials was driven by the need to provide electrical characteristics of high carrier mobility with low permeability, high capacitance and an acceptable band gap to silicon [9] to reduce tunneling [10].

The physical characteristics that must be met are thermodynamic stability with high interface quality and low roughness, film morphology that is integratable with silicon. Most of all, these films must have high reliability and low gate dielectric leakage. The film must be easily deposited or grown in sufficiently thin, noncrystalline layers with good uniformity. This film must be manufactured in high volume, compatible with existing materials and processes used for IC devices. Additionally, the film should not react with the substrate to form silicates or silicides, have minimal $SiO_x$ or other interfacial material, and the film should not surrender oxygen atoms to the substrate or gate electrode. In general, the interfacial properties of the high-κ material with the silicon substrate are critical. In order to meet the future requirement for sub-nm interfacial thickness on a gate stack, the following items will be required:

1. Good contact between high-κ and substrate. This requires good surface termination such as homogeneous hydroxyl groups.
2. No electron/hole mobility degradation with sub-nm thicknesses.

References [3, 11, 12] summarize the requirements for an effective high-κ dielectric material and review many of the proposed films.

Before being implemented in MOS gate structures, memory devices used high-κ materials for capacitors. Metal oxides, $Ta_2O_5$ and $Al_2O_3$ were the materials of choice, although hafnium-based high-κ materials were also in use and have now become the predominant capacitor dielectric. After nitride oxides surpassed their usefulness as gate dielectric materials, the evolution of high-κ began in 1999 when $HfSiO_x$ was introduced as a possible candidate [13] having dielectric constant 25 or greater. Although hafnium compounds, in particular $HfO_2$, HfO(N), and HfSiO(N), are the specific films in use, zirconium was also considered as a possible material [14]. Hafnium compounds are now used for the 22-nm node, the dominant high-κ dielectric for logic IC manufacturers.

### 7.1.2 Metal Gate Evolution

Gate electrode materials have been ever-changing. Early IC devices used metal gates, then there was a migration to silicon-based gates. Current technologies are returning to metal gates structures. The simple single gate structure for MOSFET devices have morphed into dual gate structures with each gate tuned to its work function for the channel. The threshold voltage is determined by whether the device is n- or p-type (NMOS or PMOS).

PolySi gate electrodes can have their work function modified by doping the semiconductor to obtain the desirable threshold voltages; however, metal gates cannot be so easily tuned. For highly doped polySi gate electrodes, upon applying a bias, a ~0.5-nm thick depletion region forms and contacts the insulator, adding to the EOT, and thus reducing coupling [15]. As the gate oxide thickness is scaled below 2 nm, this depletion region becomes a significant part of the EOT. In metal gate electrodes, however, this depletion region is almost nonexistent. Hence, the use of metal gate electrodes allows thinner EOT to be attained. Also, replacing polySi with metal gates that have near-silicon band edge work functions

can overcome problems with boron penetration and Fermi level pinning [16]. The change in the electrode series capacitance dictates the use of a material that reduces the capacitance as the gate oxide thins to less than 1-nm EOT. Channel mobility is also an issue when using high-κ dielectrics; metal gates eliminate this problem [17] while also addressing the capacitance requirements.

Schaeffer and coworkers have modeled the optimal gate work functions for the <50 nm devices. They postulated this value should be 0.2 eV below the conduction band of silicon for n-type MOSFET and 0.2 eV above the valence band for p-type MOSFET [18]. They have evaluated TiN, TaSiN, and WN gate electrodes although the actual work function is also dependent on the gate insulator material [19]. Many other researchers have determined the acceptable value for the work function with Cheng *et al.* summarizing the results at approximately 4.1–4.4 eV for NMOS and 4.8–5.1 eV for PMOS [20].

Researchers recognized a need for a new gate electrode that could satisfy dual work function requirements for <50 nm channel length logic devices combined with a high-κ gate dielectric. Substantial efforts have been made to replace polySi gates with metal gates [21–23] including fully integrated HKMG [24]. Many transition metals, react with $SiO_2$ at elevated temperatures to form metal silicide and metal oxide layers [25, 26]. Use of high-κ gate dielectrics with the metal gate avoids these unwanted reactions. Metal gates with high-κ gate dielectrics can be more easily integrated into the manufacturing process than polySi gates with high-κ gate dielectrics. Temperatures, >1000°C, that are needed to activate the polySi gate can degrade the performance of the high-κ dielectric [27, 28]. Materials selected to try first were ones already developed for IC manufacturing, such as the barrier metal for Cu, Al, and W processing. Candidates included TaN, TiN, and TaSiN [29], and some other films such as Ti [30], Mo [31], and Ni for FUSI devices [32], plus others.

At the same time, different techniques had been tried to successfully implement dual metal gate CMOS [33–37]. A metal wet etch-based integration scheme proposed leaving one of the metals intact (low work function), and then depositing a second metal (high work function) on top of the first metal, then etching back the metal in the areas requiring the low work function [29, 30]. One early method involved depositing one metal, patterning it, and then etching the second metal [31, 38], called gate-first. The first metal should preferably have a high etch selectivity over the gate dielectric so that the dielectric is not significantly damaged when the metal is etched. However, metal wet etch remains a challenging task [29, 31] as exposing the gate dielectric to metal etching chemistry causes undesirable thinning and potential gate dielectric damage [29, 31]. Although a highly selective metal wet etch module has been developed [41], devices with the desired electronic performance have not yet been demonstrated.

Furthermore, integration of metal gates proved difficult because exposure of the sensitive high-κ layer to blanket etching could damage the film and etching two critical lithography layers was expensive. The metal gates, using traditional patterning process of photolithography followed by etching, must withstand high temperature processing, typically >1000°C.

Various integration schemes were proposed. The replacement gate, also called gate-last, is an integration scheme where a dummy polySi gate is replaced with metal gates [42–44]. Other researchers have developed silicided gate electrodes, such as

fully silicided metal gate (FUSI) [32]. An integration scheme – dual high-κ dual metal gate CMOS – has been developed to demonstrate devices for 45-nm low standby power node applications [45], even so, this integration scheme encounters some challenges inherent in a conventional deposition-etch-deposition based dual metal gate CMOS flow. Electrical characterization results show a symmetric short channel threshold voltage, $V_t$, of ~ ± 0.45V with ~80% high field mobility for both N and PMOS and significantly lower gate leakage compared to polySi gate and silicon oxynitride dielectric gate stack. Also, in the quest for improved electrical performance, a dielectric capping layer has recently been introduced to achieve a significant shift in the threshold voltage of metal gate devices toward the silicon conduction band edge. Also, well behaved short channel devices have been demonstrated with aluminum oxide ($Al_2O_3$), gadolinium oxide ($Gd_2O_3$), and lanthanum oxide ($LaO_x$) [45–47].

## 7.1.3 High-κ/Metal Gate Integration and Structures

Integration of metal gate materials with the high-κ dielectric materials require that they be compatible with one another at subsequent processing steps and, for long term reliability, they must not interact. Although by no mean a standard process, many companies have adopted HfSiO(N) gate dielectrics and TiN and Ta gate electrodes. For example [48] and some companies are using a gate-first [49] or gate-last approach [50], and possibly the FUSI process already mentioned [32]. Recently, a hybrid approach combining both gate-first and gate-last was disclosed [51].

### *7.1.3.1 Gate-First Process*

The gate-first process, also called the metal inserted polySi stack (MIPS), is desirable because it follows the process flow used in traditional IC logic MOSFET processing where the gate electrode is defined by a lithography and etching step followed by self-aligned source/drain (S/D) implants. However, this integration scheme restricts the choice of high-κ dielectric and metal gate materials as they must be able to be etched.

Various process flows are used for gate-first integration schemes [49, 52]. A generalized process is outlined in Table 7.1. For examples, in the gate-first approach explained in reference [33], the process first cleans and deposits the high-κ, metal gate, and polySi gate-capping layers followed by a gate stack etch to define the critical dimension (CD). Gate formation is followed by halo implantation of the S/D extension, offset spacer formation, deep S/D implantation, S/D high-temperature rapid thermal anneal (RTA), and S/D silicide formation. Conventional contact and metal-layer steps complete the process. This process is similar to conventional MOSFET processes, with the substitution of high-κ for $SiO_2$ dielectric and the use of a metal gate. The polySi capping layer helps to integrate the metal gate into the conventional process.

Figure 7.1 depicts one integration scheme for gate-first using dual metal deposition and wet etch-back of the first metal. Figure 7.2 shows transmission electron microscopy (TEM) images of NMOS and PMOS transistor metal gate stacks with a high-κ gate dielectric from the same complimentary MOS (CMOS) device. The TaSiN was removed from the PMOS transistor before Ru was deposited. Some

scheme with metal 1 etch-back.

| |
|---|
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 1 deposition |
| Hardmask deposition |
| Hardmask pattern |
| Hardmask etch |
| Hardmask photoresist strip |
| Hardmask post-strip clean |
| Metal 1 etch and clean |
| Hardmask removal |
| Pre-metal 2 clean |
| Metal 2 deposition |
| PolySi (or α-Si deposition) |
| Metal 1 and 2 electrode pattern |
| Metal 1 and 2 etch |
| Metal 1 and 2 photoresist strip |
| Metal 1 and 2 post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |

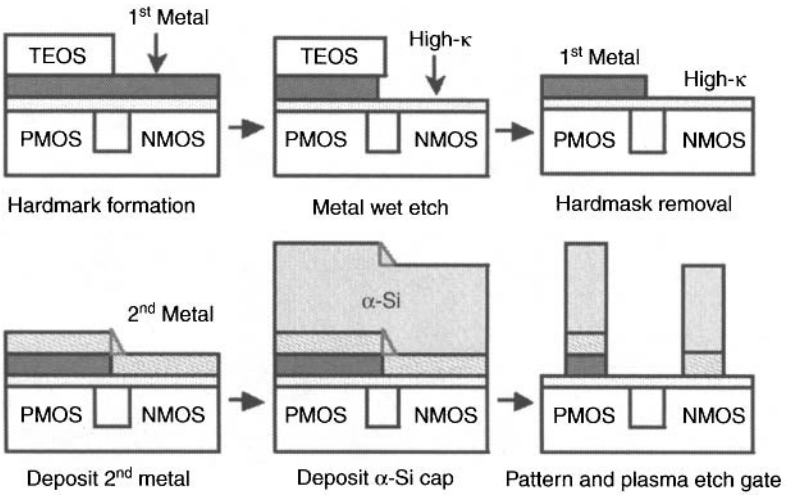



**Figure 7.1.** Schematic of the dual gate-first process flow using metal wet etch for removing the first metal layer (αSi is amorphous silicon) [52]. Reproduced with permission of ECS – The Electrochemical Society from Zhang, Z., Song, S. C., Huffman, C., Hussain, M. M., Barnett, J., Moumen, N., Alshareef, H. N., Majhi, P., Sim, J. H., Bae, S. H., and Lee, B. H., *Electrochemical and Solid State Letters*.

of the steps in Table 7.1 have been simplified such as the spacer formation and implants to focus on the important steps pertaining to HKMG cleaning and surface conditioning. Figure 7.3 shows the finished HKMG structure with the gate-first process.

### *7.1.3.2 Gate-Last Process*

The replacement gate (RPG) processing has been proposed as a method to retain the junction profiles and small gate widths for many years before the use of HKMG [53] [54]. The replacement gate process, also called disposable gate, replacement gate, damascene gate, or the gate-last process, requires a chemical mechanical polishing step and an etching process to remove the sacrificial gate materials [50]. However, because the high temperature implant drive is performed before the

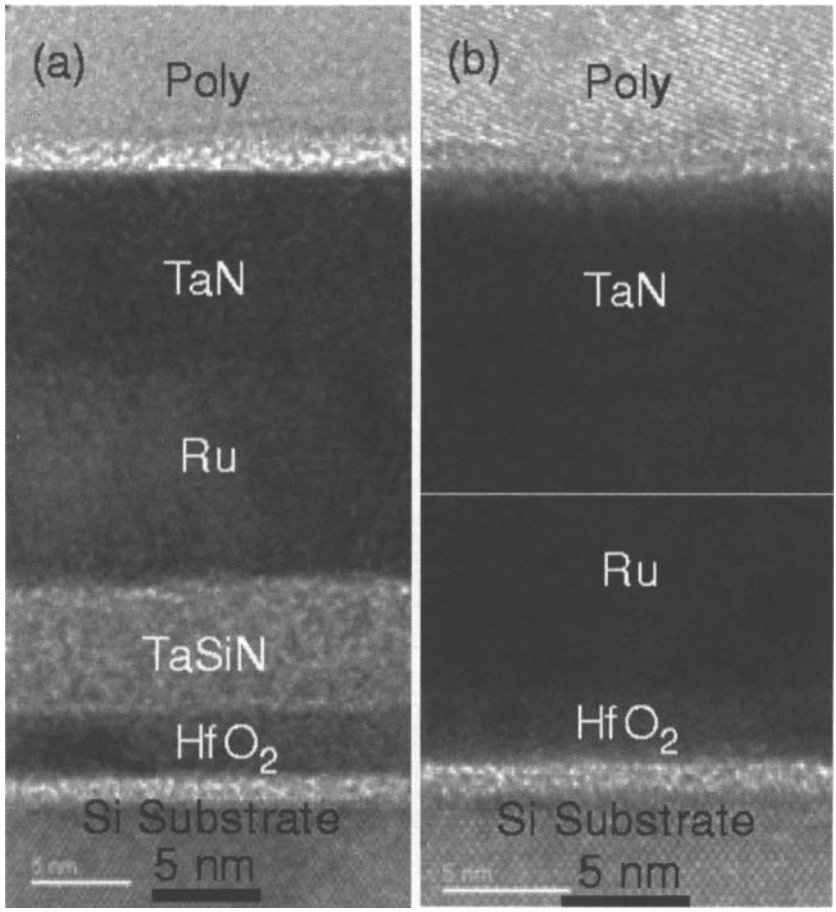



**Figure 7.2.** Cross section TEM images of dual metal gate a) NMOS and b) PMOS gate stacks structures from the same CMOS device [52]. Reproduced with permission of ECS – The Electrochemical Society from Zhang, Z., Song, S. C., Huffman, C., Hussain, M. M., Barnett, J., Moumen, N., Alshareef, H. N., Majhi, P., Sim, J. H., Bae, S. H., and Lee, B. H., *Electrochemical and Solid State Letters*.

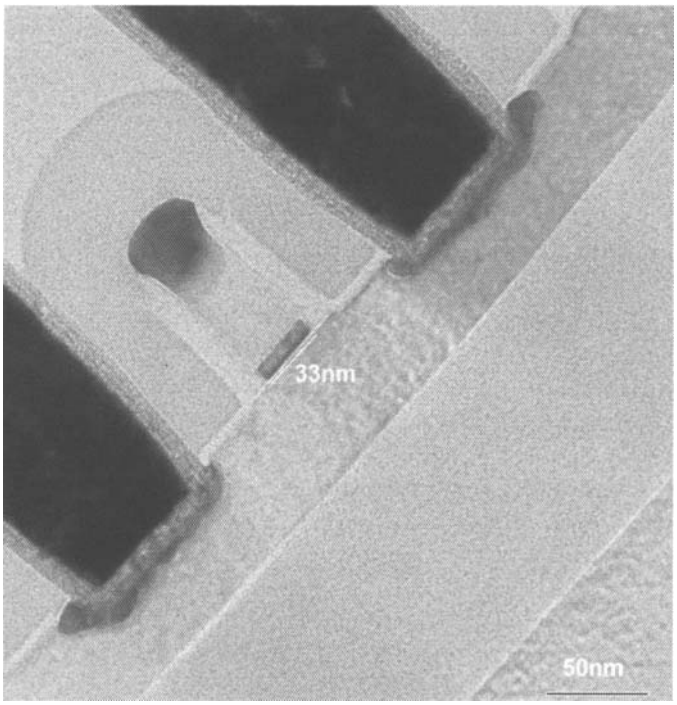



**Figure 7.3.** Cross section TEM image of a 32-nm HKMG using the gate-first integration scheme showing minimal loss of the substrate [49]. Used with permission of Chudzik, M., Doris, B., Mo, R., Sleight, J., Cartier, E., Dewan, C., Park, D., Bu, H., Natzle, W., Yan, W., Ouyang, C., Henson, K., Boyd, D., Callegari, S., Carter, R., Casarotto, D., Gribelyuk, M., Hargrove, M., He, W., Kim, Y., Linder, B., Moumen, N., Paruchuri, V. K., Stathis, J., Steen, M., Vayshenker, A., Wang, X., Zafar, S., Ando, T., Iijima, R., Takayanagi, M., Narayanan, V., Wise, R., Zhang, Y., Divakaruni, R., Khare, M., and Chen, T. C., *VLSI Symposium Technical Digest*. © 2007 IEEE.

deposition, a wider range of materials can be used for both the dielectric and the gate. The gate-last process flow can have some modifications based on the choice of materials and has the flexibility to use a wide range of materials both for the high-κ and gate electrode because of the individual processing steps for each deposition. Table 7.2 outlines the process flow for this integration scheme. For the integration scheme [34] first deposits and etches a sacrificial or dummy $SiO_2$/polySi gate stack. This is followed, the same as the gate-first approach, by the extension, spacer, S/D implant, S/D RTA, and S/D silicide steps. At this point an additional dielectric layer is deposited and resurfaced by chemical mechanical polish (CMP) stopping at the top of the dummy gate. Next, the dummy gate is removed and the final high-κ and metal layers are deposited, then CMP or a patterned etching step is used to remove the metal layer between the gate stacks stopping on top of the high-κ layer. Contact and metal layer complete the process.

Figure 7.4 depicts schematically the integration scheme for gate-last. Again, some of the steps in Table 7.2 have been simplified. Figure 7.5 shows TEM images of a NMOS and PMOS transistor fabricated with the gate-last integration scheme.

**Table 7.2.** Process flow for gate-last integration scheme.

| |
|---|
| Pre-dielectric deposition clean |
| Sacrificial gate oxide formation |
| Sacrificial polySi gate deposition |
| PolySi gate pattern |
| PolySi gate etch |
| PolySi gate photoresist strip |
| PolySi gate post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |
| Sacrificial metal 1 gate pattern |
| Sacrificial metal 1 gate etch |
| Sacrificial metal 1 gate removal |
| Sacrificial metal 1 gate photoresist strip |
| Sacrificial metal 1 gate post-strip clean |
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 1 deposition |
| Metal 1 and high-κ deposition CMP |
| Metal 1 and high-κ post-CMP clean |
| Sacrificial metal 2 gate pattern |
| Sacrificial metal 2 gate etch |
| Sacrificial metal 2 gate removal |
| Sacrificial metal 2 gate photoresist strip |
| Sacrificial metal 2 gate post-strip clean |
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 2 deposition |
| Metal 2 and high-κ deposition CMP |
| Metal 2 and high-κ post-CMP clean |

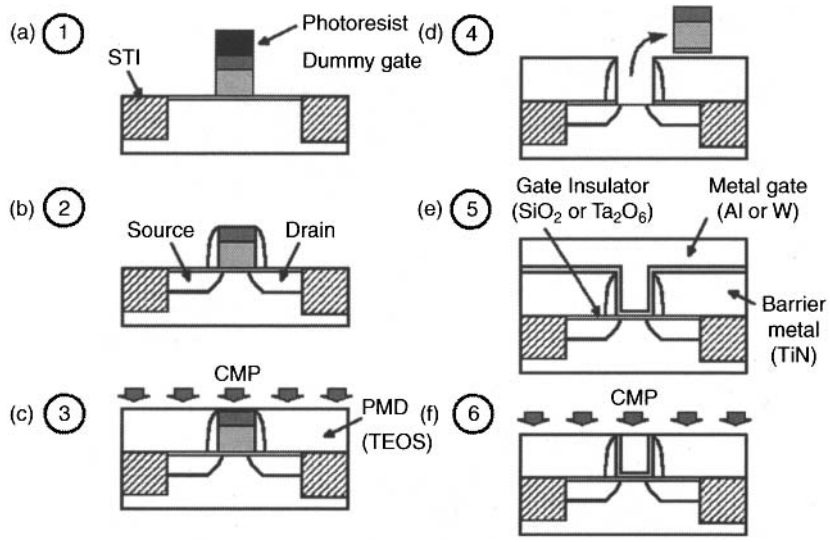



**Figure 7.4.** Schematic of the dual gate-last process flow with CMP step for defining the gate structures [42]. PMD is pre-metal dielectric. Used with permission of Yagishita, A., Saito, T., Nakajima, K., Inumiya, S., Akasaka, Y., Ozawa, Y., Hieda, K., Tsunashima, Y., Suguro, K., Arikado, T., and Okumura, K., *Transactions of Electron Deivces*. © 2000 IEEE.

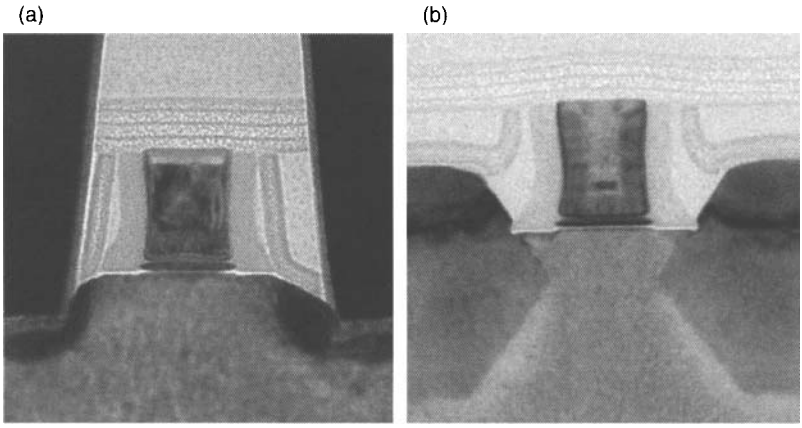



**Figure 7.5.** Cross section TEM image of a 45-nm HKMG using the gate-first integration a) NMOS and b) PMOS [50]. Used with permission of Auth, C., Cappellani, A., Chun, J.-S., Dalis, A., Davis, A., Ghani, T., Glass, G., Glassman, T., Harper, M., Hattendorf, M., Hentges, P., Jaloviar, S., Joshi, S., Klaus, J., Kuhn, K., Lavric, D., Lu, M., Mariappan, H., Mistry, K., Norris, B., Rahhal-orabi, N., Ranade, P., Sandford, J., Shifren, L., Souw, V., Tone, K., Tambwe, F., Thompson, A., Towner, D., Troeger, T., Vandervoorn, P., Wallace, C., Wiedemer, J., and Wiegand C., *VLSI Symposium on Technology*. © 2008 IEEE.

### *7.1.3.3 Comparison between Gate-First and Gate-Last Scheme*

A metal gate and high-κ dielectric can be integrated into the MOSFET with a gate-first or gate-last approach. These approaches primarily differ in whether the metal gate is deposited before or after the source/drain activation anneal. Table 7.3

**Table 7.3.** Comparison between gate-first and gate-last integration.

| | Gate-first Approach | Gate-last Approach |
|---|---|---|
| Pro | Compatible with conventional CMOS process<br>Fewer process steps<br>Potentially high yield | Low thermal process<br>More intrinsic high-κ and metal gate properties |
| Con | EOT and $V_t$ control issue<br>Halo implantation through metal gate | Need extremely conformal high-κ and metal gate process<br>Possible defect issue, lowering device yield<br>High fringing field issue<br>Previous silicide formation limits allowable subsequent high-κ/metal gate process |

summarizes the comparison between gate-first and gate-last integration schemes. When compared to the gate-last approach, the gate-first approach has the advantage of being compatible with the conventional CMOS process. Gate-first CMOS requires fewer and less-complicated process steps offering greater potential for high device yield. The primary disadvantage of the gate-first approach for high-κ metal CMOS is that the gate stack is subjected to the high-temperature S/D anneal. This presents several challenges. High temperatures can lead to crystallization of the high-κ dielectric; this increases gate leakage, makes the κ value non-uniform across the wafer, and causes intrinsic charge trapping and coulomb scattering issues. However, if a very thin high-κ layer is used, the transformation of the dielectric from amorphous to crystalline phase is kinetically suppressed [59], so an amorphous high-κ dielectric can be sustained through the high-temperature anneal process.

Another challenge is chemical reactions between the metal gate and high-κ during the anneal. If a chemically unstable metal gate is used, it reacts under high temperature with the high-κ dielectric resulting in a work function that differs from the metal's bulk properties. This issue can be avoided by using a thermally stable metal for the gate, but the choice is limited because metals that are chemically stable might not offer the desired work function. In some cases, however, a high-temperature anneal is actually required to enhance the interface dipole formation and set the appropriate work function [36]. There has also been concern that chemical reactions can increase the dielectric EOT, but that is not always true. Recent studies indicate that metal doped into the high-κ material can increase its κ value, particularly when a $HfO_2$ dielectric is used with a Ti or Ta-based metal gate [35]. Also, certain metal gate materials, such as TiN or HfSi, scavenge oxygen from the dielectric's bottom oxide layer [29], potentially decreasing EOT after the high-temperature process.

Another challenge posed by the high-temperature anneal is dopant diffusion. During the anneal, the boron dopant used in PMOS devices can diffuse from

the polySi cap through the metal gate, especially when a thin metal gate is used. Presence of boron in the gate cap is unavoidable in the gate-first process because the gate stack is formed before the dopant is implanted. Boron diffusion is a concern in high-κ processes because boron diffuses much faster in $HfO_2$ than in $SiO_2$ [39]. Boron atoms in the dielectric can degrade reliability by producing a charge that shifts the threshold voltage ($V_t$) [55]. However, B atoms produce a charge only where $SiO_2$ atoms are present in $HfO_2$, (i.e., Hf-silicate) [15]. The $V_t$ shift can be reduced by using the lowest optimal $SiO_2$ concentration in the HfSiO dielectric, even though more boron diffusion might occur. Boron diffusion can also be suppressed by using an amorphous phase metal for the gate, and also by doping the high-κ material with nitrogen.

The gate-first approach presents additional challenges because the HKMG stack must be etched before S/D implantation. Etching of the metal gate can be difficult, especially for high work function materials, which tend to be relatively noble (non-reactive) metals [38]. Furthermore, metal oxidized during dry etch processing can be difficult to remove. A high-temperature etching process is required and a combined dry and wet etch process may be needed to completely remove the etch residue.

Control of the gate CD is also an issue. Depending on the metal used, some undercut of the metal gate could occur because of isotropic etching. Other metals tend to form a metal foot at the base of the gate, below the polySi capping layer. The foot occurs because the slower etching rate of the metal allows polymer buildup on the gate sidewall, preventing etching through the polymeric layer. Any undercut or foot in the metal gate makes it difficult to control gate CD that is measured at the bottom of the gate stack, rather than the top. Undercutting can be avoided by using dry etching for metal removal, and formation of a foot can be suppressed by optimizing the dry etch process, especially etch chemistry that generates less polymer.

Another challenge is removal of the high-κ dielectric in the S/D area. The dielectric must be removed thoroughly to prevent any process induced charge effect [56] that can cause parameter drift and degrades performance. Section 7.4 discusses the removal of the high-κ dielectric. Hafnium dioxide is difficult to wet etch with HF chemistry once the $HfO_2$ is crystallized, but it can be wet etched if it is first subjected to physical bombardment. While HfSiO is easily etched by HF chemistry, the isotropic etch results in undercutting below the metal gate edge. The undercut is later filled with lower-κ material, such as nitride, which degrades device performance and reliability. High-κ dry etching processes also causes damage unless healed appropriately [57].

Finally, the metal gate-first approach presents integration issues with respect to angled implantation, such as halo implantation for the S/D extension. The metal of the gate stops ions that would normally pass through a polySi gate reducing the effective dose that reach the Si substrate. The implantation step also tends to sputter metal atoms onto the high-κ dielectric and Si substrate, possibly degrading performance and reliability. These issues can be avoided by depositing an offset spacer at the gate edge before halo implantation to prevent ions from striking the metal gate.

The gate-last approach offers the advantage of a low thermal budget process after the high-κ dielectric and metal stack are formed, thus, the resulting dielectric and metal gate properties will be closer to their intrinsic values. The gate-last approach allows CMP to be used for removing excess metal after the gate stack is finished, avoiding the need to etch the HKMG material. This is desirable when using a noble gate metal for which chemical etching is ineffective. The HKMG is formed in the trench left when the dummy gate is removed. The subsequent CMP removal is self-aligning because the gate CD had already been defined by the dummy gate. Any non-uniformity in the CMP process could leave some residual metal between the gates, shorting the devices. An alternative is to use a photolithography and dry etching process to remove the residual metal. In this case the gate CD is still defined by the dummy gate, but any offset or overlay in the top gate pattern might violate the gate-to-contact design rule.

The primary disadvantages of the gate-last approach are process complexity and small gate size. As the gate length and width are scaled, it becomes more difficult to remove the dummy gate completely and fill the gate hole evenly with the metal and high-κ gate materials. As more devices are integrated into a die, there is a greater chance of yield loss because of these issues. Typically, a wet etch is preferred for dummy gate removal because it is very selective and less damaging than a dry etch to the Si substrate. It is necessary to ensure enough overetch is applied to remove all the dummy gate residue.

Once the gate trench is cleared, a conformal process is needed to deposit the high-κ and metal gate layers. Use of physical vapor deposition (PVD) is restricted because of poor step coverage. Atomic layer deposition is preferred because it offers excellent step coverage, but the materials are limited by the available precursors. Another challenge of the gate-last approach is larger fringing capacitance caused by high-κ deposition on the gate hole sidewall. This high-κ material remains in place after the gate stack is complete increasing capacitance at the gate edge and potentially degrading the performance of the device.

The gate-last approach also limits the maximum process temperature allowed for high-κ/metal deposition and anneal to <500°C. Any higher temperature would degrade performance by increasing the sheet resistance ($R_s$) of the already formed NiSi on S/D area. This limitation can be avoided by forming the silicide contacts after the gate replacement step, but only at the cost of even greater process complexity.

### *7.1.3.4 Fully Silicided Process*

The FUSI process takes advantage of the ability to use polySi as the electrode material where silicide technology is used to form the transistor on both n- and p-channels. The FUSI electrodes can be used on either $SiO_2$, SiON, or HfSiO [58]. The metals that can be used are Co [32], Pt [59], with Ni being found to give the best electrical results [60]. Table 7.4 outlines the process flow for the FUSI integration scheme; Figure 7.6 depicts one such scheme using nickel as the metal. The

**Table 7.4.** Process flow for fully silicided gate integration scheme.

| |
|---|
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Sacrificial polySi gate deposition |
| PolySi work function tuning implants |
| PolySi gate pattern |
| PolySi gate etch |
| PolySi gate photoresist strip |
| PolySi gate post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |
| Silicide metal deposition (Ni) |
| First silicide anneal |
| Unreacted metal removal |
| Interlevel insulator dielectric deposition |
| Interlevel insulator CMP |
| Interlevel insulator post-CMP clean |
| Fully silicide anneal |
| Post-anneal clean |

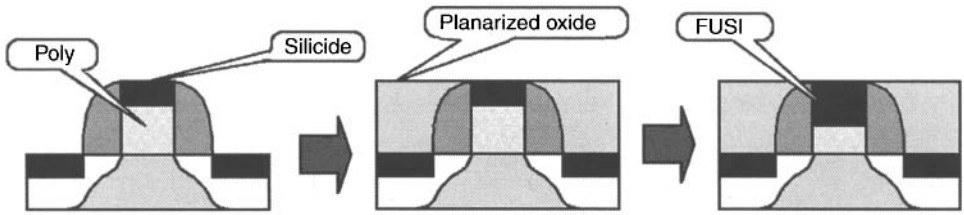



**Figure 7.6.** Schematic of the fully silicided gate process flow with CMP step prior to full silicidation [60]. Reproduced with permission of ECS – The Electrochemical Society from Maszara, W. P., *Journal of the Electrochemical Society.*

FUSI process relies on complete silicidation with a controlled silicide phase to achieve low threshold voltages. Again, some of the steps in Table 7.4 have been simplified. Although the FUSI is not a widespread technology, there is some indication of its use in volume manufacturing.

## 7.2 Surface Preparation and Cleaning

Current high-performance devices require transistor gate stacks to have an EOT, of ~1.0 nm at this thickness polySi gate depletion becomes an inevitable problem, solved by the introduction of metal gates. Since CMOS processing requires fabricating PMOS and NMOS on the same wafer, this necessitates different metal gates, plus potentially different high-κ materials and capping layers for each transistor type. In addition complex interface engineering is necessary between Si and high-κ.

Cleanliness and the proper condition of the silicon surface prior to formation of the interfacial oxide and deposition of the high-κ dielectric are critical. Due to the introduction of HKMG, the following cleaning processes are critical for pre and post-gate fabrication:

1. Pre-gate: Surface preparation and interface engineering – Section 7.2.
2. Post-gate: High-κ removal and post-gate etching clean – Section 7.3 and 7.4.

In this chapter, the items associated with cleaning are broken down step-by-step. This section will cover these pre-deposition cleaning and interface engineering.

### 7.2.1 Surface Cleaning Challenges Prior to High-κ Deposition

The HKMG stack has stringent requirements for surface preparation and cleaning. These same challenges were experienced with the standard polySi gate electrode and $SiO_2$ gate oxide structures. The most critical surface cleaning challenge for HKMG is the formation of a high quality silicon dioxide dielectric interface prior to the deposition of the high-κ dielectric.

This section will discuss the surface preparation and cleaning prior to interfacial oxide formation and the various methods of forming the interfacial oxide on silicon and also on germanium.

### 7.2.2 Pre-interfacial Oxide Formation Cleaning

High-κ layers, whether deposited by ALD or CVD, require a starting surface with a high density of hydroxyl group termination. Traditionally, SC-1 and SC-2 have been widely used for pre-gate cleaning [62]. These RCA cleanings are still promising processes; however, the fundamental problem is that SC-1/SC-2 forms a chemical oxide of 1.0~1.5-nm. Since this interface layer consumes most of EOT, the interfacial thickness must be minimized, typically <1.0 nm. Surface flatness and complete hydrogen termination are also desired prior to high-κ ALD.

Prior to formation of a chemical oxide, the silicon surface must first be freed of any native oxide and any organic contamination. In addition, all metal contamination must be removed, in particular mobile ions that can affect the gate oxide integrity (GOI). Especially lifetime-killer metals, such as Cu and Fe, must be removed as well as metals from the metal gate. To preserve GOI, gate metals must not diffuse into the silicon nor penetrate the gate oxide.

### 7.2.3 Interfacial Oxide Formation

Prior to atomic layer deposition of the high-κ film, the surface of the silicon must be free of defects and atomically smooth. Deposition of the ALD high-κ film directly onto the hydrogen-terminated silicon surface has been attempted to fabricate sharp Si/high-κ interfaces that are oxide-free and Si-H-terminated. Lab results have shown that good quality high-κ dielectrics can be formed, but at very low deposition rates with poor uniformity and, in some cases, with silicide formation [62]. Moreover, when directly compared to an oxidized surface, a Si-H terminated surface shows leakage [63]. Therefore, first attempts to produce high-κ stack on Si-H surfaces were not successful.

Several approaches have been considered for surface treatment prior to gate formation. Yamamoto *et. al.* proposed suppression of surface micro-roughness of silicon by the addition of alcohol into the water [64]. Choi *et. al.* showed that different cleaning methods, such as modified Shiraki clean and RCA clean, have different impacts on interface properties [65]. After high-κ integration, RCA-cleaning resulted in higher density of interfacial traps and thicker interfacial oxide thickness. A new or modified surface treatment was therefore required prior to high-κ formation.

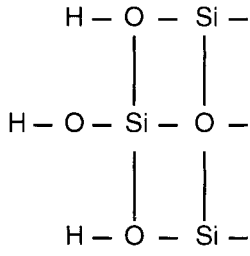
The entire cleaning sequence for successfully forming a high-quality oxide involves the use of traditional formulations to remove the organic, metallic, and particulate contamination on the wafer. Researchers at SEMATECH have used a standard RCA clean (SC-1/SC-2 – standard clean-1 and standard clean-2) with HF-last prior to an $O_3$-based oxidation in order to form the requisite interfacial oxide [66]. Instead of a traditional RCA clean for the surface preparation prior to high-κ deposition, dilute and lower temperature SC-1/SC-2 surface preparations have also been tried. Typically, prior to chemical oxide formation, wafers are etched using dilute HF (DHF) to remove 20 nm of thermal oxide [67]. Hydrochloric acid can also be added to the HF solution, or a separate SC-2 or dilute HCl rinse can be included [67].

In order to prepare the appropriate surfaces for high-κ deposition, different approaches or a combination can be used: chemical or thermal oxidization, etch-back of the oxide formed, and post-processing anneal, including densification and nitridization.

#### *7.2.3.1 Hydroxyl-terminated Surface*

Hydroxyl groups have been found to be necessary for rapid initiation of the ALD reaction on silicon [68]. Kukli and researchers have found that intermediates are formed by substitution of the hydrogen in the hydroxyl group with the ALD precursor molecule. When silicon is passived by chemical oxide (with –OH terminal groups) the ALD growth rate is faster than found on a hydrogen passivated surface. Additionally, the thickness growth rate is linear with respect to the number of ALD pulses [69]. Hydroxyl terminated surfaces can be on either a silicon substrate, with no intermediate oxygen bonding or on a thin silicon dioxide passivating layer. A thin hydroxyl layer is optimum due to the thickness limitation when trying to create an EOT of less than 1.0 nm. This is because the hydroxyl terminated silicon dioxide layer is itself only 1.0 nm thick. Table 7.5 shows the thickness of the oxide and the resultant impact on the ALD deposition.

**Table 7.5.** Termination of silicon surface and impact on ALD. Adapted from [69]. Reproduced with permission of ECS – The Electrochemical Society from De Gendt, S., Beckx, S., Caymax, M., Claes, M., Conard, T., Delabie, A., Deweerd, W., Hellin, D., Kraus, H., Onsia,, B., Parashiv, V., Puurunen, R., Rohr, E., Snow, J., Tsai, W., Van Doorne, P., Van Elshocht, S., Vertommen, J., Witters, T., and Heyns, M., *Cleaning Technology in Semiconductor Device Manufacturing VIII.*

| Termination and Thin Film | Thickness | ALD Result |
|---|---|---|
|  | < 1 nm | Fastest deposition rate<br>Thickest EOT |
| H – O –<br>H – O –<br>H – O – | > 0.3 nm | Island-like or first monolayer |
| H – O – | < 0.3 nm | Island-like |
| H – | 0 nm | Slow Growth |

The optimal silicon surface should be completely covered by a monolayer of hydroxyl groups without any underlying silicon oxide yielding the highest surface hydroxyl density concurrently with the lowest oxygen content. Uniform surface passivation is also optimal because islands lead to a non-uniform formation of the hydroxyl layer that contribute to non-uniform film thickness and surface roughness from delayed nucleation of deposition.

### 7.2.3.2 *Interfacial Oxide Formation*

The formation of this thin uniform oxide film called the interfacial oxide helps enable quality high-κ deposition. Various methods for preparing this surface prior to high-κ deposition exist. These methods include:

1. Chemical oxidation to form a thin oxide film.
2. Thermally grown oxide or oxynitride films.
3. Films grown with the above methods that are subsequently treated to enhance the electrical characteristics.

Wet chemical interfacial oxide formation processes prior to high-κ deposition typically use SC-1 solutions or ozonated deionized water (DIW) rinses. Chemical oxides grown in SC-1 solutions have long been known to be of poor electrical quality primarily due to a high density of interface traps [71] and are not suitable for preparing the surface for high-κ dielectric deposition. The chemical oxide films are also relatively thick compared to the EOT requirements for high-κ films. Chemical

oxides formed by SC-1 are on the order of 1.0 nm, greater than the target value of 0.8 nm or less.

Figure 7.7 shows leakage current densities as a function of EOT with various chemical surface treatments. The DI/$O_3$ chemistry shows the lowest and most stable leakage current behavior. Based on these results, DI/$O_3$ dominated the wet surface treatment. For the combination HF-$O_3$ process, HF removes the native oxide, and $O_3$ creates the chemical oxide. This combination is easily implemented into manufacturing with existing process chemicals, plus it can be completed in a single wet cleaning system with minimal process steps.

The use of ozone dissolved in DIW (DI/$O_3$) is another choice for interfacial oxide formation. Because ozone rapidly oxidizes silicon, control of the reaction time, temperature, and concentration of the mixture are imperative. However, chemical oxide thickness and quality are difficult to control. Onsia and coworkers have shown that controlled oxide thickness (~1 nm) can be obtained with commercially-available processing equipment [72]. The authors found that control of the uniformity was dependent on the processing conditions and that lower concentration of ozone yielded thinner oxides and also more uniform films. They also found that scavenger addition can prevent ozone decay leading to better uniformity.

Unlike gaseous $O_3$ oxidation where uniform layer-by-layer oxidation occurs across the entire silicon surface, DI/$O_3$ oxidation occurs by first forming islands followed by filling in of the empty spaces. Saturated growth is defined by the formation of a monolayer of silicon dioxide across the entire hydroxyl-terminated surface. Studies have shown that ALD-grown high-κ films exhibit heterogeneities 8-9-nm in diameter and porosity at the interfaces [73]. These features are likely caused by defects in the exposed surface that result in initial coalescence of the ALD precursors on areas that have the highest concentration of reaction sites. These film features are not observed in the bulk film.

Growth of Hf-based high-κ material was shown by Green and colleagues to have optimum nucleation when large concentrations of OH groups are present in the interfacial chemical oxide [74]. When this occurs, there is stable linear growth with constant film density and a continuous $HfO_2$ film grown uniformly in two dimensions. They compared the OH-saturated chemical oxide film with Si-H and

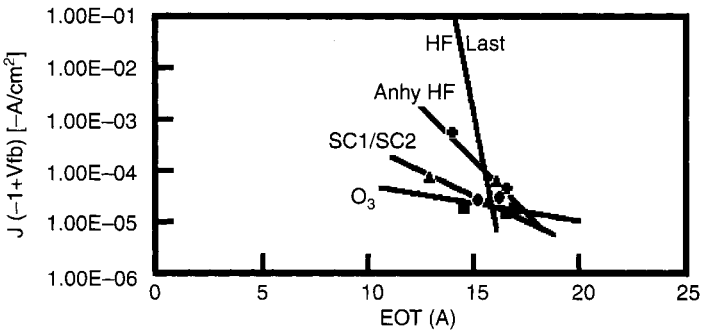



**Figure 7.7.** Leakage current densities of a high-κ stack as a function of EOT with respect to various chemical surface treatments [72]. Used with permission from SEMATECH.

SiON surfaces and found that a OH-saturated film yields the best physical and electrical characteristics.

Early studies of low-temperature oxide formation using DI/$O_3$ proposed that the silicon oxidation was limited by the amount of ozone available, but not in a true diffusion-limiting reaction because of electropotential contributions [75]. The researchers used the Cabrera-Mott model [76] to assess the formation of DI/$O_3$-formed oxide. Oxidation is proposed to occur with the following mechanism:

1. An activated O anion ($O^{-2}$) reacts with Si on the surface.
2. An electric field is created between the Si and the $O^{-2}$.
3. Fowler-Nordheim tunneling for both holes (p-type Si) and electrons (n-type Si) occurs.
4. The O anion has enough energy to overcome the activation barrier and to react with the Si at the interface.

Figure 7.8 shows the dependence of oxide thickness on the time exposed to the DI/$O_3$ at two different concentrations. The graph shows that the oxide thickness is self-limiting for 10-ppm $O_3$, and the oxide growth rate is impaired at concentrations of 1 ppm and less. A similar trend is observed with higher temperatures – the maximum thickness increases, but the oxide is still self limiting. The pH of the solution is also found to influence the oxide growth rate [77].

To obtain uniform oxide growth, researchers have developed methods to achieve high-quality oxide. One method used by Butterbaugh *et al.* controls the uniformity of oxide films grown with ozonated water by first growing a saturated oxide film followed by uniform etching with dilute HF (approximately 400–800:1 $H_2O$:49 wt% HF) [78]. They found that decreasing the oxide concentration decreased the film thickness, but increased the film non-uniformity. Therefore they formed a thicker film (0.8–1.0 nm), and then used a controlled etch-back process to obtain the

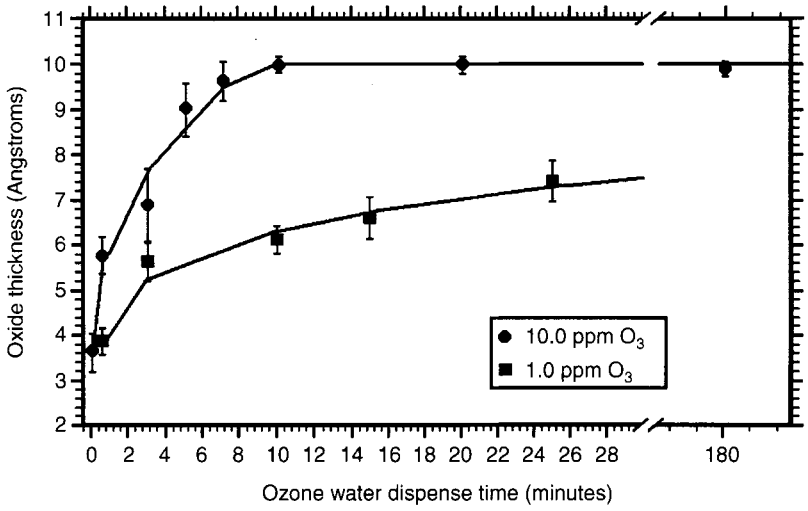



**Figure 7.8.** Chemical oxide thickness *vs.* time for two different concentrations of ozone at 22°C [75]. Courtesy of FSI International.

desired film thickness of 0.3–0.6 nm. Using less than 10 ppm ozone concentration showed difficulty in controlling the specific thickness.

Sano and coworkers used a low concentration of $O_3$ (1 ppm) in the a single wafer spin system to produce a uniform thin oxide [79]. They also reported that a single-wafer system was favored over a batch system. While the batch system showed 5.4 σ% non-uniformity for 0.7-nm oxide, the single-wafer system showed 2.3 σ% at 0.7-nm. They showed that dilute ozonated water is capable of forming a uniform and saturated thin film on a Si surface. The optimum thickness was greater than 0.7 nm because the leakage current was high at lower thicknesses of oxide. This suggests that lower thicknesses are not fully covered by hydroxyl-terminated groups. Transmission electron microscope images showed bare spots where no oxide was formed, and electron energy loss spectroscopy (EELS) also confirmed that O was not present on the surface, further supporting the island-growth theory.

Additives such as HCl and acetic acid have been proposed by *Onsia et al.* to offset the decay of $O_3$, and to increase the oxide thickness by increasing the pH [75].

A comparison of the interface layers formed with SC-1/SC-2 and $O_3$ are shown in Figure 7.9. The interfacial oxide formed by the $O_3$ cleaning step followed by a $NH_3$ anneal at 600°C has a visibly more distinct interface and a smoother film than that formed with SC-1/SC-2, but this oxide yielded a lower EOT [66]. The $O_3$ process had a more uniform leakage current across the 200-mm wafer. Under any of these conditions, exposure of the thin oxide to air augments the film; therefore, exposure should be avoided to maintain the high-quality oxide.

### 7.2.3.3 *Thermal Oxidation*

Thermal oxide formation is also a good candidate to create interfacial layers. Beside chemical oxide formation, interfacial oxide, and sometimes oxynitride can be grown using high temperature processing. Since leakage is one of the reasons thin gate dielectric films fail, research has been ongoing to find a method to grow thin high-quality $SiO_2$ that has low interface trap density and good mobility. Rapid thermal oxidation for interfacial oxide formation has been accomplished [80]. Formation of the oxide *in situ* by single wafer RTP allows the substrate to be

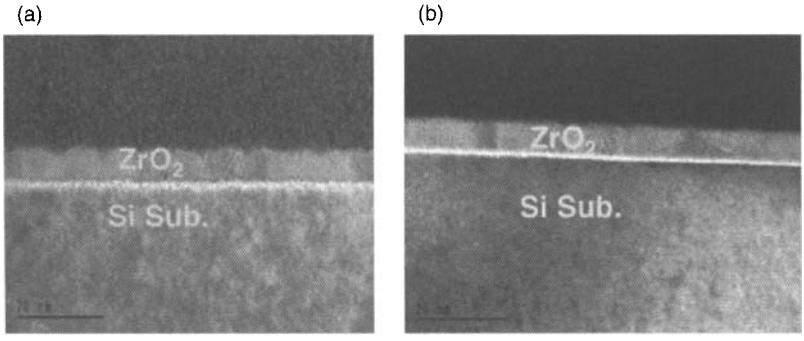



**Figure 7.9.** Transmission electron microscope images of interfacial oxide layer cleaned with a) SC-1/SC-2 and b) $O_3$, followed by a 600°C $NH_3$ anneal [66]. Used with permission of *Future Fab International.*

transferred from the RTP chamber to the ALD chamber without breaking vacuum retaining the high-quality oxide characteristics.

*In situ* steam generation (ISSG) oxidation [81] is one of these methods used to form high-quality pre-ALD interfacial oxide. Originally, ISSG oxidation was used for forming thin gate dielectric film prior to the high-κ era. The ISSG process uses $H_2$ and $O_2$ in a RTP chamber (~1050°C) that reacts to form $H_2O$ [94]:

$$2\,H_2 + 2\,O_2 \rightarrow H_2O + O^* + 2\,OH \tag{7.2}$$

This method is speculated to form a dense oxide with few dangling or strained bonds because of the generation of O* radicals that can react with these bonds to form stochiometric $SiO_2$ [83]. This oxide has been shown to be superior to other steam generated oxide processes [84].

After considering several approaches, ISSG has been shown to form high-quality interfacial oxide, after a 2-nm film is grown and etched back [67]. The saturation current data was 5~10% higher for all device lengths tested.

Other work has shown that the use of water vapor at high temperature (350–400°C) yields a thin 6-Å oxide with the appropriate hydroxyl termination groups to facilitate ALD high-κ dielectric deposition [85]. The researchers suggested that the oxide formation on HF-last, hydrogen-terminated silicon surfaces became hydroxyl-terminated after hydrogen was desorbed at ~350°C.

Methods to improve the quality of the gate oxide after growth have been undertaken. One such method has been reported by Chang *et al.* using ultraviolet-enhanced and gaseous HF processing [86].

### 7.2.3.4 *Nitrided Surfaces*

For further improvement, silicon nitride (SiN) or silicon oxynitride (SiON) have been considered for sub-nm interfacial oxide [87]. A mono-layer film of silicon nitride could perform as a diffusion barrier. Additionally, ultraviolet (UV) light can provide uniform N-termination of the silicon [88]. On the other hand, Tsujikawa *et al.* also reported high nitrogen concentration leads to carrier mobility loss [89].

Silicon nitride layers with a dielectric constant of about 7.2 have been prepared by ALD [8]. Chemically or thermally grown oxide/oxynitride films on Si, preferably with a high density of terminal hydroxyl groups, are excellent nucleation layers for CVD and ALD-grown dielectrics. However, to maximize capacitance, an interfacial layer with an EOT <1 nm is required, motivating the development of alternative surface treatment schemes. This requires an evolutionary approach to electrically thin interfacial layers by the use of high nitrogen concentration SiON or pure silicon nitride. Hydrogen-terminated silicon with $NH_3$ pre-treatment for $Al_2O_3$ ALD deposition has been shown to provide an effective barrier against interfacial $SiO_2$ formation and promote the nucleation of $Al_2O_3$ growth [90]. Nitride layers thicker than 0.3–0.4 nm were shown to provide an adequate barrier.

### 7.2.3.5 *Hydrogen-terminated Surface*

Deposition of high-κ materials directly on silicon has proved challenging because of the inter-diffusion of the metals from the high-κ dielectric into the silicon and

Next Page



*visa versa*. Also, direct deposition of the high-κ material by ALD processing on the H-terminated silicon poses a significant nucleation barrier.

Under the right conditions, the H-terminated surface can be transformed to one that nucleates the high-κ film precursors [91]. The researchers detected a $SiO_x$/SiOHf interfacial layer by angle resolved x-ray photoelectron spectroscopy (ARXPS) after multiple (>6) ALD cycles. Frank and collaborators have shown that on H-terminated surfaces nucleation can take place initiated by the organometallic precursors [92]. The reaction of the precursor, tetrakis-ethylmethylamino hafnium, takes place directly with the Si-H bond progressing from Si-H to Si-O-Hf, to $HfO_2$ [93]. The $SiO_2$ that is observed at the interface is apparent only after the annealing step. The $SiO_2$ interfacial film is critical. When this layer does not exist, silicide formation may occur leading to a decrease in electron mobility. A unique process has been proposed –sputtering Hf, Zr, or Al directly on an HF-last cleaned silicon surface, then annealing in an oxygen furnace [90]. However, an oxygen-free interface, and intermixing have proven challenging.

### 7.2.4 High-κ Deposition on Germanium

Germanium has intrinsically higher mobility than silicon and is currently under investigation as an alternative to improve transistor performance. Formation of thin high-quality germanium oxide before high-κ dielectric deposition is challenging, not only because the oxide is thermodynamically unstable, but because of the inability to form a passivating layer by simple oxidation or wet chemical methods. Germanium oxidation and passivation is covered in detail in Chapter 12. Early work with germanium used ozone to form an oxide prior to high-κ deposition after a HF vapor exposure or water rinse to remove the native oxide [94].

Germanium interfacial dielectric layers composed of $GeO_x$ or $GeO_xN_y$ are proposed to inhibit Hf diffusion into the germanium substrate [95]. Prior to interfacial oxide formation, the wafers were cleaned with a 50:1 HF solution. The nitrogen-containing interfacial oxide appears physically rougher than the $GeO_x$ interfacial oxide but shows better electrical properties due to the reduction in the defect density attributed to poor quality $GeO_x$. Figure 7.10 shows TEM images of the high-κ

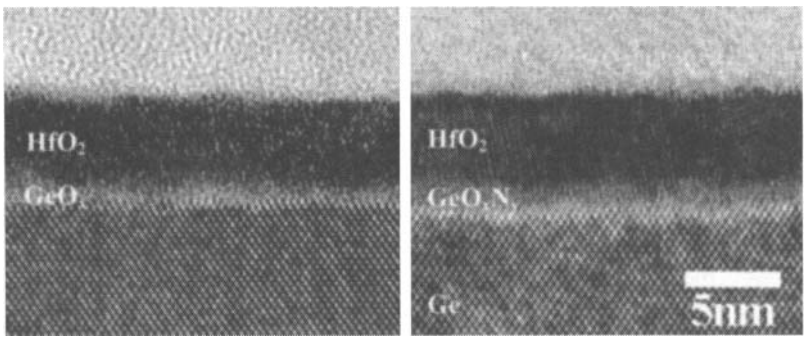



**Figure 7.10.** Transmission electron microscope images of interfacial oxide layer on germanium of a) $GeO_x$ or b) $GeO_xN_y$ [95]. Used with permission from Kim, H., McIntyre, P. C., Chui, C. O., Saraswat, K. C., Cho, M.-H, *Applied Physics Letters*, 85(1404):2902 (2004). Copyright 2004, American Institute of Physics.

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# PART 2
# APPLICATIONS

7

# Cleaning Challenges of High-κ/Metal Gate Structures

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*Abstract*

High-κ/metal gates are used as transistors for advanced logic applications to improve speed and eliminate electrical issues associated with polySi and $SiO_2$ gates. Various integration schemes are possible and will be discussed, such as dual gate, gate-first, and gate-last, both of which require specialized cleaning and etching steps. Specific areas of discussion will include cleaning and conditioning of the silicon surface, forming a high-quality chemical oxide, removal of the high-κ dielectric with selectivity to the $SiO_2$ layer, cleaning and residue removal after etching, and prevention of galvanic corrosion during cleaning.

*Keywords:* high-κ/metal gate, metal gate electrode, dual metal gate, high-κ gate dielectrics, gate-first, gate-last, high-κ removal, interfacial oxide, chemical oxide, galvanic corrosion

## 7.1 Introduction and Overview of High-κ/Metal Gate Surface Preparation

Reducing dimensions of a metal oxide semiconductor field effect transistor (MOSFET) requires a dielectric to replace conventional $SiO_2$ to accommodate the low voltage with low leakage current. The need to maintain electrical synergy between the gate and channel is an indirect motivation for the development of metal gate electrodes. Additionally, a tunable work function gate material is needed to replace the conventional poly crystalline silicon (poly-Si) gates – that are so highly doped they are almost as conductive as metal – to provide the necessary threshold voltage. Thus, high-κ/metal gate (HKMG) structures were developed to meet these needs.

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### 7.1.1 High-κ Dielectric Evolution

For years, silicon dioxide, with a dielectric constant (κ) of 4.2, was the mainstay gate dielectric material of the integrated circuit (IC) in MOSFET devices. The integration of $SiO_2$ was simple – grow an oxide from the already existing silicon substrate and make sure it was clean and defect-free before an oxidation step. As the thickness of the gate insulator shrank to maintain the required capacitance needed to meet lower voltage, high driving capability and produce faster circuits, the $SiO_2$ thickness was approaching the physical limit of a monolayer. Growing a very thin thermal oxide (<1.0 nm) is extremely challenging and as the gate layer thins, the reliability degrades exhibiting pinholes and electrical leakage, even with optimized processes.

Early researchers recognized that next-generation devices, starting at about 65 nm, would have serious issues that must be addressed such as: high gate leakage current, increased power consumption, poor time-dependent dielectric breakdown, reduced drive current, polySi-gate depletion, boron penetration, reliability degradation, and plasma process-induced damage [1, 2]. As the gate dielectric thickness decreases further for smaller than 50-nm devices, additional problems arise due to high tunneling current and reduced drive current. Green and coworkers suggested that these issues would prevent further scaling. They and others proposed that alternate gate dielectrics beyond $SiO_2$ were needed [1, 2]. By increasing the permittivity of the gate dielectric, the physical thickness of the gate may be increased providing reduced gate leakage current and enhanced transistor device characteristics with comparable device capacitance [3]. Various choices of dielectrics that could yield the requisite equivalent oxide thickness (EOT) are available, including $SiO_2$, $Si_3N_4$, Hf- and Zr-based compounds, and summarized in reference [4].

The EOT is calculated by the following equation:

$$\text{EOT} = 3.9/\kappa \tag{7.1}$$

where κ represents the physical thickness of the dielectric and interfacial layer. The required EOT for <50 nm devices is ≤1.0 nm; however, if the interfacial oxide is already 1.0-nm thick, there is no more thickness margin for high-κ layers.

Nitrided-gates, with a dielectric constant of approximately 6.5–7.2, although short-lived in the 1990's, provided a segue into high-κ dielectric films. They have been recognized as a film that prevents boron diffusion [5], can be formed with high reliability at a low thermal budget [1, 6], and lower gate leakage. However, tunneling occurs at the thicknesses required and leads to electrical issues. Several techniques exist to form oxynitride films, such as: thermally-grown oxynitride [5], nitridization with NO [7], rapid thermal processing (RTP) with a N-containing additive such as $N_2O$ [6] or $NH_3$, chemical vapor deposited (CVD) nitrides, silicon nitride grown with atomic layer deposition (ALD) [8], and other alternative processes that can also improve gate oxide reliabilities [1].

The evolution to high-κ dielectric materials was driven by the need to provide electrical characteristics of high carrier mobility with low permeability, high capacitance and an acceptable band gap to silicon [9] to reduce tunneling [10].

The physical characteristics that must be met are thermodynamic stability with high interface quality and low roughness, film morphology that is integratable with silicon. Most of all, these films must have high reliability and low gate dielectric leakage. The film must be easily deposited or grown in sufficiently thin, noncrystalline layers with good uniformity. This film must be manufactured in high volume, compatible with existing materials and processes used for IC devices. Additionally, the film should not react with the substrate to form silicates or silicides, have minimal $SiO_x$ or other interfacial material, and the film should not surrender oxygen atoms to the substrate or gate electrode. In general, the interfacial properties of the high-κ material with the silicon substrate are critical. In order to meet the future requirement for sub-nm interfacial thickness on a gate stack, the following items will be required:

1. Good contact between high-κ and substrate. This requires good surface termination such as homogeneous hydroxyl groups.
2. No electron/hole mobility degradation with sub-nm thicknesses.

References [3, 11, 12] summarize the requirements for an effective high-κ dielectric material and review many of the proposed films.

Before being implemented in MOS gate structures, memory devices used high-κ materials for capacitors. Metal oxides, $Ta_2O_5$ and $Al_2O_3$ were the materials of choice, although hafnium-based high-κ materials were also in use and have now become the predominant capacitor dielectric. After nitride oxides surpassed their usefulness as gate dielectric materials, the evolution of high-κ began in 1999 when $HfSiO_x$ was introduced as a possible candidate [13] having dielectric constant 25 or greater. Although hafnium compounds, in particular $HfO_2$, HfO(N), and HfSiO(N), are the specific films in use, zirconium was also considered as a possible material [14]. Hafnium compounds are now used for the 22-nm node, the dominant high-κ dielectric for logic IC manufacturers.

### 7.1.2 Metal Gate Evolution

Gate electrode materials have been ever-changing. Early IC devices used metal gates, then there was a migration to silicon-based gates. Current technologies are returning to metal gates structures. The simple single gate structure for MOSFET devices have morphed into dual gate structures with each gate tuned to its work function for the channel. The threshold voltage is determined by whether the device is n- or p-type (NMOS or PMOS).

PolySi gate electrodes can have their work function modified by doping the semiconductor to obtain the desirable threshold voltages; however, metal gates cannot be so easily tuned. For highly doped polySi gate electrodes, upon applying a bias, a ~0.5-nm thick depletion region forms and contacts the insulator, adding to the EOT, and thus reducing coupling [15]. As the gate oxide thickness is scaled below 2 nm, this depletion region becomes a significant part of the EOT. In metal gate electrodes, however, this depletion region is almost nonexistent. Hence, the use of metal gate electrodes allows thinner EOT to be attained. Also, replacing polySi with metal gates that have near-silicon band edge work functions

can overcome problems with boron penetration and Fermi level pinning [16]. The change in the electrode series capacitance dictates the use of a material that reduces the capacitance as the gate oxide thins to less than 1-nm EOT. Channel mobility is also an issue when using high-κ dielectrics; metal gates eliminate this problem [17] while also addressing the capacitance requirements.

Schaeffer and coworkers have modeled the optimal gate work functions for the <50 nm devices. They postulated this value should be 0.2 eV below the conduction band of silicon for n-type MOSFET and 0.2 eV above the valence band for p-type MOSFET [18]. They have evaluated TiN, TaSiN, and WN gate electrodes although the actual work function is also dependent on the gate insulator material [19]. Many other researchers have determined the acceptable value for the work function with Cheng *et al.* summarizing the results at approximately 4.1–4.4 eV for NMOS and 4.8–5.1 eV for PMOS [20].

Researchers recognized a need for a new gate electrode that could satisfy dual work function requirements for <50 nm channel length logic devices combined with a high-κ gate dielectric. Substantial efforts have been made to replace polySi gates with metal gates [21–23] including fully integrated HKMG [24]. Many transition metals, react with $SiO_2$ at elevated temperatures to form metal silicide and metal oxide layers [25, 26]. Use of high-κ gate dielectrics with the metal gate avoids these unwanted reactions. Metal gates with high-κ gate dielectrics can be more easily integrated into the manufacturing process than polySi gates with high-κ gate dielectrics. Temperatures, >1000°C, that are needed to activate the polySi gate can degrade the performance of the high-κ dielectric [27, 28]. Materials selected to try first were ones already developed for IC manufacturing, such as the barrier metal for Cu, Al, and W processing. Candidates included TaN, TiN, and TaSiN [29], and some other films such as Ti [30], Mo [31], and Ni for FUSI devices [32], plus others.

At the same time, different techniques had been tried to successfully implement dual metal gate CMOS [33–37]. A metal wet etch-based integration scheme proposed leaving one of the metals intact (low work function), and then depositing a second metal (high work function) on top of the first metal, then etching back the metal in the areas requiring the low work function [29, 30]. One early method involved depositing one metal, patterning it, and then etching the second metal [31, 38], called gate-first. The first metal should preferably have a high etch selectivity over the gate dielectric so that the dielectric is not significantly damaged when the metal is etched. However, metal wet etch remains a challenging task [29, 31] as exposing the gate dielectric to metal etching chemistry causes undesirable thinning and potential gate dielectric damage [29, 31]. Although a highly selective metal wet etch module has been developed [41], devices with the desired electronic performance have not yet been demonstrated.

Furthermore, integration of metal gates proved difficult because exposure of the sensitive high-κ layer to blanket etching could damage the film and etching two critical lithography layers was expensive. The metal gates, using traditional patterning process of photolithography followed by etching, must withstand high temperature processing, typically >1000°C.

Various integration schemes were proposed. The replacement gate, also called gate-last, is an integration scheme where a dummy polySi gate is replaced with metal gates [42–44]. Other researchers have developed silicided gate electrodes, such as

fully silicided metal gate (FUSI) [32]. An integration scheme – dual high-κ dual metal gate CMOS – has been developed to demonstrate devices for 45-nm low standby power node applications [45], even so, this integration scheme encounters some challenges inherent in a conventional deposition-etch-deposition based dual metal gate CMOS flow. Electrical characterization results show a symmetric short channel threshold voltage, $V_t$, of ~ ± 0.45V with ~80% high field mobility for both N and PMOS and significantly lower gate leakage compared to polySi gate and silicon oxynitride dielectric gate stack. Also, in the quest for improved electrical performance, a dielectric capping layer has recently been introduced to achieve a significant shift in the threshold voltage of metal gate devices toward the silicon conduction band edge. Also, well behaved short channel devices have been demonstrated with aluminum oxide ($Al_2O_3$), gadolinium oxide ($Gd_2O_3$), and lanthanum oxide ($LaO_x$) [45–47].

## 7.1.3 High-κ/Metal Gate Integration and Structures

Integration of metal gate materials with the high-κ dielectric materials require that they be compatible with one another at subsequent processing steps and, for long term reliability, they must not interact. Although by no mean a standard process, many companies have adopted HfSiO(N) gate dielectrics and TiN and Ta gate electrodes. For example [48] and some companies are using a gate-first [49] or gate-last approach [50], and possibly the FUSI process already mentioned [32]. Recently, a hybrid approach combining both gate-first and gate-last was disclosed [51].

### *7.1.3.1 Gate-First Process*

The gate-first process, also called the metal inserted polySi stack (MIPS), is desirable because it follows the process flow used in traditional IC logic MOSFET processing where the gate electrode is defined by a lithography and etching step followed by self-aligned source/drain (S/D) implants. However, this integration scheme restricts the choice of high-κ dielectric and metal gate materials as they must be able to be etched.

Various process flows are used for gate-first integration schemes [49, 52]. A generalized process is outlined in Table 7.1. For examples, in the gate-first approach explained in reference [33], the process first cleans and deposits the high-κ, metal gate, and polySi gate-capping layers followed by a gate stack etch to define the critical dimension (CD). Gate formation is followed by halo implantation of the S/D extension, offset spacer formation, deep S/D implantation, S/D high-temperature rapid thermal anneal (RTA), and S/D silicide formation. Conventional contact and metal-layer steps complete the process. This process is similar to conventional MOSFET processes, with the substitution of high-κ for $SiO_2$ dielectric and the use of a metal gate. The polySi capping layer helps to integrate the metal gate into the conventional process.

Figure 7.1 depicts one integration scheme for gate-first using dual metal deposition and wet etch-back of the first metal. Figure 7.2 shows transmission electron microscopy (TEM) images of NMOS and PMOS transistor metal gate stacks with a high-κ gate dielectric from the same complimentary MOS (CMOS) device. The TaSiN was removed from the PMOS transistor before Ru was deposited. Some

scheme with metal 1 etch-back.

| |
|---|
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 1 deposition |
| Hardmask deposition |
| Hardmask pattern |
| Hardmask etch |
| Hardmask photoresist strip |
| Hardmask post-strip clean |
| Metal 1 etch and clean |
| Hardmask removal |
| Pre-metal 2 clean |
| Metal 2 deposition |
| PolySi (or α-Si deposition) |
| Metal 1 and 2 electrode pattern |
| Metal 1 and 2 etch |
| Metal 1 and 2 photoresist strip |
| Metal 1 and 2 post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |

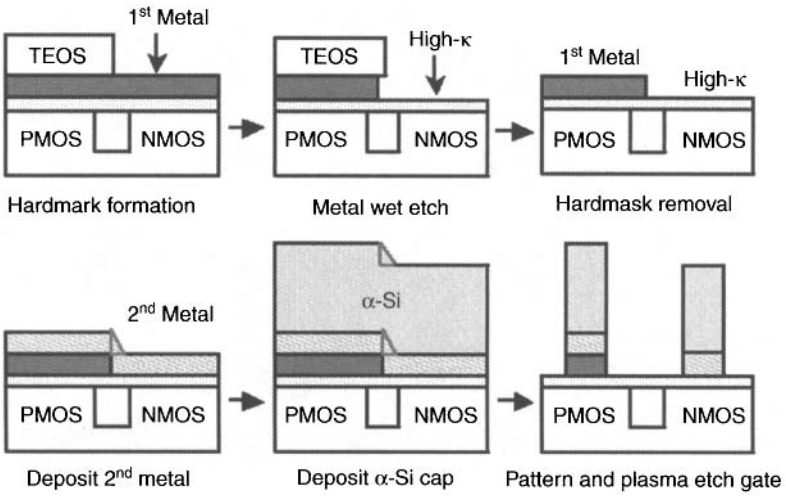



**Figure 7.1.** Schematic of the dual gate-first process flow using metal wet etch for removing the first metal layer (αSi is amorphous silicon) [52]. Reproduced with permission of ECS – The Electrochemical Society from Zhang, Z., Song, S. C., Huffman, C., Hussain, M. M., Barnett, J., Moumen, N., Alshareef, H. N., Majhi, P., Sim, J. H., Bae, S. H., and Lee, B. H., *Electrochemical and Solid State Letters*.

of the steps in Table 7.1 have been simplified such as the spacer formation and implants to focus on the important steps pertaining to HKMG cleaning and surface conditioning. Figure 7.3 shows the finished HKMG structure with the gate-first process.

### *7.1.3.2 Gate-Last Process*

The replacement gate (RPG) processing has been proposed as a method to retain the junction profiles and small gate widths for many years before the use of HKMG [53] [54]. The replacement gate process, also called disposable gate, replacement gate, damascene gate, or the gate-last process, requires a chemical mechanical polishing step and an etching process to remove the sacrificial gate materials [50]. However, because the high temperature implant drive is performed before the

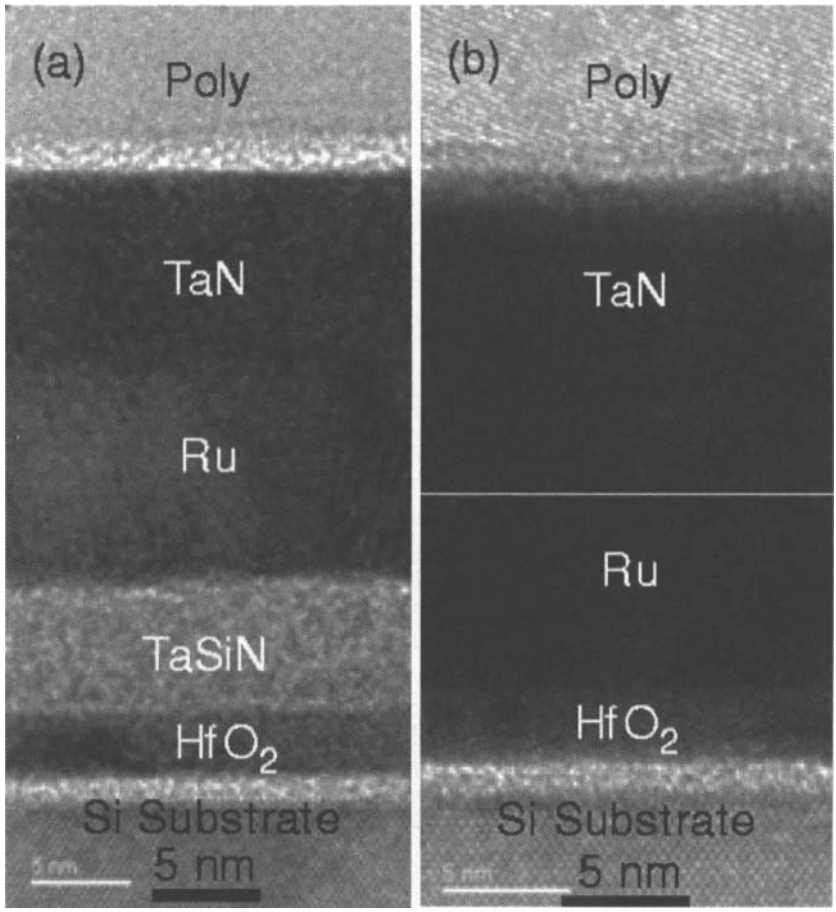



**Figure 7.2.** Cross section TEM images of dual metal gate a) NMOS and b) PMOS gate stacks structures from the same CMOS device [52]. Reproduced with permission of ECS – The Electrochemical Society from Zhang, Z., Song, S. C., Huffman, C., Hussain, M. M., Barnett, J., Moumen, N., Alshareef, H. N., Majhi, P., Sim, J. H., Bae, S. H., and Lee, B. H., *Electrochemical and Solid State Letters*.

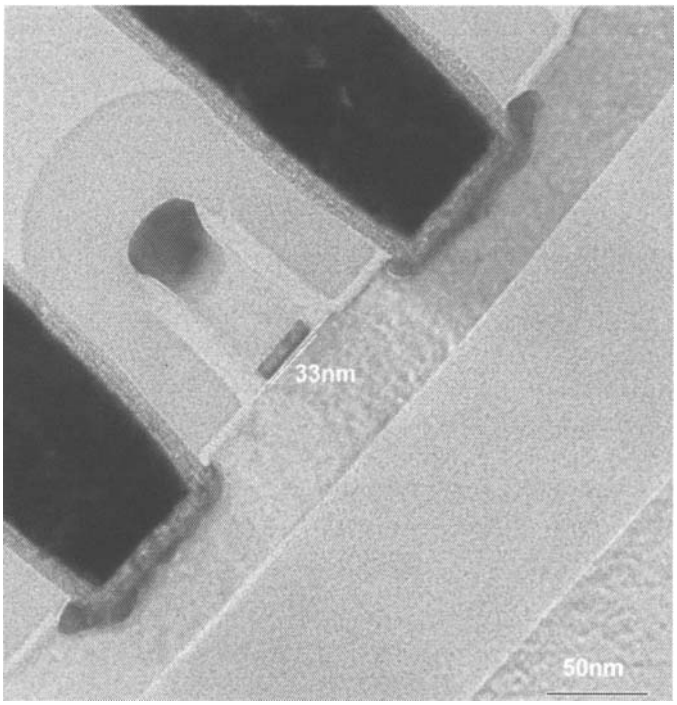



**Figure 7.3.** Cross section TEM image of a 32-nm HKMG using the gate-first integration scheme showing minimal loss of the substrate [49]. Used with permission of Chudzik, M., Doris, B., Mo, R., Sleight, J., Cartier, E., Dewan, C., Park, D., Bu, H., Natzle, W., Yan, W., Ouyang, C., Henson, K., Boyd, D., Callegari, S., Carter, R., Casarotto, D., Gribelyuk, M., Hargrove, M., He, W., Kim, Y., Linder, B., Moumen, N., Paruchuri, V. K., Stathis, J., Steen, M., Vayshenker, A., Wang, X., Zafar, S., Ando, T., Iijima, R., Takayanagi, M., Narayanan, V., Wise, R., Zhang, Y., Divakaruni, R., Khare, M., and Chen, T. C., *VLSI Symposium Technical Digest*. © 2007 IEEE.

deposition, a wider range of materials can be used for both the dielectric and the gate. The gate-last process flow can have some modifications based on the choice of materials and has the flexibility to use a wide range of materials both for the high-κ and gate electrode because of the individual processing steps for each deposition. Table 7.2 outlines the process flow for this integration scheme. For the integration scheme [34] first deposits and etches a sacrificial or dummy $SiO_2$/polySi gate stack. This is followed, the same as the gate-first approach, by the extension, spacer, S/D implant, S/D RTA, and S/D silicide steps. At this point an additional dielectric layer is deposited and resurfaced by chemical mechanical polish (CMP) stopping at the top of the dummy gate. Next, the dummy gate is removed and the final high-κ and metal layers are deposited, then CMP or a patterned etching step is used to remove the metal layer between the gate stacks stopping on top of the high-κ layer. Contact and metal layer complete the process.

Figure 7.4 depicts schematically the integration scheme for gate-last. Again, some of the steps in Table 7.2 have been simplified. Figure 7.5 shows TEM images of a NMOS and PMOS transistor fabricated with the gate-last integration scheme.

**Table 7.2.** Process flow for gate-last integration scheme.

| |
|---|
| Pre-dielectric deposition clean |
| Sacrificial gate oxide formation |
| Sacrificial polySi gate deposition |
| PolySi gate pattern |
| PolySi gate etch |
| PolySi gate photoresist strip |
| PolySi gate post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |
| Sacrificial metal 1 gate pattern |
| Sacrificial metal 1 gate etch |
| Sacrificial metal 1 gate removal |
| Sacrificial metal 1 gate photoresist strip |
| Sacrificial metal 1 gate post-strip clean |
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 1 deposition |
| Metal 1 and high-κ deposition CMP |
| Metal 1 and high-κ post-CMP clean |
| Sacrificial metal 2 gate pattern |
| Sacrificial metal 2 gate etch |
| Sacrificial metal 2 gate removal |
| Sacrificial metal 2 gate photoresist strip |
| Sacrificial metal 2 gate post-strip clean |
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Metal 2 deposition |
| Metal 2 and high-κ deposition CMP |
| Metal 2 and high-κ post-CMP clean |

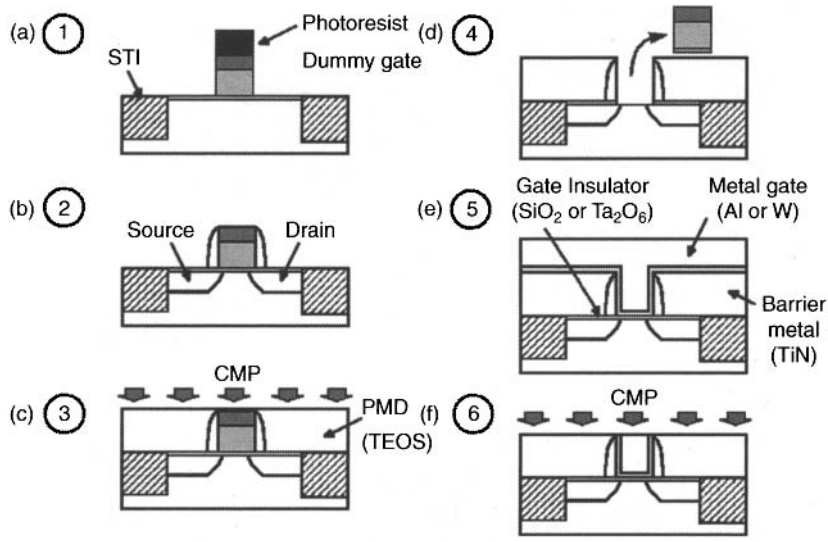



**Figure 7.4.** Schematic of the dual gate-last process flow with CMP step for defining the gate structures [42]. PMD is pre-metal dielectric. Used with permission of Yagishita, A., Saito, T., Nakajima, K., Inumiya, S., Akasaka, Y., Ozawa, Y., Hieda, K., Tsunashima, Y., Suguro, K., Arikado, T., and Okumura, K., *Transactions of Electron Deivces*. © 2000 IEEE.

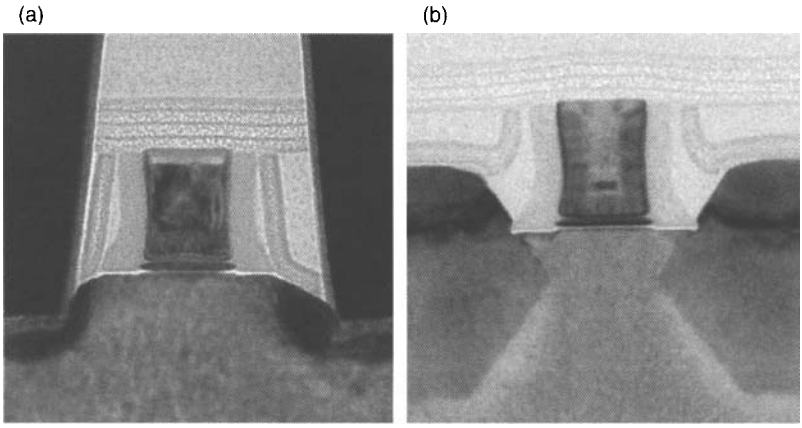



**Figure 7.5.** Cross section TEM image of a 45-nm HKMG using the gate-first integration a) NMOS and b) PMOS [50]. Used with permission of Auth, C., Cappellani, A., Chun, J.-S., Dalis, A., Davis, A., Ghani, T., Glass, G., Glassman, T., Harper, M., Hattendorf, M., Hentges, P., Jaloviar, S., Joshi, S., Klaus, J., Kuhn, K., Lavric, D., Lu, M., Mariappan, H., Mistry, K., Norris, B., Rahhal-orabi, N., Ranade, P., Sandford, J., Shifren, L., Souw, V., Tone, K., Tambwe, F., Thompson, A., Towner, D., Troeger, T., Vandervoorn, P., Wallace, C., Wiedemer, J., and Wiegand C., *VLSI Symposium on Technology*. © 2008 IEEE.

### *7.1.3.3 Comparison between Gate-First and Gate-Last Scheme*

A metal gate and high-κ dielectric can be integrated into the MOSFET with a gate-first or gate-last approach. These approaches primarily differ in whether the metal gate is deposited before or after the source/drain activation anneal. Table 7.3

**Table 7.3.** Comparison between gate-first and gate-last integration.

| | Gate-first Approach | Gate-last Approach |
|---|---|---|
| Pro | Compatible with conventional CMOS process<br>Fewer process steps<br>Potentially high yield | Low thermal process<br>More intrinsic high-κ and metal gate properties |
| Con | EOT and $V_t$ control issue<br>Halo implantation through metal gate | Need extremely conformal high-κ and metal gate process<br>Possible defect issue, lowering device yield<br>High fringing field issue<br>Previous silicide formation limits allowable subsequent high-κ/metal gate process |

summarizes the comparison between gate-first and gate-last integration schemes. When compared to the gate-last approach, the gate-first approach has the advantage of being compatible with the conventional CMOS process. Gate-first CMOS requires fewer and less-complicated process steps offering greater potential for high device yield. The primary disadvantage of the gate-first approach for high-κ metal CMOS is that the gate stack is subjected to the high-temperature S/D anneal. This presents several challenges. High temperatures can lead to crystallization of the high-κ dielectric; this increases gate leakage, makes the κ value non-uniform across the wafer, and causes intrinsic charge trapping and coulomb scattering issues. However, if a very thin high-κ layer is used, the transformation of the dielectric from amorphous to crystalline phase is kinetically suppressed [59], so an amorphous high-κ dielectric can be sustained through the high-temperature anneal process.

Another challenge is chemical reactions between the metal gate and high-κ during the anneal. If a chemically unstable metal gate is used, it reacts under high temperature with the high-κ dielectric resulting in a work function that differs from the metal's bulk properties. This issue can be avoided by using a thermally stable metal for the gate, but the choice is limited because metals that are chemically stable might not offer the desired work function. In some cases, however, a high-temperature anneal is actually required to enhance the interface dipole formation and set the appropriate work function [36]. There has also been concern that chemical reactions can increase the dielectric EOT, but that is not always true. Recent studies indicate that metal doped into the high-κ material can increase its κ value, particularly when a $HfO_2$ dielectric is used with a Ti or Ta-based metal gate [35]. Also, certain metal gate materials, such as TiN or HfSi, scavenge oxygen from the dielectric's bottom oxide layer [29], potentially decreasing EOT after the high-temperature process.

Another challenge posed by the high-temperature anneal is dopant diffusion. During the anneal, the boron dopant used in PMOS devices can diffuse from

the polySi cap through the metal gate, especially when a thin metal gate is used. Presence of boron in the gate cap is unavoidable in the gate-first process because the gate stack is formed before the dopant is implanted. Boron diffusion is a concern in high-κ processes because boron diffuses much faster in $HfO_2$ than in $SiO_2$ [39]. Boron atoms in the dielectric can degrade reliability by producing a charge that shifts the threshold voltage ($V_t$) [55]. However, B atoms produce a charge only where $SiO_2$ atoms are present in $HfO_2$, (i.e., Hf-silicate) [15]. The $V_t$ shift can be reduced by using the lowest optimal $SiO_2$ concentration in the HfSiO dielectric, even though more boron diffusion might occur. Boron diffusion can also be suppressed by using an amorphous phase metal for the gate, and also by doping the high-κ material with nitrogen.

The gate-first approach presents additional challenges because the HKMG stack must be etched before S/D implantation. Etching of the metal gate can be difficult, especially for high work function materials, which tend to be relatively noble (non-reactive) metals [38]. Furthermore, metal oxidized during dry etch processing can be difficult to remove. A high-temperature etching process is required and a combined dry and wet etch process may be needed to completely remove the etch residue.

Control of the gate CD is also an issue. Depending on the metal used, some undercut of the metal gate could occur because of isotropic etching. Other metals tend to form a metal foot at the base of the gate, below the polySi capping layer. The foot occurs because the slower etching rate of the metal allows polymer buildup on the gate sidewall, preventing etching through the polymeric layer. Any undercut or foot in the metal gate makes it difficult to control gate CD that is measured at the bottom of the gate stack, rather than the top. Undercutting can be avoided by using dry etching for metal removal, and formation of a foot can be suppressed by optimizing the dry etch process, especially etch chemistry that generates less polymer.

Another challenge is removal of the high-κ dielectric in the S/D area. The dielectric must be removed thoroughly to prevent any process induced charge effect [56] that can cause parameter drift and degrades performance. Section 7.4 discusses the removal of the high-κ dielectric. Hafnium dioxide is difficult to wet etch with HF chemistry once the $HfO_2$ is crystallized, but it can be wet etched if it is first subjected to physical bombardment. While HfSiO is easily etched by HF chemistry, the isotropic etch results in undercutting below the metal gate edge. The undercut is later filled with lower-κ material, such as nitride, which degrades device performance and reliability. High-κ dry etching processes also causes damage unless healed appropriately [57].

Finally, the metal gate-first approach presents integration issues with respect to angled implantation, such as halo implantation for the S/D extension. The metal of the gate stops ions that would normally pass through a polySi gate reducing the effective dose that reach the Si substrate. The implantation step also tends to sputter metal atoms onto the high-κ dielectric and Si substrate, possibly degrading performance and reliability. These issues can be avoided by depositing an offset spacer at the gate edge before halo implantation to prevent ions from striking the metal gate.

The gate-last approach offers the advantage of a low thermal budget process after the high-κ dielectric and metal stack are formed, thus, the resulting dielectric and metal gate properties will be closer to their intrinsic values. The gate-last approach allows CMP to be used for removing excess metal after the gate stack is finished, avoiding the need to etch the HKMG material. This is desirable when using a noble gate metal for which chemical etching is ineffective. The HKMG is formed in the trench left when the dummy gate is removed. The subsequent CMP removal is self-aligning because the gate CD had already been defined by the dummy gate. Any non-uniformity in the CMP process could leave some residual metal between the gates, shorting the devices. An alternative is to use a photolithography and dry etching process to remove the residual metal. In this case the gate CD is still defined by the dummy gate, but any offset or overlay in the top gate pattern might violate the gate-to-contact design rule.

The primary disadvantages of the gate-last approach are process complexity and small gate size. As the gate length and width are scaled, it becomes more difficult to remove the dummy gate completely and fill the gate hole evenly with the metal and high-κ gate materials. As more devices are integrated into a die, there is a greater chance of yield loss because of these issues. Typically, a wet etch is preferred for dummy gate removal because it is very selective and less damaging than a dry etch to the Si substrate. It is necessary to ensure enough overetch is applied to remove all the dummy gate residue.

Once the gate trench is cleared, a conformal process is needed to deposit the high-κ and metal gate layers. Use of physical vapor deposition (PVD) is restricted because of poor step coverage. Atomic layer deposition is preferred because it offers excellent step coverage, but the materials are limited by the available precursors. Another challenge of the gate-last approach is larger fringing capacitance caused by high-κ deposition on the gate hole sidewall. This high-κ material remains in place after the gate stack is complete increasing capacitance at the gate edge and potentially degrading the performance of the device.

The gate-last approach also limits the maximum process temperature allowed for high-κ/metal deposition and anneal to <500°C. Any higher temperature would degrade performance by increasing the sheet resistance ($R_s$) of the already formed NiSi on S/D area. This limitation can be avoided by forming the silicide contacts after the gate replacement step, but only at the cost of even greater process complexity.

### *7.1.3.4 Fully Silicided Process*

The FUSI process takes advantage of the ability to use polySi as the electrode material where silicide technology is used to form the transistor on both n- and p-channels. The FUSI electrodes can be used on either $SiO_2$, SiON, or HfSiO [58]. The metals that can be used are Co [32], Pt [59], with Ni being found to give the best electrical results [60]. Table 7.4 outlines the process flow for the FUSI integration scheme; Figure 7.6 depicts one such scheme using nickel as the metal. The

**Table 7.4.** Process flow for fully silicided gate integration scheme.

| |
|---|
| Pre-dielectric deposition clean |
| Interfacial chemical oxide formation |
| High-κ deposition |
| Sacrificial polySi gate deposition |
| PolySi work function tuning implants |
| PolySi gate pattern |
| PolySi gate etch |
| PolySi gate photoresist strip |
| PolySi gate post-strip clean |
| Extension source/drain implants |
| Spacer formation |
| Source/drain implants |
| Silicide metal deposition (Ni) |
| First silicide anneal |
| Unreacted metal removal |
| Interlevel insulator dielectric deposition |
| Interlevel insulator CMP |
| Interlevel insulator post-CMP clean |
| Fully silicide anneal |
| Post-anneal clean |

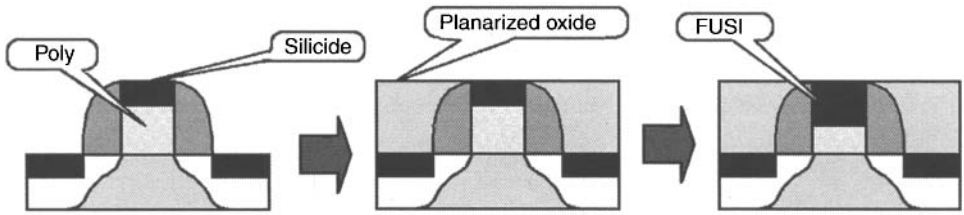



**Figure 7.6.** Schematic of the fully silicided gate process flow with CMP step prior to full silicidation [60]. Reproduced with permission of ECS – The Electrochemical Society from Maszara, W. P., *Journal of the Electrochemical Society.*

FUSI process relies on complete silicidation with a controlled silicide phase to achieve low threshold voltages. Again, some of the steps in Table 7.4 have been simplified. Although the FUSI is not a widespread technology, there is some indication of its use in volume manufacturing.

## 7.2 Surface Preparation and Cleaning

Current high-performance devices require transistor gate stacks to have an EOT, of ~1.0 nm at this thickness polySi gate depletion becomes an inevitable problem, solved by the introduction of metal gates. Since CMOS processing requires fabricating PMOS and NMOS on the same wafer, this necessitates different metal gates, plus potentially different high-κ materials and capping layers for each transistor type. In addition complex interface engineering is necessary between Si and high-κ.

Cleanliness and the proper condition of the silicon surface prior to formation of the interfacial oxide and deposition of the high-κ dielectric are critical. Due to the introduction of HKMG, the following cleaning processes are critical for pre and post-gate fabrication:

1. Pre-gate: Surface preparation and interface engineering – Section 7.2.
2. Post-gate: High-κ removal and post-gate etching clean – Section 7.3 and 7.4.

In this chapter, the items associated with cleaning are broken down step-by-step. This section will cover these pre-deposition cleaning and interface engineering.

### 7.2.1 Surface Cleaning Challenges Prior to High-κ Deposition

The HKMG stack has stringent requirements for surface preparation and cleaning. These same challenges were experienced with the standard polySi gate electrode and $SiO_2$ gate oxide structures. The most critical surface cleaning challenge for HKMG is the formation of a high quality silicon dioxide dielectric interface prior to the deposition of the high-κ dielectric.

This section will discuss the surface preparation and cleaning prior to interfacial oxide formation and the various methods of forming the interfacial oxide on silicon and also on germanium.

### 7.2.2 Pre-interfacial Oxide Formation Cleaning

High-κ layers, whether deposited by ALD or CVD, require a starting surface with a high density of hydroxyl group termination. Traditionally, SC-1 and SC-2 have been widely used for pre-gate cleaning [62]. These RCA cleanings are still promising processes; however, the fundamental problem is that SC-1/SC-2 forms a chemical oxide of 1.0~1.5-nm. Since this interface layer consumes most of EOT, the interfacial thickness must be minimized, typically <1.0 nm. Surface flatness and complete hydrogen termination are also desired prior to high-κ ALD.

Prior to formation of a chemical oxide, the silicon surface must first be freed of any native oxide and any organic contamination. In addition, all metal contamination must be removed, in particular mobile ions that can affect the gate oxide integrity (GOI). Especially lifetime-killer metals, such as Cu and Fe, must be removed as well as metals from the metal gate. To preserve GOI, gate metals must not diffuse into the silicon nor penetrate the gate oxide.

### 7.2.3 Interfacial Oxide Formation

Prior to atomic layer deposition of the high-κ film, the surface of the silicon must be free of defects and atomically smooth. Deposition of the ALD high-κ film directly onto the hydrogen-terminated silicon surface has been attempted to fabricate sharp Si/high-κ interfaces that are oxide-free and Si-H-terminated. Lab results have shown that good quality high-κ dielectrics can be formed, but at very low deposition rates with poor uniformity and, in some cases, with silicide formation [62]. Moreover, when directly compared to an oxidized surface, a Si-H terminated surface shows leakage [63]. Therefore, first attempts to produce high-κ stack on Si-H surfaces were not successful.

Several approaches have been considered for surface treatment prior to gate formation. Yamamoto *et. al.* proposed suppression of surface micro-roughness of silicon by the addition of alcohol into the water [64]. Choi *et. al.* showed that different cleaning methods, such as modified Shiraki clean and RCA clean, have different impacts on interface properties [65]. After high-κ integration, RCA-cleaning resulted in higher density of interfacial traps and thicker interfacial oxide thickness. A new or modified surface treatment was therefore required prior to high-κ formation.

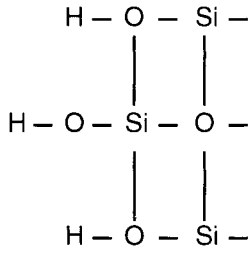
The entire cleaning sequence for successfully forming a high-quality oxide involves the use of traditional formulations to remove the organic, metallic, and particulate contamination on the wafer. Researchers at SEMATECH have used a standard RCA clean (SC-1/SC-2 – standard clean-1 and standard clean-2) with HF-last prior to an $O_3$-based oxidation in order to form the requisite interfacial oxide [66]. Instead of a traditional RCA clean for the surface preparation prior to high-κ deposition, dilute and lower temperature SC-1/SC-2 surface preparations have also been tried. Typically, prior to chemical oxide formation, wafers are etched using dilute HF (DHF) to remove 20 nm of thermal oxide [67]. Hydrochloric acid can also be added to the HF solution, or a separate SC-2 or dilute HCl rinse can be included [67].

In order to prepare the appropriate surfaces for high-κ deposition, different approaches or a combination can be used: chemical or thermal oxidization, etch-back of the oxide formed, and post-processing anneal, including densification and nitridization.

#### *7.2.3.1 Hydroxyl-terminated Surface*

Hydroxyl groups have been found to be necessary for rapid initiation of the ALD reaction on silicon [68]. Kukli and researchers have found that intermediates are formed by substitution of the hydrogen in the hydroxyl group with the ALD precursor molecule. When silicon is passived by chemical oxide (with –OH terminal groups) the ALD growth rate is faster than found on a hydrogen passivated surface. Additionally, the thickness growth rate is linear with respect to the number of ALD pulses [69]. Hydroxyl terminated surfaces can be on either a silicon substrate, with no intermediate oxygen bonding or on a thin silicon dioxide passivating layer. A thin hydroxyl layer is optimum due to the thickness limitation when trying to create an EOT of less than 1.0 nm. This is because the hydroxyl terminated silicon dioxide layer is itself only 1.0 nm thick. Table 7.5 shows the thickness of the oxide and the resultant impact on the ALD deposition.

**Table 7.5.** Termination of silicon surface and impact on ALD. Adapted from [69]. Reproduced with permission of ECS – The Electrochemical Society from De Gendt, S., Beckx, S., Caymax, M., Claes, M., Conard, T., Delabie, A., Deweerd, W., Hellin, D., Kraus, H., Onsia,, B., Parashiv, V., Puurunen, R., Rohr, E., Snow, J., Tsai, W., Van Doorne, P., Van Elshocht, S., Vertommen, J., Witters, T., and Heyns, M., *Cleaning Technology in Semiconductor Device Manufacturing VIII.*

| Termination and Thin Film | Thickness | ALD Result |
|---|---|---|
|  | < 1 nm | Fastest deposition rate<br>Thickest EOT |
| H – O –<br>H – O –<br>H – O – | > 0.3 nm | Island-like or first monolayer |
| H – O – | < 0.3 nm | Island-like |
| H – | 0 nm | Slow Growth |

The optimal silicon surface should be completely covered by a monolayer of hydroxyl groups without any underlying silicon oxide yielding the highest surface hydroxyl density concurrently with the lowest oxygen content. Uniform surface passivation is also optimal because islands lead to a non-uniform formation of the hydroxyl layer that contribute to non-uniform film thickness and surface roughness from delayed nucleation of deposition.

### 7.2.3.2 *Interfacial Oxide Formation*

The formation of this thin uniform oxide film called the interfacial oxide helps enable quality high-κ deposition. Various methods for preparing this surface prior to high-κ deposition exist. These methods include:

1. Chemical oxidation to form a thin oxide film.
2. Thermally grown oxide or oxynitride films.
3. Films grown with the above methods that are subsequently treated to enhance the electrical characteristics.

Wet chemical interfacial oxide formation processes prior to high-κ deposition typically use SC-1 solutions or ozonated deionized water (DIW) rinses. Chemical oxides grown in SC-1 solutions have long been known to be of poor electrical quality primarily due to a high density of interface traps [71] and are not suitable for preparing the surface for high-κ dielectric deposition. The chemical oxide films are also relatively thick compared to the EOT requirements for high-κ films. Chemical

oxides formed by SC-1 are on the order of 1.0 nm, greater than the target value of 0.8 nm or less.

Figure 7.7 shows leakage current densities as a function of EOT with various chemical surface treatments. The DI/$O_3$ chemistry shows the lowest and most stable leakage current behavior. Based on these results, DI/$O_3$ dominated the wet surface treatment. For the combination HF-$O_3$ process, HF removes the native oxide, and $O_3$ creates the chemical oxide. This combination is easily implemented into manufacturing with existing process chemicals, plus it can be completed in a single wet cleaning system with minimal process steps.

The use of ozone dissolved in DIW (DI/$O_3$) is another choice for interfacial oxide formation. Because ozone rapidly oxidizes silicon, control of the reaction time, temperature, and concentration of the mixture are imperative. However, chemical oxide thickness and quality are difficult to control. Onsia and coworkers have shown that controlled oxide thickness (~1 nm) can be obtained with commercially-available processing equipment [72]. The authors found that control of the uniformity was dependent on the processing conditions and that lower concentration of ozone yielded thinner oxides and also more uniform films. They also found that scavenger addition can prevent ozone decay leading to better uniformity.

Unlike gaseous $O_3$ oxidation where uniform layer-by-layer oxidation occurs across the entire silicon surface, DI/$O_3$ oxidation occurs by first forming islands followed by filling in of the empty spaces. Saturated growth is defined by the formation of a monolayer of silicon dioxide across the entire hydroxyl-terminated surface. Studies have shown that ALD-grown high-κ films exhibit heterogeneities 8-9-nm in diameter and porosity at the interfaces [73]. These features are likely caused by defects in the exposed surface that result in initial coalescence of the ALD precursors on areas that have the highest concentration of reaction sites. These film features are not observed in the bulk film.

Growth of Hf-based high-κ material was shown by Green and colleagues to have optimum nucleation when large concentrations of OH groups are present in the interfacial chemical oxide [74]. When this occurs, there is stable linear growth with constant film density and a continuous $HfO_2$ film grown uniformly in two dimensions. They compared the OH-saturated chemical oxide film with Si-H and

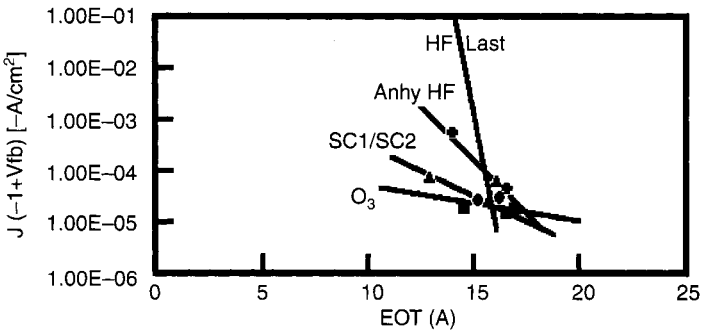



**Figure 7.7.** Leakage current densities of a high-κ stack as a function of EOT with respect to various chemical surface treatments [72]. Used with permission from SEMATECH.

SiON surfaces and found that a OH-saturated film yields the best physical and electrical characteristics.

Early studies of low-temperature oxide formation using DI/$O_3$ proposed that the silicon oxidation was limited by the amount of ozone available, but not in a true diffusion-limiting reaction because of electropotential contributions [75]. The researchers used the Cabrera-Mott model [76] to assess the formation of DI/$O_3$-formed oxide. Oxidation is proposed to occur with the following mechanism:

1. An activated O anion ($O^{-2}$) reacts with Si on the surface.
2. An electric field is created between the Si and the $O^{-2}$.
3. Fowler-Nordheim tunneling for both holes (p-type Si) and electrons (n-type Si) occurs.
4. The O anion has enough energy to overcome the activation barrier and to react with the Si at the interface.

Figure 7.8 shows the dependence of oxide thickness on the time exposed to the DI/$O_3$ at two different concentrations. The graph shows that the oxide thickness is self-limiting for 10-ppm $O_3$, and the oxide growth rate is impaired at concentrations of 1 ppm and less. A similar trend is observed with higher temperatures – the maximum thickness increases, but the oxide is still self limiting. The pH of the solution is also found to influence the oxide growth rate [77].

To obtain uniform oxide growth, researchers have developed methods to achieve high-quality oxide. One method used by Butterbaugh *et al.* controls the uniformity of oxide films grown with ozonated water by first growing a saturated oxide film followed by uniform etching with dilute HF (approximately 400–800:1 $H_2O$:49 wt% HF) [78]. They found that decreasing the oxide concentration decreased the film thickness, but increased the film non-uniformity. Therefore they formed a thicker film (0.8–1.0 nm), and then used a controlled etch-back process to obtain the

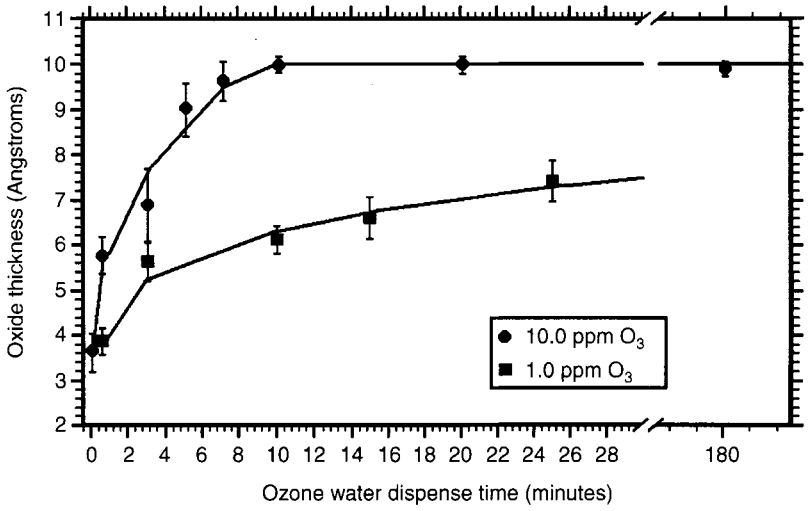



**Figure 7.8.** Chemical oxide thickness *vs.* time for two different concentrations of ozone at 22°C [75]. Courtesy of FSI International.

desired film thickness of 0.3–0.6 nm. Using less than 10 ppm ozone concentration showed difficulty in controlling the specific thickness.

Sano and coworkers used a low concentration of $O_3$ (1 ppm) in the a single wafer spin system to produce a uniform thin oxide [79]. They also reported that a single-wafer system was favored over a batch system. While the batch system showed 5.4 σ% non-uniformity for 0.7-nm oxide, the single-wafer system showed 2.3 σ% at 0.7-nm. They showed that dilute ozonated water is capable of forming a uniform and saturated thin film on a Si surface. The optimum thickness was greater than 0.7 nm because the leakage current was high at lower thicknesses of oxide. This suggests that lower thicknesses are not fully covered by hydroxyl-terminated groups. Transmission electron microscope images showed bare spots where no oxide was formed, and electron energy loss spectroscopy (EELS) also confirmed that O was not present on the surface, further supporting the island-growth theory.

Additives such as HCl and acetic acid have been proposed by *Onsia et al.* to offset the decay of $O_3$, and to increase the oxide thickness by increasing the pH [75].

A comparison of the interface layers formed with SC-1/SC-2 and $O_3$ are shown in Figure 7.9. The interfacial oxide formed by the $O_3$ cleaning step followed by a $NH_3$ anneal at 600°C has a visibly more distinct interface and a smoother film than that formed with SC-1/SC-2, but this oxide yielded a lower EOT [66]. The $O_3$ process had a more uniform leakage current across the 200-mm wafer. Under any of these conditions, exposure of the thin oxide to air augments the film; therefore, exposure should be avoided to maintain the high-quality oxide.

### 7.2.3.3 *Thermal Oxidation*

Thermal oxide formation is also a good candidate to create interfacial layers. Beside chemical oxide formation, interfacial oxide, and sometimes oxynitride can be grown using high temperature processing. Since leakage is one of the reasons thin gate dielectric films fail, research has been ongoing to find a method to grow thin high-quality $SiO_2$ that has low interface trap density and good mobility. Rapid thermal oxidation for interfacial oxide formation has been accomplished [80]. Formation of the oxide *in situ* by single wafer RTP allows the substrate to be

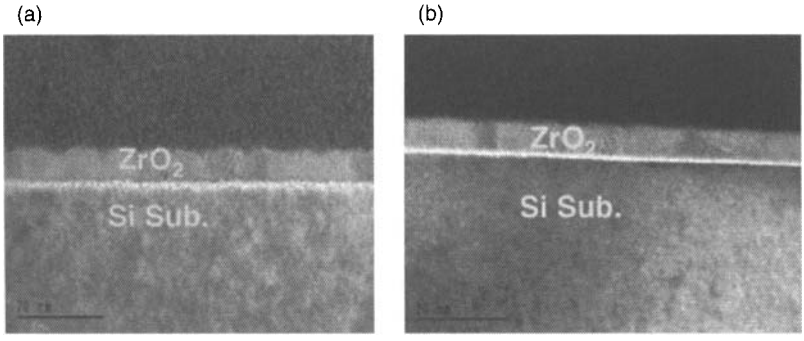



**Figure 7.9.** Transmission electron microscope images of interfacial oxide layer cleaned with a) SC-1/SC-2 and b) $O_3$, followed by a 600°C $NH_3$ anneal [66]. Used with permission of *Future Fab International.*

transferred from the RTP chamber to the ALD chamber without breaking vacuum retaining the high-quality oxide characteristics.

*In situ* steam generation (ISSG) oxidation [81] is one of these methods used to form high-quality pre-ALD interfacial oxide. Originally, ISSG oxidation was used for forming thin gate dielectric film prior to the high-κ era. The ISSG process uses $H_2$ and $O_2$ in a RTP chamber (~1050°C) that reacts to form $H_2O$ [94]:

$$2\,H_2 + 2\,O_2 \rightarrow H_2O + O^* + 2\,OH \tag{7.2}$$

This method is speculated to form a dense oxide with few dangling or strained bonds because of the generation of O* radicals that can react with these bonds to form stochiometric $SiO_2$ [83]. This oxide has been shown to be superior to other steam generated oxide processes [84].

After considering several approaches, ISSG has been shown to form high-quality interfacial oxide, after a 2-nm film is grown and etched back [67]. The saturation current data was 5~10% higher for all device lengths tested.

Other work has shown that the use of water vapor at high temperature (350–400°C) yields a thin 6-Å oxide with the appropriate hydroxyl termination groups to facilitate ALD high-κ dielectric deposition [85]. The researchers suggested that the oxide formation on HF-last, hydrogen-terminated silicon surfaces became hydroxyl-terminated after hydrogen was desorbed at ~350°C.

Methods to improve the quality of the gate oxide after growth have been undertaken. One such method has been reported by Chang *et al.* using ultraviolet-enhanced and gaseous HF processing [86].

### 7.2.3.4 *Nitrided Surfaces*

For further improvement, silicon nitride (SiN) or silicon oxynitride (SiON) have been considered for sub-nm interfacial oxide [87]. A mono-layer film of silicon nitride could perform as a diffusion barrier. Additionally, ultraviolet (UV) light can provide uniform N-termination of the silicon [88]. On the other hand, Tsujikawa *et al.* also reported high nitrogen concentration leads to carrier mobility loss [89].

Silicon nitride layers with a dielectric constant of about 7.2 have been prepared by ALD [8]. Chemically or thermally grown oxide/oxynitride films on Si, preferably with a high density of terminal hydroxyl groups, are excellent nucleation layers for CVD and ALD-grown dielectrics. However, to maximize capacitance, an interfacial layer with an EOT <1 nm is required, motivating the development of alternative surface treatment schemes. This requires an evolutionary approach to electrically thin interfacial layers by the use of high nitrogen concentration SiON or pure silicon nitride. Hydrogen-terminated silicon with $NH_3$ pre-treatment for $Al_2O_3$ ALD deposition has been shown to provide an effective barrier against interfacial $SiO_2$ formation and promote the nucleation of $Al_2O_3$ growth [90]. Nitride layers thicker than 0.3–0.4 nm were shown to provide an adequate barrier.

### 7.2.3.5 *Hydrogen-terminated Surface*

Deposition of high-κ materials directly on silicon has proved challenging because of the inter-diffusion of the metals from the high-κ dielectric into the silicon and

Next Page



*visa versa*. Also, direct deposition of the high-κ material by ALD processing on the H-terminated silicon poses a significant nucleation barrier.

Under the right conditions, the H-terminated surface can be transformed to one that nucleates the high-κ film precursors [91]. The researchers detected a $SiO_x$/SiOHf interfacial layer by angle resolved x-ray photoelectron spectroscopy (ARXPS) after multiple (>6) ALD cycles. Frank and collaborators have shown that on H-terminated surfaces nucleation can take place initiated by the organometallic precursors [92]. The reaction of the precursor, tetrakis-ethylmethylamino hafnium, takes place directly with the Si-H bond progressing from Si-H to Si-O-Hf, to $HfO_2$ [93]. The $SiO_2$ that is observed at the interface is apparent only after the annealing step. The $SiO_2$ interfacial film is critical. When this layer does not exist, silicide formation may occur leading to a decrease in electron mobility. A unique process has been proposed –sputtering Hf, Zr, or Al directly on an HF-last cleaned silicon surface, then annealing in an oxygen furnace [90]. However, an oxygen-free interface, and intermixing have proven challenging.

### 7.2.4 High-κ Deposition on Germanium

Germanium has intrinsically higher mobility than silicon and is currently under investigation as an alternative to improve transistor performance. Formation of thin high-quality germanium oxide before high-κ dielectric deposition is challenging, not only because the oxide is thermodynamically unstable, but because of the inability to form a passivating layer by simple oxidation or wet chemical methods. Germanium oxidation and passivation is covered in detail in Chapter 12. Early work with germanium used ozone to form an oxide prior to high-κ deposition after a HF vapor exposure or water rinse to remove the native oxide [94].

Germanium interfacial dielectric layers composed of $GeO_x$ or $GeO_xN_y$ are proposed to inhibit Hf diffusion into the germanium substrate [95]. Prior to interfacial oxide formation, the wafers were cleaned with a 50:1 HF solution. The nitrogen-containing interfacial oxide appears physically rougher than the $GeO_x$ interfacial oxide but shows better electrical properties due to the reduction in the defect density attributed to poor quality $GeO_x$. Figure 7.10 shows TEM images of the high-κ

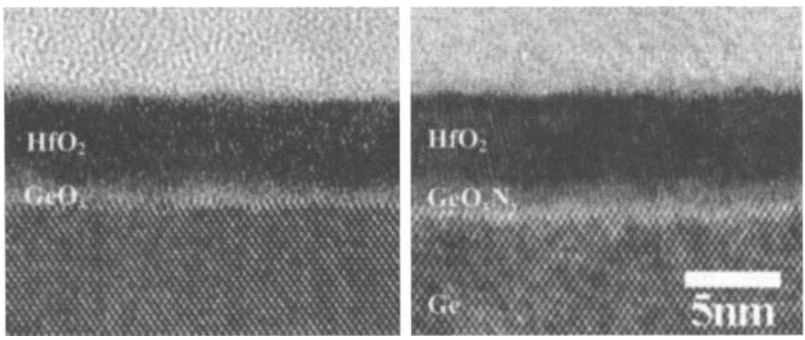



**Figure 7.10.** Transmission electron microscope images of interfacial oxide layer on germanium of a) $GeO_x$ or b) $GeO_xN_y$ [95]. Used with permission from Kim, H., McIntyre, P. C., Chui, C. O., Saraswat, K. C., Cho, M.-H, *Applied Physics Letters*, 85(1404):2902 (2004). Copyright 2004, American Institute of Physics.

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# 8

# High Dose Implant Stripping

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*Abstract*
Specialized processes have been developed for high dose implant stripping (HDIS) because of the difficulty in removing the highly cross-linked and carbonized photoresist crust. Traditional plasma followed by wet processing has limitation due to the silicon loss, and all-wet processing has limitations due to the implant dose and energy creating a damaged crust layer that cannot easily be removed with standard processing chemicals. This chapter discusses the definition of high-dose implant, the formation of the crust, the methods to remove the crust and the bulk photoresist, the limitations of the processes plus newly developed methods to address these limitations.

***Keywords***: high-dose implant stripping, photoresist stripping, sulfuric acid hydrogen peroxide mixture, hydrogen plasma, photoresist crust, silicon loss, junction loss

## 8.1 Introduction and Overview of High Dose Implant Stripping

Post-ion implant photoresist is challenging to completely remove due to the high doses of the ions that are implanted into the photoresist because the photoresist is cross-linked and dehydrated during the process. Plasma stripping followed by a wet cleaning process, typically SPM (sulfuric acid hydrogen peroxide mixture) sometimes followed by SC-1 (standard clean-1), is the process of record at most IC (integrated circuit) manufacturing facilities. Due to the loss of the silicon substrate during the plasma and SC-1 processing steps and also due to the change in materials for the gate electrodes that are incompatible with SPM and SC-1, alternative methods are being developed and current methods are being optimized for high dose implant stripping (HDIS). This chapter will discuss the challenges of high dose implant stripping, the effect of the implant on the photoresist, and the methods for removing the implanted photoresist.

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### 8.1.1 High Dose Implant

High dose implants are used when shallow source/drain junction extensions are formed, when the polysilicon gate material is doped for CMOS (complementary metal oxide semiconductor) devices, and when a collector implant is needed for BiCMOS (bipolar-CMOS) and bipolar devices. Figure 8.1 shows the ranges of doses for various implants [1]. High dose is usually defined as doses greater than $5 \times 10^{14}$ atom/cm$^2$ for As, P, B, or $BF_2$. Implantation can be performed using ionized beamline or plasma doping implantation.

As scaling of CMOS devices progresses, ultra-shallow low-energy implants are used to define the source/drain extension. In some cases the depth of the implant can be on the order of several hundred angstroms or less [2]. The ultra-shallow junctions (USJ) are heavily doped with abrupt profiles and low sheet resistivity, generated by low energy implants causing the dopant to reside very close to the surface. Figure 8.2 shows an example of the doping profile obtained by $Cs^+$ SIMS (secondary ion mass spectroscopy) for an arsenic $1 \times 10^{15}$ atoms/cm$^2$ implanted at 5 keV showing the penetration depth to be approximately 150–200 Å. An example for ultra-low energy boron implant, plotting the cumulative dose *vs.* depth; approximately 100 Å for 0.5 keV implant energy, [3] is shown in Figure 8.3. Significant challenges arise when stripping photoresist after the shallow source/drain extension implant for logic devices. In particular the loss of the silicon, silicon dioxide, and dopant and their affect on the electrical properties of the device will be discussed in Section 8.1.5.

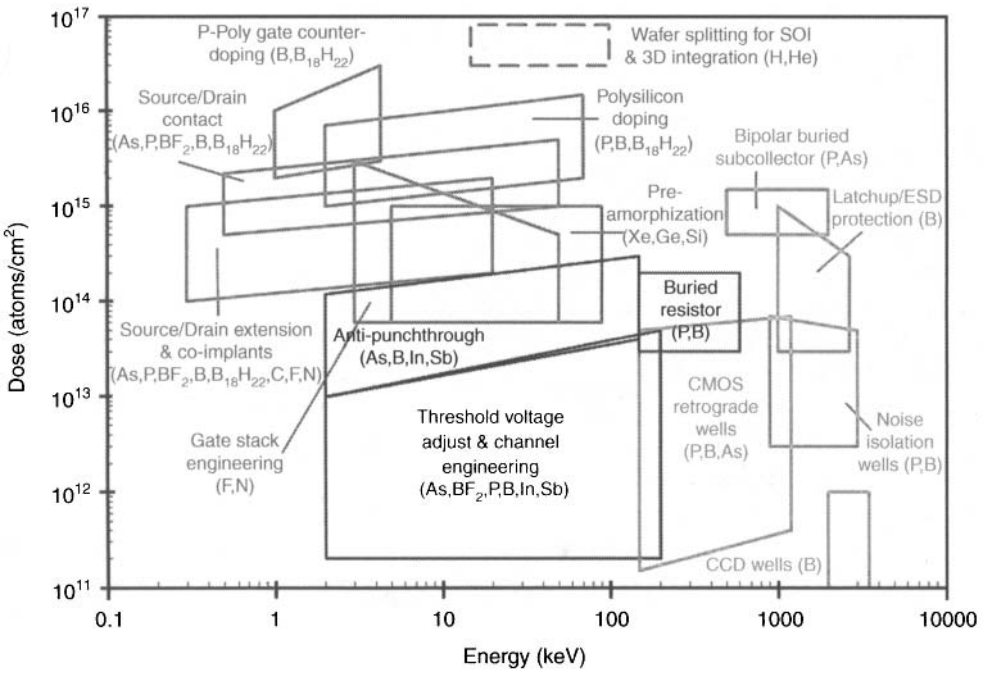


**Figure 8.1.** The high dose implant regime is defined as greater than $5 \times 10^{14}$ atoms/cm$^2$. Various implant layers are shown that use high doses. Adapted from [1]. Updated 2010 and used with permission from Axcelis Technology.

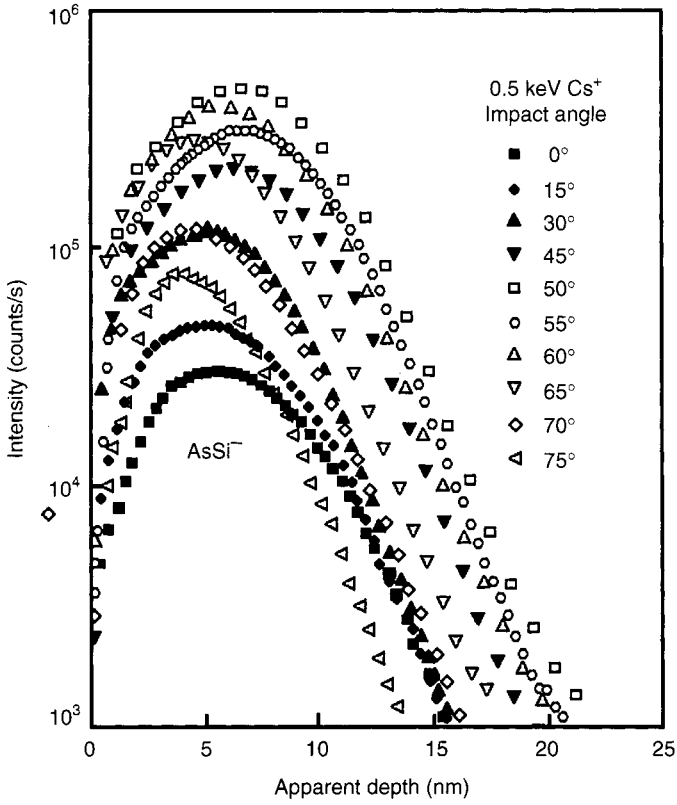


**Figure 8.2.** Arsenic depth profiles obtained by SIMS for $1 \times 10^{15}$ atoms/cm$^2$ implanted at 5 keV [2]. Used with permission of Fujitsu, from Kataoka, Y., Shigeno, M., Tada, Y., Yamazaki., K., and Kase, M., *Fujitsu Sci. Tech. J.*, 38(1):69 (2002).

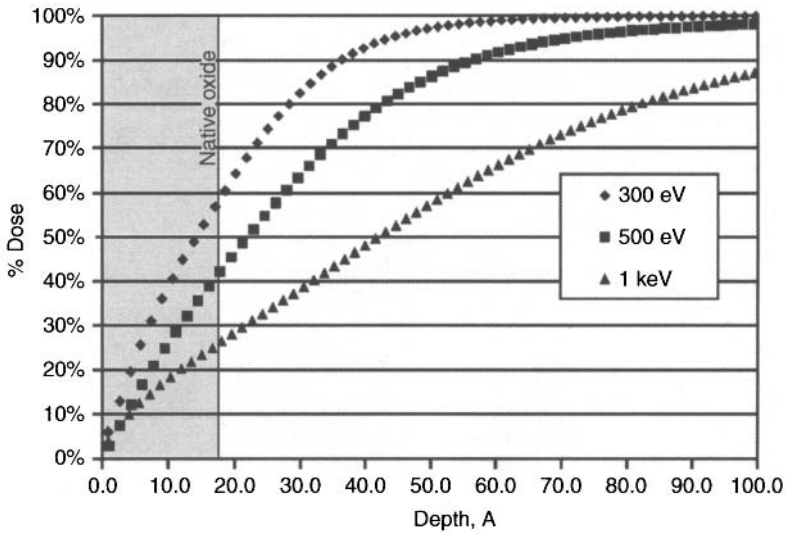


**Figure 8.3.** Cumulative dose *vs.* depth of $B^+$ implant at $1 \times 10^{15}$ atoms/cm$^2$ [3]. Used with permission from Axcelis Technologies.

## 8.1.2 Photoresist Modifications Due to Implant

After hard baking and prior to implantation, dissolved in the photoresist film is a low concentration of solvents and also $N_2$ formed during the exposure process [4]. There is no crust on the surface, and the photoresist resin is similar to the composition as first applied. As early as 1978, Okuyama surmised the physical effects caused by high dose implant resulted in the resist being cross-linked due to bonds being broken during the implantation process resulting in a highly carbonized crust layer [5]. Infrared (IR) spectroscopy analysis showed that the photoresist hydrocarbon structure was reduced and the remaining structure was carbonaceous; "graphitization" was the term used by Okuyama.

Figure 8.4 shows the IR spectrum of the implanted photoresist compared to the unimplanted photoresist; the implanted photoresist is devoid of any spectral peak and similar to graphite. Also, the resist is dehydrated and the solvents that are uniformly distributed in the bulk photoresist have been out-gassed in the top layer, shrinking the photoresist layer and the critical dimension of the pattern [5].

Lee *et al.* in 1988 further characterized the photoresist by FTIR (Fourier transfer infrared) spectroscopy [6]. The absorption band assigned to the aliphatic C-H bond stretch at 2820–2995 $cm^{-1}$ was analyzed as a function of ion species and ion energy. Decrease in the C-H bonds was used to monitor the degree of carbonization

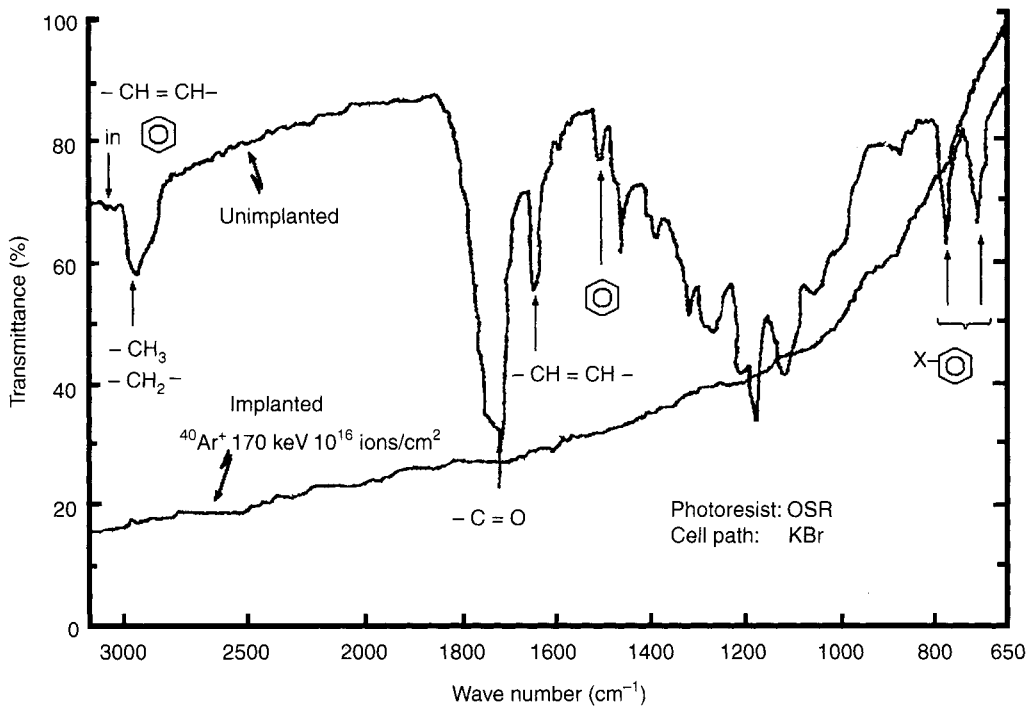


**Figure 8.4.** Infrared transmittance spectrum of photoresist before and after implantation. The base polymer of photoresist, OSR, is manufactured by Tokyo Oka Kogyo, is poly(-vinyloxyethylcinnamate), a negative tone resist [5]. Reproduced with permission of ECS – The Electrochemical Society from Okuyama, Y., Hashimoto, T., and Koguchi, T., *Journal of the Electrochemical Society.*

caused by the ion implant. A substantial decrease in these bonds after implant resulted, and also was observed by Okuyama. Raman spectroscopic analysis by Kawaguchi *et al.* [7] indicates that the organic composition of the crust is a mixture of sp2 graphite- and sp3 diamond-like carbon structures, confirming the "graphitization" observed by Okuyama. Additionally, the hydrogen content of the resist was reduced approximately 50 atomic% after high dose ion implantation, as measured by hydrogen forward scattering.

Orvek and Huffman recognized that after high dose implant processes the pattern integrity is compromised and the resist becomes difficult to remove [8]. They used scanning electron microscopy (SEM) to visually explain the changes in the photoresist after implantation. Selective etching of the unaffected photoresist under the carbonized layer revealed the crust, not only on the top but also on the sidewall. They found that the crust is dependent on the ion energy of the implant and also is depended on the species implanted; the higher the ion energy and the smaller the species size, the thicker the crust that is formed. However, the beam current, which is proportional to the energy input to the wafer, did not have a large effect on the crust thickness [8]. The graph in Figure 8.5 shows the dependence of crust thickness upon ion energy.

Okuyama, Lee, and Overk showed that the application of heat did not change the photoresist; only upon implantation was the bonding structure altered for both the top portion of the photoresist and on the sidewall. The photoresist is relatively

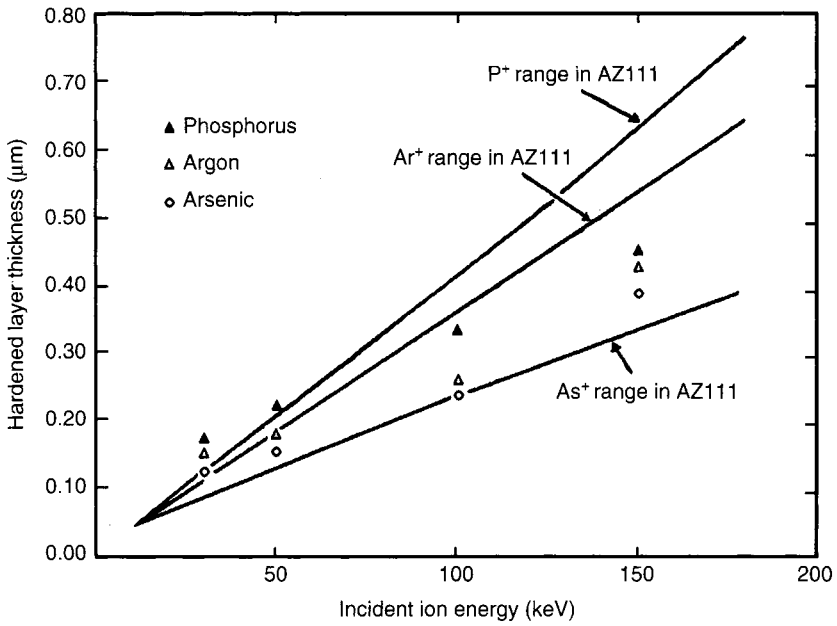


**Figure 8.5.** Plot of the thickness of the carbonized crust layer as a function of the ion energy for various implants. The photoresist is AZ®111 manufactured by AZ Electronics Materials. The lines are the calculated maximum thickness of the crust layers, the actual averages are designated by the symbols [8]. Reprinted from *Nuclear Instruments and Methods in Physics Research*, B7/8, Orvek, K., and Huffman, C., "Carbonized Layer Formation in Ion Implanted Photoresist Masks", page 501. Copyright (1985) with permission from Elsevier.

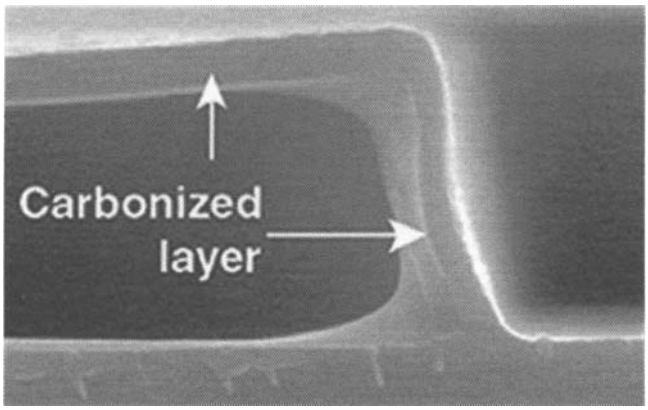


**Figure 8.6.** Cross section SEM of high dose ion implanted photoresist at 50 keV, 15 mA, $As^+$. For illustration, a delineation etch removed the unchanged resist leaving behind only the heavily carbonized crust [9]. Used with permission from Axcelis Technologies.

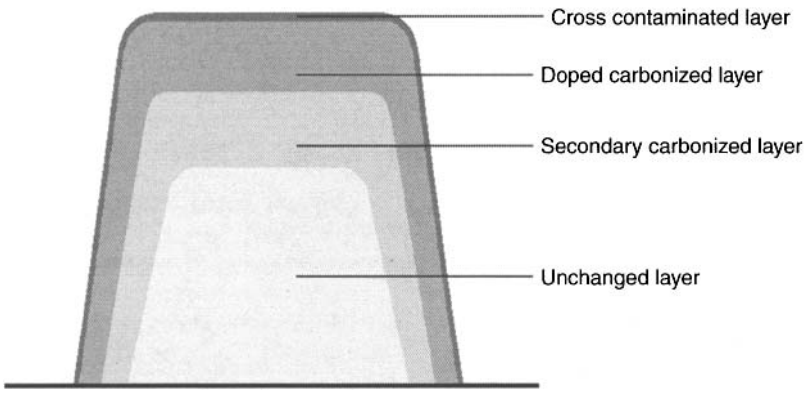


**Figure 8.7.** Gradient of the photoresist, adapted from [10]. Used with permission of the authors.

untouched under the crust, clearly shown by the SEM photos taken by Orvek and Huffman [8]. Figure 8.6 shows a cross section of a photoresist line with the unaltered layer etched from under the crust layer. The crust layer is clearly seen.

Fujimura, Konno, and their research team characterized the crust using x-ray photoelectron spectroscopy (XPS) and nuclear magnetic resonance (NMR) [10]. The photoresist used was a cresol novolac-based resin with both aromatic and aliphatic groups. They found that the crust is thicker than the mean depth of the implant indicating that dehydration and cross-linking is deeper than implanted species can penetrate. The crust shows various gradients due to the implant; the crust layer is composed of the highly cross-linked and highly doped augmented photoresist, the "cross contaminated layer" mostly on the surface, then a less cross-linked, lighter doped layer, the "doped carbonized layer", next a secondary doped layer with less cross-linking and little doping, the "secondary carbonized layer", and finally, the unchanged layer with no cross-linking and no doping, as illustrated in Figure 8.7. They found that both dose and energy impact the crust thickness and the maximum density of the species in the crust. Additionally, they have proposed the structure of the cross-linked photoresist, as shown in Figure 8.8.

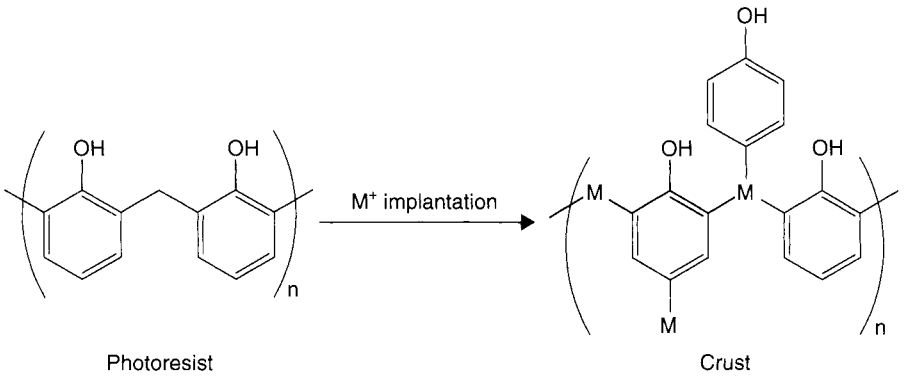


**Figure 8.8.** Proposed chemical reaction between the high-dose ion-implant (M = B, P, or As) and photoresist [10], as interpreted by [12]. This reaction results in the hard to remove crust (highly cross linked polymer). Reproduced with permission of ECS – The Electrochemical Society from Visintin, P. M., Korzenski, M. B., and Baum, T. H., *Journal of the Electrochemical Society*.

Conversely, Trevetanova *et al.* has characterized arsenic implanted DUV photoresist and found by micro Raman spectroscopy and solid state nuclear magnetic resonance (NMR) that no amorphous carbon is found in the crust [11]. In-depth analysis has shown with ion bombardment three different effects are observed: chain scission, crosslinking, and hydrogen/oxygen loss. At very low doses and light mass ions, the chain scission dominates, at moderate doses and heavy mass ions, crosslinking is the dominate mechanism, and at some high doses and high mass ions, enough oxygen and carbon are lost that only carbon remains. Research is ongoing to further characterize these phenomena.

Work by Smith confirmed that the crust layer thickness varies upon dose, energy, and implant species. In 1983 he estimated the thickness of the crust resulting from implant using an equation that takes into account these parameters [13] and later refined the model [14]. He recognized that the implant species had high enough energy to break the bonds of the organic photoresist and also outgas the solvent-rich material. The damage to the photoresist releases hydrogen causing the photoresist to shrink from the original thickness. Smith also recognized that this phenomenon is independent of the type of organic photoresist.

Investigation by Christenson in 2007 showed that the primary factors controlling crust formation appear to be dose, energy, and implant species. Other factors that contribute to crust formation including the implant dose rate, beam raster speed, beam return path, wafer cooling, photoresist resist thickness, and sidewall profile [15]. Christenson calculated the effects of the implanted ions on the photoresist using the "stopping range of ions in matter" (SRIM) computer simulation [16, 17] with a resist stoichiometry of $C_5O_2H_8$, a density of 0.95 g/cm$^3$, for boron, phosphorus, and arsenic implants with energies varying from 1 to 160 keV. Christenson [15] proposes three damage mechanisms that contribute to formation of the crust layer:

1. Concentration of implanted ions.
2. Ionization.
3. Collisions.

The damage and cross linking of the resist layer scales linearly with the dose; higher concentration of implanted ionic species leads to more damage due to the number of potentially damaging incidents. Moreover, the concentration of implanted ions was shown to vary from the surface into the bulk film confirming Fujimura's results. Christenson has demonstrated through modeling that the crust extends to the surface of the feature whereas the maximum concentration of implanted species occurs well into the feature. The second damage mechanism involves the energy transferred to the electrons of the photoresist molecules by the implanted ions, thus resulting in ionization of these molecules resulting in the breaking of chemical bonds and the loss of volatile species such as $H_2$ or $O_2$ leaving primarily amorphous carbon as observed by Smith and others. The final damage mechanism involves the collision of the species; at high energies, the peak level of collision damage varies slightly with increasing energy, as shown in Figure 8.9. Increasing the ion energy resulted in a thicker layer of crust, but it does not significantly increase the peak level of damage within the crust.

Plasma doping concentrates more of the dopant species close to the surface than beamline implantation; consequently, Christenson observed that the peak level of collision displacements is a function of species and energy and the peak displacement rate decreases rapidly at low energies [15].

### 8.1.3 Post-photoresist Removal Residue

In addition to the crust layer, residue from the implantation creates processing challenges; implant residue consisting of a matrix of the dopant and other material are also observed and $SiO_2$ may be sputtered from the barrier layer and reside on the top or sidewall of the photoresist. Metallic contamination arising from the resist is

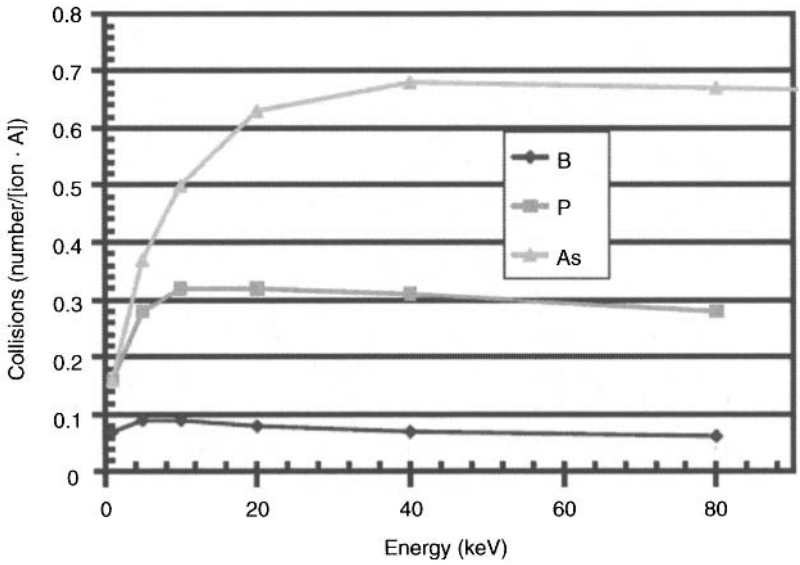


**Figure 8.9.** The peak level of collision events as a function of ion energy and implanted species [15]. Reproduced with permission of ECS – The Electrochemical Society from Christenson, K., *ECS Transactions*.

also present, as with other resist stripping processes. Residue concentration and composition can depend on the lithography pattern, the resist composition, the implantation processes, the type of implant system, the implant parameters, and the stripping and cleaning processes. Most likely not all instances of residues associated with high dose implant photoresist stripping have been documented in the literature; however, many have been thoroughly characterized. This section outlines the residue that has been frequently observed.

Draper *et al.* observed that an amorphous form of elemental arsenic was present as residue after implanted photoresist stripping in $O_2$ plasma and SPM [18]. The As residue was relatively free of oxygen or carbon, was stable for long periods of time, did not react with Si substrate, and was not at a higher concentration near the surface. Also a high concentration of the residue was observed at the interface where the photoresist served as the implant mask appearing as round droplets, as shown in Figure 8.10. The arsenic residue was present at implant

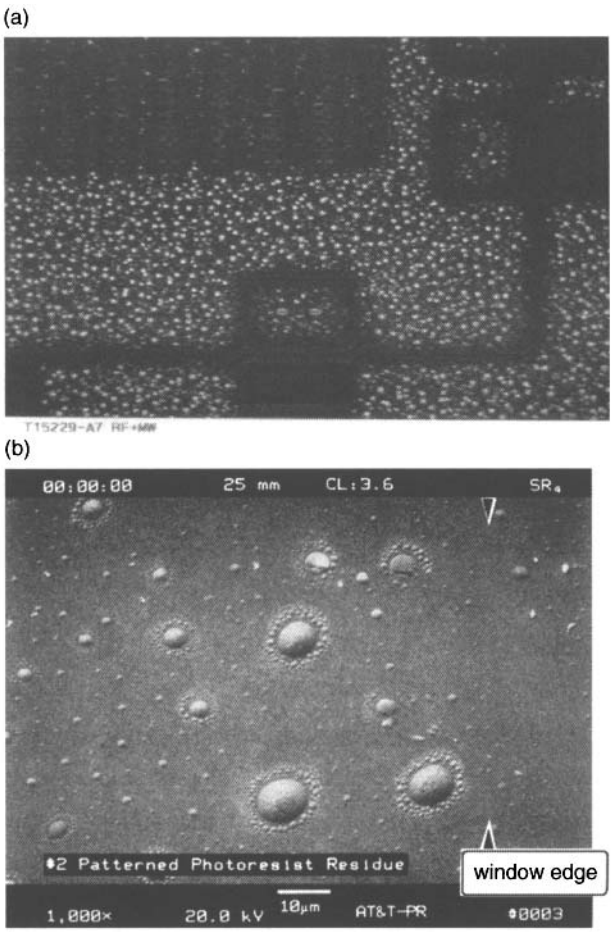


**Figure 8.10.** Examples of implant residues after stripping and cleaning. (a) Micrograph of post-$O_2$ plasma resist strip implant residue. Used with permission of Novellus Systems. (b) SEM of post-plasma resist strip and SPM clean arsenic implant residue [18]. Used with permission from Material Research Society, reprinted from Draper, C. W., Pearce, C. W. Glick, J. T., Gordon, M., Olness, G. E., Bernasek, S. L, *Journal of Material Research*, Vol. 12, Pittsburg, PA, (1997) page 2799.

doses of $3.0 \times 10^{15}$ atoms/cm$^2$ at 35 keV ion energy with 6 mA beam current and $1 \times 10^{16}$ atoms/cm$^2$ at 100 KeV with 8 mA beam current and was independent of the type of photoresist. Since elemental arsenic has low solubility in water and SPM, the residue was not removed in the post-plasma wet cleaning process. Hydrofluoric acid was used to etch the $SiO_2$ and lift-off the arsenic residue.

Oxidized dopant residues, possibly due to oxidation during the $O_2$ plasma stripping process have been observed [10, 19]. The implanted species may be oxidized to $As_2O_5$, $P_4O_{10}$, and $B_2O_3$, none of which are volatile, and all are slightly hydroscopic. These residues may not be observed immediately after stripping, but can appear as a function of time because of their hydrophylic nature. However, unlike the elemental form, these residues are all water or acid soluble although $As_2O_5$ is only slightly soluble, and can in some cases be rinsed off the wafer. Figure 8.11 shows examples of residue arising from the implanted species.

Sputtering of the silicon surface is a byproduct of the implant process and leads to residue that cannot be removed with oxygen plasma or SPM. Residue appears as long strings or spider-like threads that can be observed microscopically [19]. Figure 8.12 shows an example of a densely spaced line before and after stripping. Examples Kadavanich *et al.* performed analysis of residue found on the wafer surface after an $O_2$ or 4% $H_2/N_2$ (forming gas) plasma stripping process [20]. Employing Auger electron spectroscopy (AES), they found, that the string-like residue was composed mainly of silicon and oxygen, and thus surmised a silicon oxide species. Using SRIM calculations, they estimated 3–4 monolayers of Si are sputtered at the implant conditions of $5 \times 10^{15}$ atoms/cm$^2$ at 30 keV. Also, using scratch testing, they found the residue to be fairly dense and strongly adherent to the surface.

For implanted species that are predominantly found as surface contaminants, heavy metal contamination can also occur and is surmised to come from the impurities in sulfuric acid [18] or the photoresist [21]. Draper also discusses other surface contaminants including amorphous carbon, crystalline graphite, arsenic-rich string-like features, very fine transition metal particulates, and hardened photoresist flakes.

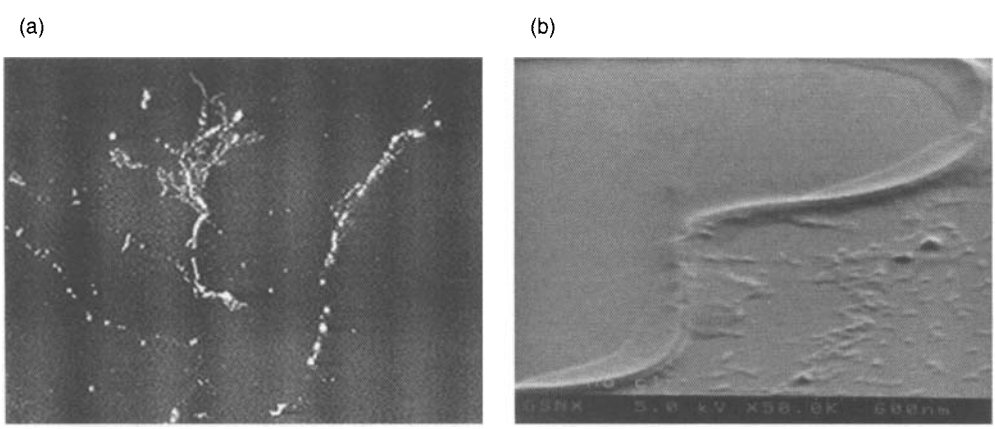


**Figure 8.11.** Examples of residues after stripping and cleaning. (a) Micrograph of post-$O_2$ plasma sputtered residue [19]. Reprinted from *MICRO*. Copyright Tom Cheyney, Los Angeles, CA. Used with permission. (b) SEM of post-$O_2$ plasma resist strip residue, showing delineation at edge of lithography feature. Used with permission of Novellus Systems.

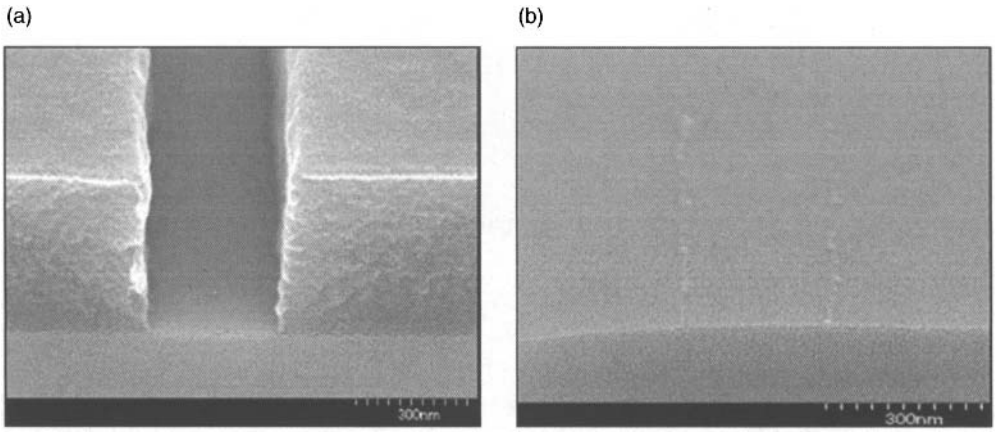


**Figure 8.12.** Example of a densely patterned region for a high-dose arsenic-implant wafer (a) before cleaning and (b) after cleaning showing remaining residue [12]. Reproduced with permission of ECS – The Electrochemical Society from Visintin, P. M., Korzenski, M. B., and Baum, T. H., *Journal of the Electrochemical Society*.

Edge effects were observed by Christenson [15]; the thick photoresist edge bead that is not removed during the patterning process is especially susceptible to being unreactive to wet-cleaning only processes and can redeposit on the surface or clog filters.

The highly cross linked and carbonized crust layer has low chemical reactivity in both plasma and wet cleaning processes. Cross-linked photoresist is observed to be very underactive even in plasma oxygen environments; a high temperature is needed to remove the crust. For the most part, this crust layer is inert to most wet chemicals. Graphite and diamond-like films are unreactive in $O_2$ unless under extreme conditions, for graphite >500°C, although the crust is not cross linked to this extreme, nevertheless, the carbonaceous crust layer is difficult to remove and will be discussed in Section 8.2.

### 8.1.4 Silicon Loss and Silicon Dioxide Formation and Loss

In addition to the photoresist being affected by the implant, the silicon can also be damaged, leading to oxidation and high etching rates. Lui and coworkers observed that the rate of removal with dilute HF solution of the oxide exposed during the implant is significantly higher than unexposed oxide [22], possible due to the breaking of the Si-O bond. After annealling at 700°C the oxide recoverd to the same etching rate. This has implication for wet cleaning and also plasma stripping where the oxide can be etched during the process.

Silicon damage caused by ion implantation was recognized in 1972 by Gibbons [23]. Numerous studies of the silicon damage induced by implantation have been performed with the conclusions:

1. Formation of amorphous layers and damaged crystalline layers.
2. Localized layers and regions of amorphous silicon.
3. Continuous layers and regions of damage silicon with crystal defects.
4. Defects include vacancies and interstitials.

The damage to the silicon also has implications for wet and plasma cleaning; these damage areas are more prone to reaction with the processing chemicals and the damaged layer also can be removed at a faster rate than undamaged material.

Processes necessary to remove the implant residues may require the use of oxidizing chemistries to remove carbonaceous materials or fluorides to remove the silicon-containing materials. However each of these can result in unwanted effects such as etching and oxidation of the substrate or other features of the device, especially the implant-damaged material. These detrimental effects include silicon loss that may lead to a decrease in the concentration of implant at the top surface of the junction thus causing an increase in sheet resistivity and to doping deactivation where the implanted species is not longer in the crystalline lattice. This Si loss can also manifest as current leakage due to film removal under the gate structure. Silicon loss caused by plasma oxidation may increase the surface concentration by dopant segregation and pileup. Silicon dioxide loss especially before annealing may remove the dopant by out-diffusing and evaporation or, in the case of loss, through oxidation enhances the dopant concentration since the grown $SiO_2$ layer prevents the dopants from escaping during the high temperature step [24]. Although keeping a barrier layer of $SiO_2$ on the Si surface is desirable, consuming Si by the formation of $SiO_2$ is not desirable. Also, the oxidation process is isotropic and the Si under the gate electrode may be undercut causing detrimental junction leakage.

Plasma oxidation is considered a major cause of silicon loss during resist stripping. Different theories exist for the mechanism of oxidation by plasma, reviewed in reference [25]. One theory is the plasma oxidation is comparable to thermal oxidation; similar to the Deal-Grove oxidation model proposed by Kim *et al.* [26] who states that the diffusion rate constant of $O_2$ through the $SiO_2$ to the Si is enhanced up to the diffusion rate for thermal oxidation; in other words, the oxidation is enhanced in $O_2$ plasma for the thin layers encountered for high dose stripping. The researchers, who used ECR (electron cyclotron resonance) plasma, which are comparable to downstream plasma, theorize that due to oxygen atoms dissociated by the plasma, the oxidation is related to the atomic diffusion through oxide layer and the atomic chemical reaction at the Si–$SiO_2$ interface.

Researchers at the University of Pittsburgh propose that when electrons impact the Si surface in $O_2$ plasma, oxidation occurs by dissociative electron attachment for adsorbed $O_2$ species and the formation of O and $O^-$ species from adsorbed $O_2^-$ [27]. Another theory proposed that when a bias is applied, the oxidation mechanism is enhanced by ion bombardment; the oxygen ions are implanted into the silicon and chemical reactions occur that cause the growth of $SiO_x$ [28]. Additionally, the silicon is damaged during the implant process and, consequently, oxidation is increased.

The International Technology Roadmap for Semiconductors (ITRS) sets a stringent target of less than 0.2–0.4 Å, dependent on ½ pitch, per cleaning process step when the source/drain implant extensions are in place [29]. This problem is exacerbated by repetition since various ions are implanted with different dose levels using photoresist masks many times during the formation of the source/drain extension of different MOS transistors. With six to eight potential high dose implant and subsequent etching steps, only 1.6–3.2 Å of total Si loss is allowed for the entire front end of line (FEOL) manufacturing process. In many

**Table 8.1.** Best case film loss of Si and $SiO_2$ from various processing steps.

| Process type | Film loss |
|---|---|
| Best Plasma | 1.4 to 1.8 Å Si |
| SC-1 @ 80°C | ~1 Å/min Si |
| SPM | <1 Å Si, 0 Å $SiO_2$ |

cases, the damaged silicon is not always consumed or oxidized immediately after the implant cleaning step leaving the layer vulnerable to attack at subsequent processing steps. Table 8.1 shows the best-case Si and $SiO_2$ losses for various processes. Besides Si, SiGe used for PMOS (p-type MOS) logic transistors leads to additional process requirements due to the solubility of germanium in water [30]. Obviously, the current processes are challenged to meet these goals, and many research and development programs are ongoing to meet or exceed these specifications.

Research has shown that the damaged implanted silicon does not etch at the same rate as the undamaged unimplanted bulk silicon [31] in both wet chemical and plasma processing. It is well known that damaged layers etch faster than undamaged layers; however, extensive qualitative data is lacking for highly implanted silicon. Also, there are varying degrees of damage such as the formation of amorphous silicon and damaged crystalline silicon with dislocations loops, plus different combinations and degrees of each [32]. It is also known that the implant process causes extensive damage of the crystalline silicon that subsequently is compromised by the etching and cleaning processes. The $SiO_2$ layer can also be damaged by implantation [33] and this oxide does not etch at the same rate as undamaged $SiO_2$ [22]. Wirbeleit and coworkers have found that the implanted silicon oxidizes to a thickness 3–4 times that of unimplanted silicon during an $O_2$ plasma stripping process [34]. Formerly high temperature annealing could repair the damage for both silicon and silicon dioxide, but this solution is not an option for shallow junctions.

Measuring the silicon substrate loss can be performed using many different techniques [35, 36], with the most common being ellipsometry of Si on SOI (silicon on insulator). However, due to the varying degrees of damage and being further confounded by the implant, it is difficult to quantitatively express the depth of damage without physically observing the layers, such as by TEM (transmission electron microscopy) analysis – destructive – or by sensitive thin film thickness measurements such as ellispometry – non-destructive. Doping deactivitation discussed in the next section gives an assessment of the changes in electrical properties of the device with respect to the amount of silicon removed that contains the implanted species.

Another key issue is spacer loss that is especially critical for gate-first high-κ metal gate, as the spacer is also used as a thin diffusion barrier, and loss not only can change the critical dimension (CD) but expose the sensitive metal gate or high-κ dielectric to the cleaning chemistries.

In general, film loss is one of the most challenging problems to solve with respect to high dose implant stripping. Many research and development projects are underway to better understand the causes and mitigation of enhanced oxidation and to develop new processes to reduce the oxidation.

### 8.1.5 Dopant Deactivation

Dopant deactivation is used in a broad sence, it means any affect to the electrical characteristics of the IC device junctions caused by the stripping and cleaning process. As the junctions become shallower, this phenomenon becomes increasingly important to prevent. Wirbeleit and coworkers have defined three different ways plasma processing can impact the junction [34]:

1. Oxidation or etching of the surface causing junction loss.
2. Leaching of the near-surface dopants.
3. Changing the chemical bonding of the junction surface possibly leading to vacancy enhanced diffusion.

As discussed in Section 8.1.1, the low-energy high dose implants have most of the dopant very close to the surface, thus, making it possible for the stripping process to affect the top electrically active layer that is critical for the device to retain.

Dopant deactivation also can be caused by damage to the silicon including amorphization [37] which is caused by the implant process and also by the stripping process. This amorphization increases the susceptibility to the chemistries used for processing. Additionally, erosion of the silicon substrate containing the dopant will cause an increase in sheet resistivity ($R_s$). the higher the $R_s$, the more loss of dopant, as compared to the initial $R_s$ value [3, 34]. The deactivation becomes apparent after the anneal step. Therefore, the implant, stripping, cleaning, and anneal parameters all must be integrated to create a process that meets the required electrical parameters of the IC device.

The loss of the dopant in USJ can be caused by wet cleaning processes using SC-1, reported by Buh *et al.*; n-type Si etches at a faster rate than p-type [38]. They found the dopant loss caused by SC-1 a significant factor in process optimization for n-type field effect transistor with USJ. Another study [39] showed that the arsenic doping deactivation by wet cleaning of the post-implanted n-channel source/drain was a major challenge in scaling devices while the p-channel was driven more by the shallow junction limitations. It is speculated that the dopants that are leached into the SC-1 solution form soluble oxides, however, As ($HAsO_3^-$) is more soluble that B (as $H_3BO_2$).

The plasma stripping process can also deactivate the doping. Berry and coworkers have observed a significant decrease in $R_s$ for fluorine-containing stripping chemistries; possibly due to the high concentration of the dopant at the surface in addition to the amorphized silicon that etches more rapidly than the undamaged silicon [40], as shown in Figure 8.13. Pure $O_2$ stripping chemistries have better retention of the resistivity. This is speculated to be due to the denser oxide that is formed on the surface than with other plasmas. Boron and arsenic implants behave differently. Arsenic, used for n-channel devices, diffusion into the silicon was enhanced with $H_2/N_2$ plasma while $O_2/H_2/N_2$ plasma showed an increased

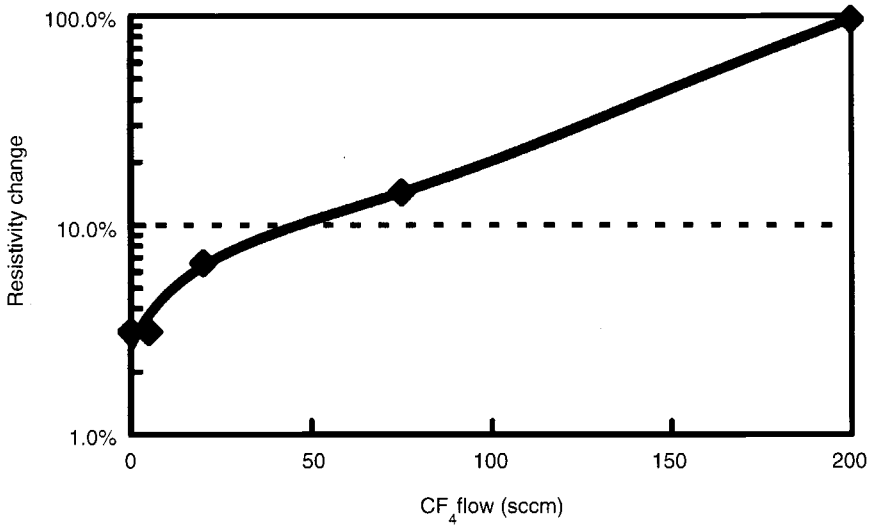


**Figure 8.13.** The change in sheet resistance caused by $CF_4$-containing plasma stripping process, as compared to a $CF_4$-free stripping process [40]. The plasma process conditions are 7000 sccm total flow with 10% $H_2/N_2$ in $O_2$. The implant conditions are 2.0 keV As at $5 \times 10^{14}$ atoms/cm$^2$ dose, then annealed 10 sec at 1000°C. Used with permission of Berry, I. L., Waldfried, C., Han, K., Luo, S., Sonnemans, R., and Ameen, M., *8th International Workshop Junction Technology (IWJT)*. © 2008 IEEE.

concentration at the surface. For boron, used for p-channel devices, a dependence on the implant energy was observed. At higher implant energies chemistry has little affect on the doping profile while at low implant energies, $R_s$ is increased, likely due to the consumption of the boron during the plasma stripping process. Berry has also shown that the implant dose is an important factor. As the damage to the silicon increases with increasing implant dose, $R_s$ increases, a threshold is observed at $>1 \times 10^{15}$ atoms/cm$^2$ whereas $R_s$ increases.

## 8.2 High Dose Implant Cleaning and Stripping Processes

High dose implanted photoresist is stripped by using a sequential process consisting of plasma followed by wet cleaning. This traditional method has significant challenges: popping of the photoresist, incomplete removal of residue, high amount of silicon loss including dopant deactivation; all result in manufacturing and yield issues. Other methods of stripping the photoresist have been developed: all-wet processing, cryoaerosol, and laser cleaning are some examples. Extension of the plasma and wet cleaning process using modified plasma processing is an area of active work. New stripping chemicals that can remove the resist and that do not affect the exposed films are being developed. New wet cleaning process reactors and techniques are all being investigated. This section will discuss the various methods of HDIS.

### 8.2.1 Process Requirements

Obtaining an optimum process is critical for IC devices. The metrics for measuring successful devices are electrical functionality within process parameters,

high device yield, and long term reliability. An optimum high HDIS process must result in:

1. Minimal loss of the critical top surface dopant.
2. Minimal Si substrate loss and/or oxide loss.
3. Minimal oxidation of the Si substrate.
4. No etching of material composing the gates or augmentation of the material composition.

Other technical metrics that are important are:

5. Low particle adders during processing.
6. Minimal metallic contamination.
7. No substrate pitting or roughening.
8. No remaining photoresist or other organic contamination, including crust.

Of course, cost is always a factor; a low cost of ownership (CoO) is desirable, but not at the expense of technical requirements.

### 8.2.2 Process Comparison: Wet and Dry

Each type of stripping processing has advantages and disadvantages in meeting HDIS success criteria. Plasma processes consume Si and $SiO_2$; however, these processes have a low CoO and promising development projects are underway that dramatically reduce silicon consumption. Wet processes are attractive because of minimal loss of Si or $SiO_2$. Standard clean-1 is the largest contributor to Si loss; however, dilute chemistries minimize the effect. Sulfuric acid hydrogen peroxide mixture does not contribute to $SiO_2$ film loss but will oxidize Si while HF or neutral oxide etch (NOE) dip will intentionally consume $SiO_2$. Integration strategies for advanced logic devices are using raised source/drain trench structures to alleviate the stringent Si loss specifications; however, undercut of the gate dielectric is still critical.

The integrated stripping and cleaning process typically consist of the following process key steps: crust breakthrough and removal, bulk resist removal, residue removal, and particle removal. The plasma process removes the crust and the bulk resist and the wet process removes the residue and particles. Figure 8.14 shows an outline of a process flow noting each process step. The plasma process is typically performed in a downstream reactor and the wet process is typically performed in

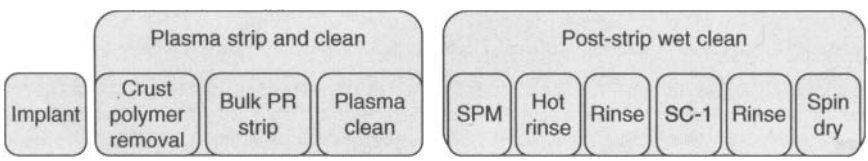


**Figure 8.14.** Outline of a high dose implant strip process showing the plasma and wet stripping cleaning flow. Used with permission of the authors.

a wet bench or batch spin spray platform although there are many projects focusing on single wafer spin spray photoresist removal. The plasma process is outlined in Section 8.3 and the wet process is outlined in Section 8.4.

## 8.3 Plasma Processing

The plasma process and equipment has evolved from a simple $O_2$-based batch downstream reaction chamber to a sophisticated, microprocessor-controlled multichamber platform capable of removing the crust and stripping the photoresist. However, there are still many challenges facing plasma processes, including:

1. No popping of photoresist.
2. Complete removal of all photoresist and organic residues.
3. Minimal loss of Si and $SiO_2$ and minimal doping deactivation.
4. No additional defectivity.
5. No charge damage to active devices.

Plasma processing is used for removing photoresist primarily because of its ability to rapidly strip photoresist at low cost while achieving the process requirements outlined here.

Either oxygen- or hydrogen-based gases are used to strip the photoresist. Plasma systems are capable of stripping bulk photoresist at very fast rates – approximately 15 μm/min is typical. Additives such as fluorine-containing gases are added to increase the stripping rate. The crust stripping rate is lower – approximately 0.5 to 1 μm/min. High dose implant stripping tools typically employ microwave downstream plasma (MWD) reactors with radiofrequency (RF) biased or inductively coupled reactors with or without bias.

### 8.3.1 Photoresist Popping

The crust layer does not behave like bulk resist during the stripping process. Fujimura recognized that the resist would wrinkle and crack if downstream $O_2$ plasma was used to attempt to strip the implanted resist [10]. Many techniques have been developed to address the issue of removing the crust without "popping" and without leaving crust residue. One such method is removing the crust at a lower temperature to prevent the underlying bulk resist from "popping" that occurs when the bulk photoresist is heated and the solvents vaporize with the crust preventing the solvents from escaping, as shown in Figure 8.15. The "popped" photoresist crust can redeposit on the wafer surface. This residue is extremely difficult to remove with a simple $O_2$-based resist strip process and due to the nature of the contamination that was discussed in Section 8.1.3.

Pre-treatment of the photoresist is also helpful. Deep ultraviolet (UV) treatments, baking and light exposure, also can help diminish the popping by stabilizing the resist by driving off solvents and also by cross-linking the photoresist preventing the surface effects caused by the implant.

Another method to prevent popping is to remove the photoresist in a rapid manner, for example, using reactive ion etching (RIE) to remove the crust layer.

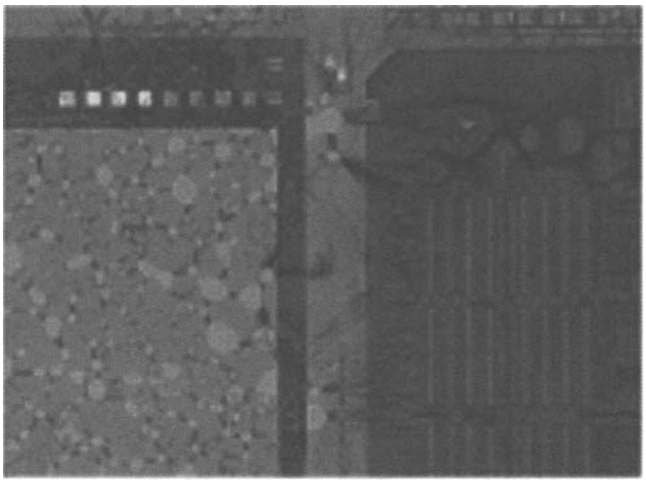

**Figure 8.15.** Micrograph of the high dose implanted photoresist showing popping. This occurs when the bulk photoresist is heated during the plasma strip step without first removing the crust layer [41]. Used with permission from Axcelis Technologies.

Due to the resistance of the carbonized crust layer to downstream plasma, ion bombardment to physically assist the chemical stripping process contributes to the faster etching rate crust removal. However, this is at the expense of the underlying film – removal of the $SiO_2$ or Si is accelerated and undesirable charging can occur. Fujimura first attempted removing the crust with an RIE etch, then stripping the unchanged photoresist with downstream plasma [10]. The temperature of the RIE process must remain low to prevent popping of the photoresist. Typically, the temperature of the crust removal process must remain lower than the final photolithography post-develop bake temperature. However, not all the crust needs to be removed to prevent popping.

Many engineers and researchers have published papers showing that RIE alone or RIE combined with downstream plasma is able to remove the crust layer without popping. Coupling the plasma with temperature has resulted in production-worthy stripping processes. McComber and Nair in 1991 developed a residue-free stripping process based on a combination of deep UV (DUV) pre-treatment and temperature control with low temperature being used for the crust removal step followed by a higher temperature process for the remaining photoresist [42]. With the use of higher doses of dopants and higher implant currents, stabilization of the photoresist prior to implantation is critical; Marshall and coworkers in 1998 established an integrated process for implantation, stabilization, and the subsequent stripping [43].

A controlled increased ramp of temperature during the crust removal step has been used to prevent popping of the photoresist. During the ramp, the crust is slowly being etched away, at a low enough temperature to prevent popping [19]. However, the ramp from low to high temperature, typically less than the soft bake temperature of the PR to approximately 200°C or greater, is prolonged because of the slow etching rate of the crust, sometimes as low as a few hundred Anstroms per minute. In some cases where the processing tool is incapable of modulating the temperature, the entire process is performed at low temperature.

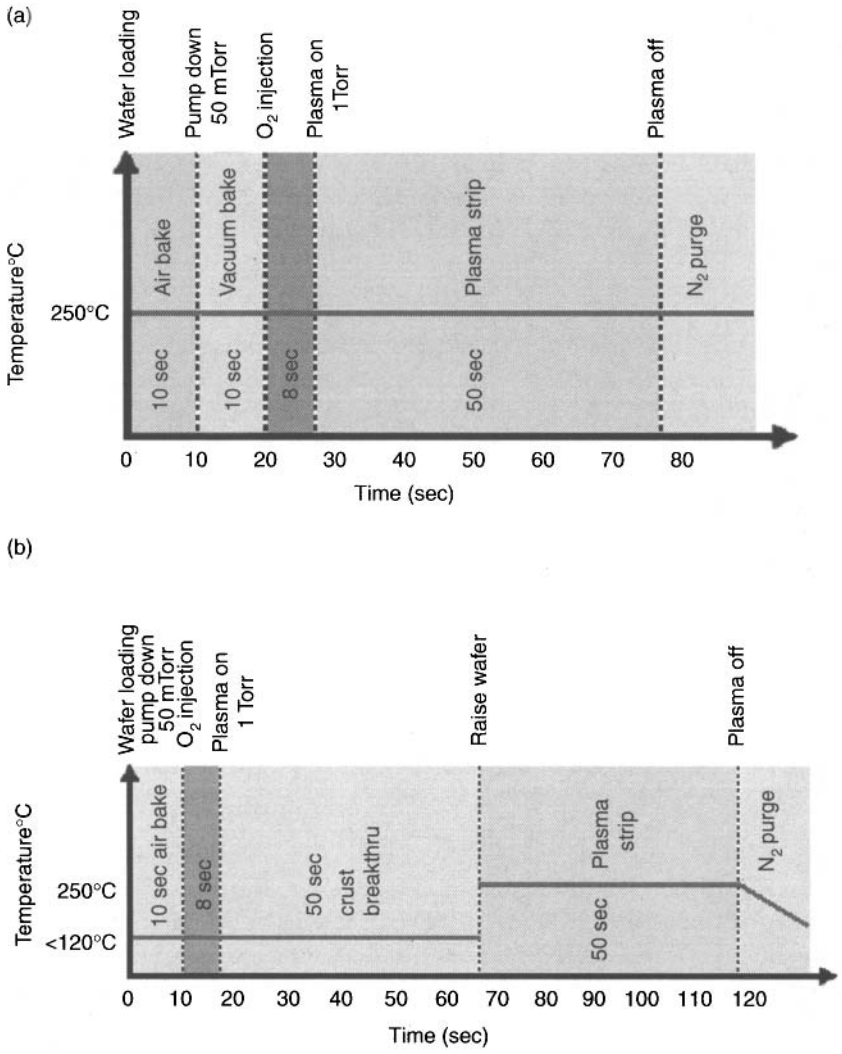


**Figure 8.16.** Examples of (a) typical temperature ramp and (b) controlled in-situ bake temperature profile for plasma processing used to prevent popping of the photoresist. Adapted by the authors from [41] and [44].

Another method for preventing popping by temperature modulation is proposed by Park *et al.* in which the resist is purposely heated and the temperature ramped in a controlled manner under vacuum [44]. A typical temperature ramp is shown in Figure 8.16a and the controlled ramp is shown in Figure 8.16b.

Besides temperature modifications and pre-treatment of the photoresist, processes using additives such as fluorine-containing gases assisted in increasing the etch rate not only of the photoresist, but also of the crust. Multi-step process recipes were developed to remove:

1. Crust.
2. Bulk photoresist.
3. Post-strip residues.

Typical plasma stripping and cleaning processes for bulk photoresist stripping and high dose implant strip processes are outlined in [45]. Typically, these processes initiate at a low temperature, then gradually ramp with the bulk photoresist removal at a high temperature and the residues being removed with a F-containing gas [46]. However, care must be taken to prevent excessive etching of the $SiO_2$ film.

Hydrogen addition using forming gas was reported by Fujimura *et al.* as being a gas that could effectively etch the crust and photoresist with minimal oxidation of the silicon [47]. Section 8.3.3 discusses the process chemistry used for high dose implant stripping.

## 8.3.2 Plasma-induced Damage

The use of plasma for stripping can potentially cause both physical and electrical damage to the wafer surface. This section will discuss the damage induced from charging and the physical damage to the substrate caused by the high dose implant resist strip process.

### *8.3.2.1 Charging Damage*

Charging damage can arise from transference of the charged species in the plasma to the substrate. It is known that plasmas used to deposit, etch, or strip films can detrimentally impart charge on the wafer surface [48]. Particularly sensitive is the gate dielectric. Even when only partially exposed during the stripping process, the gate dielectric can suffer premature breakdown and substrate leakage. The gate dielectric is exposed during the HDIS process – under the gate conductor and sometimes is still covering the source and drain areas. Additionally, the bombardment of the energetic ions during plasma processing can cause damage to the near surface. Photons also have the ability to excite electrons providing a means to break bonds, causing holes to form, and further causing reliability issues. References available that thoroughly discuss the causes of charge damage, also referred to as radiation damage, are given in [49, 50] and [51].

Features size, antenna ratio, dielectric thickness, interconnect structure, and other circuit design factors affect the ability of the charge to damage the gate oxide [52]. Analysis of charge damage can be performed by various methods: thin oxide capacitors arranged to collect the charge [53] by forming antenna structures [52] to check the gate oxide integrity (GOI), as well as CHARM® monitors using EEPROM (electrically erasable programmable read-only memory) stacked gate technology to collect the charge and then measuring the surface potential [54], and simple IV curves [55]. Gabriel presents an overview of various testing options for determining the amount of charge damage [56].

Modeling of reactor design and the plasma parameters affecting charge damage has been performed [57] and different types of plasma generators; RF or MWD, for example, have been assessed with respect to the damage they impart [19, 58]. High-density, low-energy plasma sources, such as downstream modules, are shown to impart less charge damage than high-energy biased plasma [59]. Development of low-damage stripping modules have been achieved. Savas and coworkers have demonstrated that inductively coupled plasma (ICP) achieves

high stripping rates with low ion density by generating a high amount of reactive neutral species [60].

Although most bulk photoresist stripping processes use a purely downstream reactor, typically MW or ICP, high dose stripping needs additional ion bombardment available with biased plasma to remove the hardened crust. Most notorious for causing charge damage is the combination of biased and downstream plasma sources. Chan [61] and coworkers at TSMC have evaluated the substrate damage caused by an ICP system with independent control of the bias and the top plasma. Although not a true downstream plasma, the study is a good representation of a dual-source processor. They have shown by carefully controlling the plasma parameters, including power, a damage-free process can be obtained. Additioninally they have shown that the damage to both p- and n-channel devices correlates well with the electrical data.

Plasma conditions and chemistry also play a role in charge damage. Researchers have shown that the combination of bias and fluorine from $NF_3$-containing stripping chemistries contribute more charge on the wafer's surface than downstream MW with RF bias $O_2/H_2/N_2$ plasma. The free fluorine generated by the addition of the bias to the downstream plasma leads to high plasma voltages that are speculated to cause the damage [62].

#### *8.3.2.2 Physical Damage*

With the use of bias to strip the high dose implanted photoresist, physical damage to the wafer can be imparted due to bombardment of the ionic species of the stripping plasma. Although the damage is less severe than with etching plasmas, sputtering and substrate damage are common. Other damaging effects have been documented and there is always a concern new defects due to the stripping process will occur.

Substrate damage with dual mode downstream and bias has been shown to be minimal by Kawaguchi and team [7, 63] They have shown by observing removal of the implanted species minimal amounts of silicon are removed with the dual mode plasma and essentially none are removed with downstream plasma only. The damage caused by the implant is observed to be about 50 Å deep. Additionally, oxidation of the surface does occur also observed by Fujimura [10].

Silicon and poly-Si pitting defects induced by ion implanted PR popping during dry strip process were observed by Chin and coworkers [64]. The chemistry used for stripping included a fluorine-containing additive that caused etching, and, subsequently, pitting of the substrate and gate line where the photoresist had popped exposing these areas to the plasma longer than the areas were popping did not occur.

### 8.3.3 Stripping Process Chemistry

Oxygen-based stripping is the typical method for removing photoresist. Although other gases have been used for specialized applications, $O_2$ processes are ubiquitously found within the industry on all types of plasma stripping equipment. The addition of forming gas is becoming more ubiquitous either as an additive to $O_2$,

alone, or with $O_2$ being an additive. Forming gas for photoresist stripping is used to increase the stripping rate of photoresist since hydrogen increases the density of activated $O_2 \rightarrow O\bullet$ (free radical) and reduces the activation energy for removal due the formation of OH radicals [65]. Besides reducing the implanted species to volatile gases, forming gas is also used as an alternate gas to $O_2$ to achieve a slow etching rate for the crust removal step. Water vapor has shown some success for breaking through the implanted crust and accelerating the slow strip rate by using RF bias only. Helium is also added possibly due to the high RF bias power and low pressure. Fluorine-containing gases were first used for removing post-stripping residues. Although they have a high oxide etching rate, they are helpful with the removal of crust and hard to remove residues when no other process is capable.

In most instances the carbonized crust layer is removed by the use of low-power RF reactive ion etching (RIE), either alone or in combination with MW power. Early use of hydrogen plasma for stripping and combination of microwave and remote plasma was demonstrated by Fujimura *et al.* [47] and Kikuchi and Bersin [66]. Commercialization and high volume production using both forming gas and dual plasma sources was realized by work at GaSonics in 1998 [19]. Reducing $H_2$-based chemistry for the bulk photoresist stripping step shows promise for minimizing Si loss and $SiO_2$ formation. However, the stripping rates have suffered due to the low concentrations of $H_2$, typically 4% $H_2$ in $N_2$, which are used. Addition of forming gas to $O_2$-based plasma has shown successful results.

The use of fluorine-containing gases has shown ambiguous results. Some researchers show that fluorine-containing gases are detrimental to retention of oxide while others show that fluorine enhances the cleanliness with a minimal loss of oxide. Rounds and coworkers at Axcelis have shown success by using $CF_4$ [41] in combination with $O_2$ and forming gas and temperature control. The lower temperature controls the photoresist popping and also reduces the oxide loss. However, the forming gas is needed to mitigate the oxide loss. Figure 8.17 shows

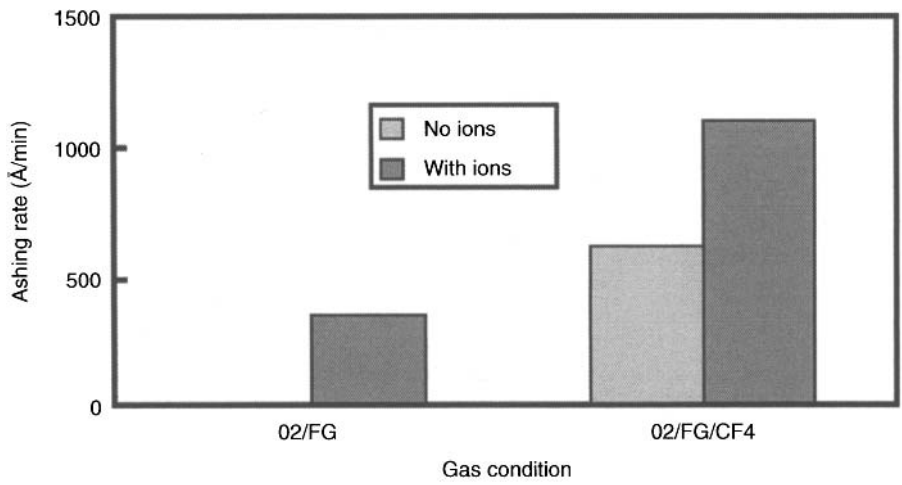


**Figure 8.17.** Crust removal gas compositions with and without bias power [41]. The temperature is 120 ± 30°C. FG = forming gas. Used with permission of Axcelis Technologies.

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# Aluminum Interconnect Cleaning and Drying

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*Abstract*

The cleaning challenges associated with the integration of Al are examined for post-tungsten plug, post-conductor line etching, and post-via etching. The different residues formed during these processing steps are described and the approaches to clean and remove these residues by wet processing are presented. The chemical formulations used to remove the residues are discussed; fluoride-containing and hydroxylamine mixtures are the main focus. The applications and the process parameters for successful cleaning are presented.

*Keywords:* aluminum cleaning, interconnect cleaning, via cleaning, metal line cleaning, tungsten plug cleaning, fluoride formulation, hydroxylamine, post-etch aluminum residue, post-etch residue removal

## 9.1 Introduction to Aluminum Interconnect Cleaning

Since the middle 1970's, aluminum (Al) has been the predominant material for metallization used in integrated circuit (IC) manufacturing. Starting in the mid-1990's, copper (Cu) has supplanted Al as the interconnect metal of choice for advanced logic devices, largely as a result of its higher electrical conductivity, better resistance to electromigration, higher reliability, and lower overall manufacturing cost [1, 2].

This transition, however, would not have been possible without the concurrent development of advanced planarization methods and damascene-style process integration, because Cu cannot easily be etched by plasma processing. While Cu has assumed the leading-edge position with respect to advanced technology development, Al has a large installed base. This has come about due to the technical requirements for logic applications that have complex circuitry requiring complicated interconnect levels. Compared to logic devices, the switch from Al to Cu metallization is not as pressing for DRAM (dynamic random access memory), Flash memory, specialized ASIC (application-specific integrated circuits), or for analog or low-end consumer electronics. However, Cu is expected to surpass Al on a surface-area basis due to adoption of Cu by memory manufacturers by 2013–2015 [3].

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The early adoption and extendibility of Al are a result of its desirable physical and chemical properties. It has excellent electrical conductivity – only three metals have higher conductivities, as shown in Table 9.1. Aluminum also exhibits several other properties that make it a successful interconnect material:

1. It is amenable to etching by both wet and dry methods.
2. It is relatively inexpensive in high purity.
3. It quickly forms a passivation layer in air that is very thin (~5 nm) as well as physically and chemically robust [4] that mitigates corrosion concerns during manufacture.

In this chapter the cleaning challenges associated with the integration of Al will be examined. After a discussion of the etching technologies employed in patterning Al features, the different residues formed during distinct processing steps required for Al integration will be described. General approaches to residue removal will be presented with a specific focus on wet cleaning. A variety of dry (plasma-based) approaches to residue removal have been described – based on oxygen, hydrogen [6], ammonia [7], carbon dioxide (discussed in Section 9.5), fluorocarbons [8], and alcohols [9]; but none have proven more than a complementary approach to wet cleaning, which is required for high-volume manufacturing during aluminum interconnect formation.

The remainder of this chapter surveys the applications and chemistries involved with Al cleaning. The methodologies employed in developing formulations to effect these cleaning processes have been, for the most part, excluded because they are the subject of Chapter 5.

**Table 9.1.** Electrical resistivity of ten most conductive metals [5].

| Material | Resistivity @ 298°K (mΩ-cm) |
|---|---|
| Silver | 1.617 |
| Copper | 1.712 |
| Gold | 2.255 |
| Aluminum | 2.709 |
| Calcium | 3.42 |
| Beryllium | 3.7 |
| Magnesium | 4.48 |
| Sodium | 4.88 |
| Tungsten | 5.39 |
| Molybdenum | 5.47 |

## 9.2 Source of Post-Etch Residues Requiring Wet Cleaning

Wet etching does not create post-etch residues. The transition in the late 1970's from wet to dry (plasma or reactive ion) etching of Al metal was driven in large measure by the anisotropic capability of dry methods. Directional etching control allows higher pattern densities and eliminates other issues associated with wet etching including re-deposition of partially etched materials (due to the inability of wet etching chemistries to completely remove Si and Cu added to the Al and process reproducibility [10]. The degree of anisotropy increased as batch-style etchers yielded to single-wafer etching chambers and as a result of this evolution post-plasma etch residues started to appear on the sidewalls of patterned features. These residues (referred to as post-etch residues, PER) aided in achieving vertical feature profiles, thereby allowing for higher pattern density [11]; however, their removal by solvent cleaning required long process times and high temperatures to be effective, as will be shown in Section 9.3. Eventually the use of non-reactive cleaning solutions became unworkable and PER cleaning began to adopt approaches that are still used today.

With subtractive-etching Al integration schemes, there are basically three different cleaning process steps required, and each will be separately discussed, though some are grouped together because they are closely related from a residues standpoint. They are:

1. Post-tungsten (W) plug etchback.
2. Post Al-line etching and Al pad cleaning.
3. Post-via etching and post-pad etching.

For each of the above examples, a basic understanding of the etching process is required since the nature of the residues formed is determined by a combination of the etching process used and the chemicals and materials that are present during etching.

Post-etch residues in Al interconnect have garnered a series of other names over the last 20 years. They have frequently been referred to as polymers or sidewall polymers – probably as a result of their relative lack of solubility in common solvents historically used for wet photoresist removal. After Al plasma etching and $O_2$ stripping they have been called post-ash residues or post-strip residues. Interestingly, it is after plasma stripping that the residues most resemble polymers; they are composed of extended molecular chains more related to metal oxides than molecular organic contamination [12]. For post-via etching many residues have metals embedded in a carbon-based backbone [13]. However, after plasma stripping it is unlikely that much organic material remains [13]; therefore terms such as "polymer" are misrepresentative.

It is common to see residues that stand up alongside and above the top surface of the metal lines, and these have been referred to as "fences", "posts", and, amusingly, "bat ears" when they stand high enough. Residues formed during via etch that appear to arise out of the vias resemble and have been labeled "crowns."

### 9.2.1 Post-tungsten Plug Etchback Cleaning

Tungsten is the metal most commonly used to fill vias that connect stacked metal wiring levels, especially below ~0.8 μm. The issue of via cleaning will be discussed in a subsequent section; however, the needs for post-tungsten etchback cleaning will be discussed here. The process flow for forming tungsten plugs has been well described in the literature [14].

After deposition (typically using chemical vapor deposition (CVD) techniques but sometimes using PVD), of the W into the plugs to form contact with the semiconductor transistor, or to form via contacts between metal levels, the overburden W must be removed. There are two common removal methods. The first, and more common today, is the use of tungsten chemical mechanical polishing (CMP) [15]. The second, referred to as tungsten etchback, as shown in Figure 9.1, involves removing the W using a plasma process with fluorine-containing gas, for example, $SF_6$ [16, 17], according to the following consolidated reaction [18]:

$$W + SF_6 + \text{excess } O_2 \rightarrow WF_6(g) + SO_x(g) + WOF_4(g) \qquad (9.1)$$

The requirement for cleaning after etchback is driven by the following:

1. The oxide surface on which the TiN and then W are deposited will naturally have some topography and around certain features the removal of the metals from the etchback process is not 100% efficient, leaving behind what are normally referred to as "stringers".
2. Imperfections in the etching process will leave behind (mostly Ti-based) $TiF_x$ residues [19]. Both the stringers and the Ti-based residues are potentially conductive and must be completely cleaned to eliminate the possibility of electrical shorting in the finished device. In most cases, there are no tungsten-based residues because most

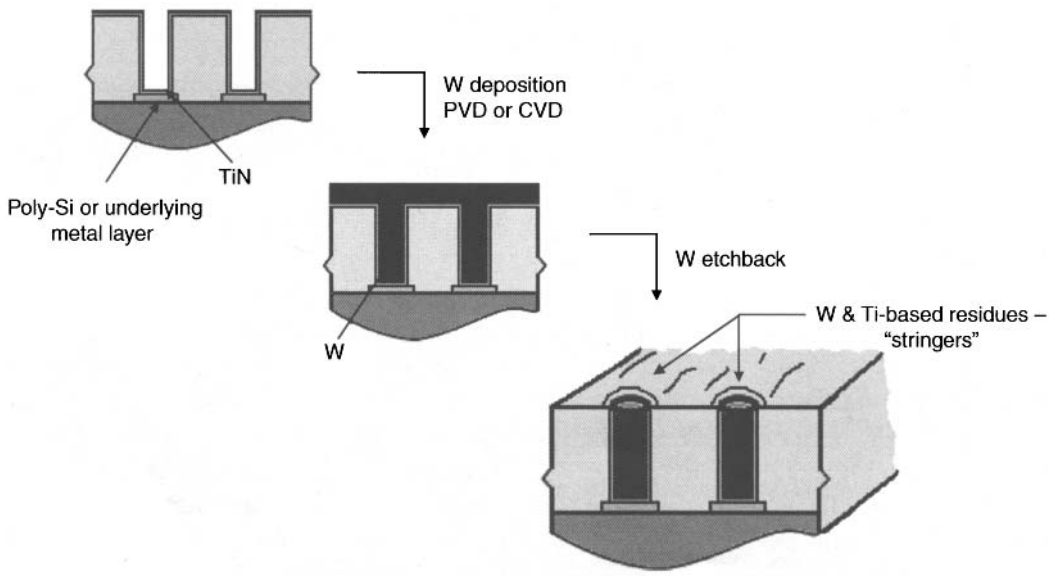



**Figure 9.1.** Schematic of the W etch-back process. Used with permission from author.

potentially resultant W compounds are volatile. However, W can be incorporated into the Ti residues.

3. Excessive plasma etching, in order to remove the stringers, will result in recessed tungsten in the areas in which it is required. Keyholes and seams at the center of the W filled contact can then be opened and collect unwanted residue so plasma cleaning needs to be minimized.

Thus, the residues that are formed during the W etchback process can be thought of as $(Ti,W)_xF_y$. Fortunately, because no photoresist mask is present and typically carbon-containing plasma is not used, there is no carbon-based residue. However, it has been reported that using $SF_6$ gas leaves sulfur residues [20]. Their removal requires a wet chemical treatment that can dissolve these types of materials. Aqueous hydrofluoric acid cleaning has been used [21], as have ammonium hydroxide hydrogen peroxide (APM) solutions, which can etch the metal surface [20].

## 9.2.2 Post-aluminum Line Etch Cleaning

Typically, aluminum has small amounts of silicon added (0.5–3 wt%) for the prevention of junction spiking and/or copper added (0.5–4 wt%) to minimize electromigration. Barrier metals below the aluminum are common, typically titanium and/or titanium nitride (TiN) in a stack [22]. These prevent the aluminum from reacting with the silicon, and also, if electromigration is severe, allow a conductive path. The Ti serves as an adhesion layer between the Al lines and the dielectric and W contacts, which is necessary due to the poor adhesion of TiN to $SiO_x$. Antireflective coatings (ARC's), typically TiN, are also used on top of the aluminum. All the metal layers employed in aluminum metallization can be deposited by physical vapor deposition (PVD).

Residues created following Al line patterning are different in composition than those described in the prior section. After lithography and resist development, the exposed metal stack is etched by a plasma primarily consisting of chlorine-containing molecules, according to the following reactions [23]:

$$2\,Al + 3\,Cl_2 \rightarrow 2\,AlCl_3(g) \tag{9.2}$$

$$2\,AlCl_3 \rightarrow Al_2Cl_6 \tag{9.3}$$

Following the etching process, the remaining photoresist is removed, either by a hot solvent treatment or, more commonly, by an oxygen plasma treatment. This oxygen plasma treatment can have a dramatic effect on the post-etch residues that are left behind as they ensure oxidation of the residue matrix and any embedded metallic residue. As illustrated in Figure 9.2, the etching process leaves behind residues that must be removed: they are physically fragile and are at risk of dislodging during a subsequent oxide deposition step, creating particulate contamination. They may also be conductive and thus risk creating interlevel metal shorts.

Figure 9.3 shows SEM (scanning electron microscope) images of etched and plasma stripped metal lines, a) before and b) after residue removal. The images reveal that most of the residue is found at the top edge of the pattern and at the foot of the metal lines. This observation is common and is important in understanding

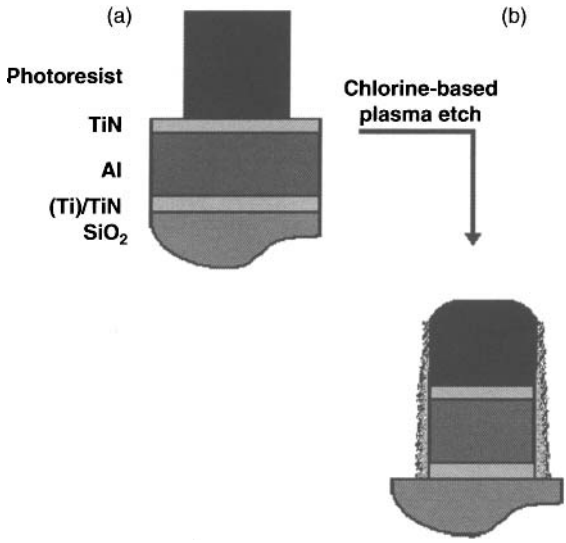



**Figure 9.2.** Schematic Al metal line a) before etching and b) after etching showing residue creation. Used with permission of the author.

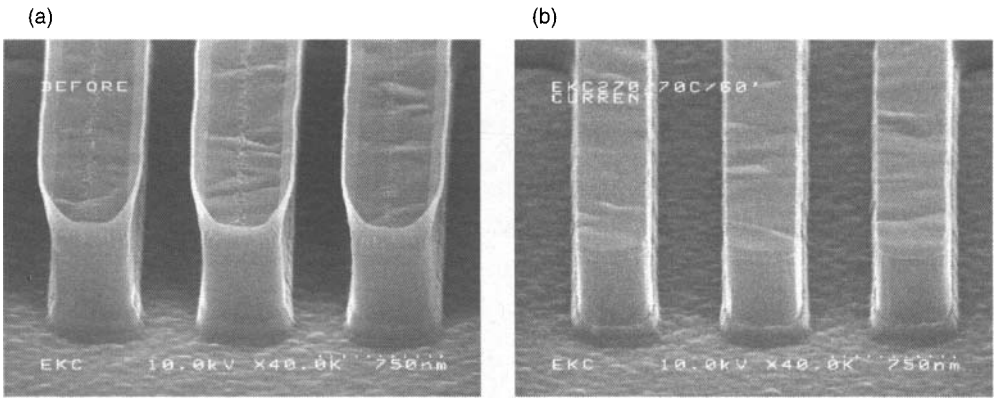



**Figure 9.3.** Scanning electron microscope images of Al metal lines a) after etching and stripping with residue present and b) after cleaning showing residue removal. Courtesy of DuPont/EKC Technology (2010).

the chemical nature of the residues that are formed. There is a significant difference observed between the types of residues formed after metal etching versus after via etching, as evidenced by the different processes and the relative ease of the two types of cleaning.

Post-metal etch residues are relatively easy to clean using a wide variety of cleaning compositions – those based on hydroxylamine or on fluoride either with or without carboxylic acids. This is suggestive of residue composition containing small amounts of chloride and possibly fluoride depending on whether a fluorocarbon passivation step is included after the Cl-based metal etching step [24]. Also included in the residue are small amounts of aluminum, copper, and silicon, depending on the degree of over-etch into the pre-metal dielectric, to ensure complete removal of the metal features. Depending on the specific etching process

and structure, there is wide variation in the specific residue composition. These residues have been analyzed by Auger electron spectroscopy (AES) [12], thermal desorption spectroscopy (TDS) [25] and electron-dispersive spectroscopy (EDS) [26, 27]. Figure 9.4 shows AES depth spectra of the residues after aluminum line etching and cleaning [12]. After etching a Cl signal is detected from the process gases at a depth of ~400Å, possibly indicating the Cl is encapsulated by the sputtered silicon oxide (the synonymous Si and O signals).

The etching process is tailored for removal of Al forming volatile $AlCl_3$; however, the top TiN is refractory and challenging to etch because titanium halides are generally less volatile than $AlCl_3$ and can remain as residue on the sidewall of the line even during ion bombardment. Therefore, the top metal is sometimes etched with a fluorine-containing chemistry [28]. This adds additional complexity to the

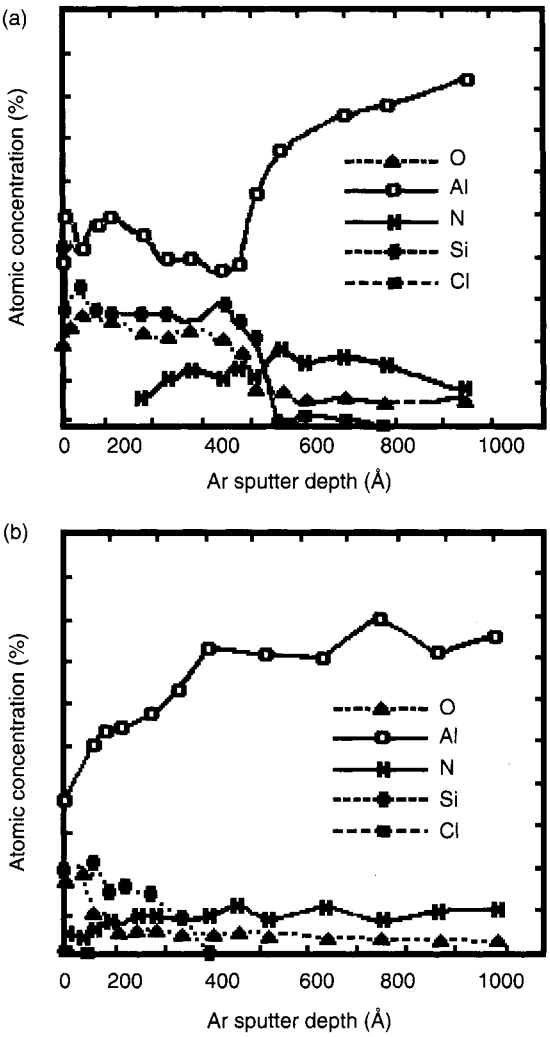



**Figure 9.4.** Auger electron spectroscopy spectra of aluminum sidewalls a) after aluminum line etching and with residue present and b) after sidewall residue removal with $BCl_3$ plasma [12]. Reproduced with permission of ECS – The Electrochemical Society from Kawamoto, H., Miyayoto, H., and Ikawa, E., *Proceedings of the Tenth Symposium on Plasma Processing.*

**Table 9.2.** Melting points of selected metal halides [30].

| Name | Formula | mp/°C |
|---|---|---|
| Aluminum chloride | $AlCl_3$ | 192.6 |
| Titanium(II) chloride | $TiCl_2$ | 1035 |
| Titanium(III) chloride | $TiCl_3$ | 425 (decomposes) |
| Titanium(IV) chloride | $TiCl_4$ | −24.12 |
| Aluminum fluoride | $AlF_3$ | 2250* (@220 MPa) |
| Titanium(III) fluoride | $TiF_3$ | 950 (decomposes) |
| Titanium(IV) fluoride | $TiF_4$ | 377 |

* For $AlF_3$ the temperature indicated is the triple point

residues [29], as typically $CF_x$ species are detected when $CF_4$ is used for etching TiN. Table 9.2 shows the volatility of selected metal halides that potentially may be formed during Al interconnect delineation.

The etching process must entirely clear the metal being removed; however, the plasma process over-etches into the silicon oxide at the bottom of the metal lines, as shown in the micrograph of Figure 9.3. This results in sputtering of silicon oxide onto the sidewall and top of the metal lines, adding to the complexity of the residue, especially at the bottom. Thus, the residues that are formed during Al metal-line etching are predominantly made of titanium oxide-fluoride species at the top and bottom of the metal features [28] as well as back-sputtered $SiO_X$ at the bottom of the features plus $AlO_x$ [12] and AlCl containing residue [25].

Aluminum has unique properties. It is amphoteric (reacting with both acids and bases) and forms a self-passivating oxide layer, $Al_2O_3$, upon exposure to oxygen that is insoluble in water:

$$4\,Al + 3\,O_2 \rightarrow 2\,Al_2O_3 \tag{9.4}$$

Alternatively, $Al(OH)_3$, a hydrated form of $Al_2O_3$, is only slightly soluble in water (0.0001 g/100 mL at 20°C), and is formed upon exposure of Al metal to water:

$$2\,Al + 6\,H_2O \rightarrow 2\,Al(OH)_3 + 3\,H_2 \tag{9.5}$$

In alkaline solutions, aluminum forms $Al(OH)_4^-$, which is thought best represented by $H_2AlO_3^-$ [31], through an intermediary of $Al(OH)_3$ [32]:

$$Al + 3\,OH^-(aq) \rightarrow Al(OH)_3 + 3\,e^- \tag{9.6}$$

$$Al + 4\,OH^-(aq) \rightarrow Al(OH)_4^-(aq) \rightarrow H_2AlO_3^-(aq) + H_2O \tag{9.7}$$

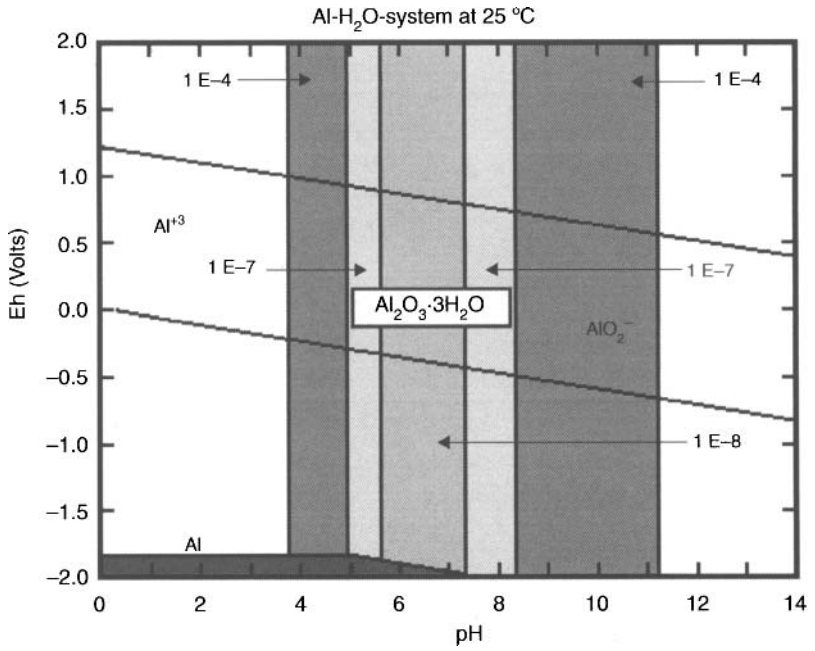



**Figure 9.5.** Pourbaix diagram of aluminum-water system. The solid lines represent the regime of stable water; the solid lines represent the solubilities of the species. Courtesy of Robert Small, RS Associates.

In acidic solutions, $AlO_2^-$ forms in an overall reaction given as [31]:

$$Al(OH)_3 + 3\,H^+(aq) \rightarrow Al^{+3}(aq) + 3\,H_2O \rightarrow AlO_2^-(aq) + 4\,H^+(aq) + H_2O \quad (9.8)$$

A Pourbaix diagram of aluminum in water (Figure 9.5) indicates an estimated minimum solubility of Al at pH 7.7 [31]. Even at their highest solubilities, Al complexes are not very soluble in either aqueous acid or base, and since Al passivates quickly under these conditions, its etch rates are typically low. The Al species formed in aqueous solution are independent of electropotential, so even with an oxidizing chemical, such as $H_2O_2$, for example in dilute sulfuric acid hydrogen peroxide solutions, there is no excessive oxidation of the aluminum. Only at very high and very low pH values are aluminum and its oxides soluble.

Before concluding the subject of metal etching and cleaning, it is worthwhile to highlight two common phenomena encountered in metal line cleaning. The first is known as pitting, or "mouse bites" – tiny holes observed in the side of metal lines when viewed by SEM. Although frequently ascribed to cleaning issues, most pitting is the result of selective, electrochemical attack on $\theta$-phase $Al_2Cu$ [33], although different chemical cleaning solutions will cause pitting at different rates – for example, sparging the rinsing water with $CO_2$ [34]. The second is a phenomenon known as W-plug attack, further discussed in Section 9.3.1. This can occur during post-Al etch cleaning when a metal line is misaligned with an underlying W plug exposing the W, the metal liner/adhesion layer between the W, and the metal line, to the wet cleaning treatment. This was first observed in the late 1990's as device critical dimensions dropped below 0.35 μm.

A variety of factors appear to be involved with W plug corrosion. Surface charging at the W surface resulting from the etch and/or ash processes is believed to play a role [35]. However, observations have shown that a given W plug might be attacked while an adjacent plug remains intact during cleaning. Thus, other contributing factors have been postulated, including:

1. Whether a plug is electrically grounded or floating. Grounded plugs are less susceptible to corrosion [36].
2. Whether or not a given W plug is connected to an N+ or P+ transistor device at the semiconductor front end. The N+ connections are less likely to exhibit W corrosion [37].
3. The size of the Al contacts both above and below a given W plug. The larger the area of contact to the metal levels, the less likely plug attack is to take place [33].
4. The contribution of ambient light; it is postulated to induce or enhance tungsten attack [38].
5. The chemical nature of the post-etch residue cleaning step following plasma etch. Alkaline solutions that contain hydroxylamine appear to exacerbate tungsten corrosion [39, 40].

As a result of this long list of potential factors, a variety of solutions emerged to mitigate exposed tungsten plug attack by, for example, employing a light shield to reduce ambient light shining on the wafer during cleaning and/or changing the cleaning chemical. However, based on the proposed theory of surface charging during plasma processing, many creative approaches to dissipating this surface charge have been documented, including:

1. Ensuring that the W plug is designed to be electrically grounded [35].
2. Adding water or hydrogen gases to $O_2$ stripping chemistries [41].
3. Exposing a wafer to ionized air prior to residue cleaning [42].
4. Treating the wafer surface with one of an assortment of liquids intended to dispel charge through ionic conductivity:
   a. Immersing the wafers in KOH, $NH_4OH$, $Na_2CO_3$, or sodium acetate [43].
   b. Contacting with liquid mercury [44].
   c. Treating with dilute nitric acid to passivate the W layer [45].

### 9.2.3 Post-via Etch Cleaning

The metal lines described in Section 9.2.2 are connected by vias that are normally filled with W, and less commonly with Al. Figure 9.6 shows a schematic of the via formation process. Prior to via filling, a cleaning step is required. However, if complete and effective cleaning is not accomplished, subsequent metal deposition steps are likely to result in poor step coverage and potential failures due to delamination and electromigration. In addition, cleaning is necessary so that subsequent metal steps form a good electrical contact to the underlying metal, because the contact resistance for vias is a key parameter for interconnect performance [46]. In this case the silicon oxide, such as tetraethyl orthosilicate (TEOS),

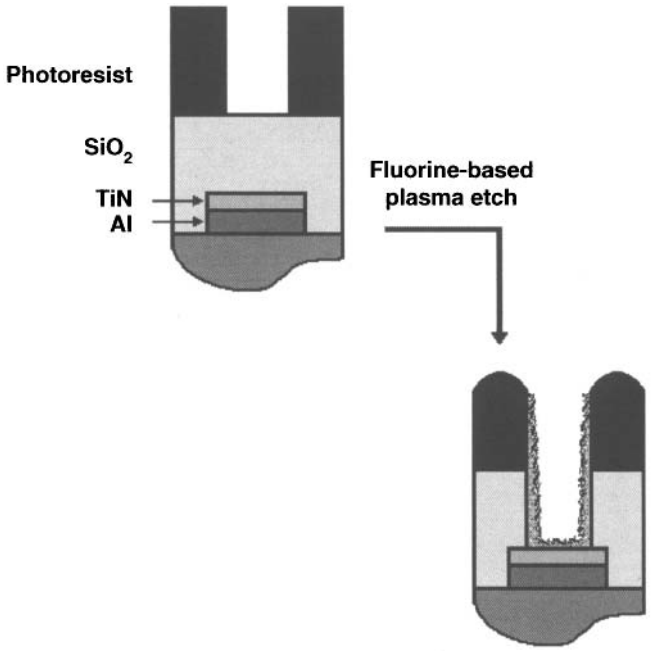



**Figure 9.6.** Schematic of a) Al via etching and b) residue creation. Used with permission of the author.

spin-on glass (SOG), borophoshosilicate glass (BPSG), or other similar dielectric material is etched. The process to etch the dielectric is typically performed with a fluorocarbon-containing plasma, with or without hydrogen incorporated on the fluorocarbon molecule, according to the following reaction:

$$SiO_2 + 4\,[F] + \text{hydrocarbon} \rightarrow SiF_4(g) + H_2O(g) + CO_2(g) \qquad (9.9)$$

Ideally the amount of residue remaining on the via sidewalls is minimal, due to the cleanliness of the etch reaction, which is a result of the exceptionally high bond strength between silicon and fluorine (582 kcal $mol^{-1}$), leading to a strong thermodynamic driving force for this reaction to take place and a concomitant reduction in occurrences of side reactions. However, if the etch process has not been optimized, it is possible to create large amounts of highly intractable, insoluble residues that have been referred to as polymers due to their chemical similarity (and associated lack of reactivity) to Teflon®, poly(tetrafluoroethylene) (PTFE) [47]. This is especially true if $:CF_2$ monomers form, which can easily form long chain polymeric-type residue similar to PTFE [48]. The bulk of the residue forms as the via is etched to completion when the TiN or underlying metal layer is exposed, as shown in Figures 9.7. As over-etching continues, especially if the TiN is completely etched and the much softer aluminum is exposed, punch-through occurs, and more metal-based residue is sputtered onto the walls of the via. In extreme cases, an abundance of residue is formed that can be very difficult to remove.

It is widely-known that via cleaning, especially in the punch-through case, is typically more challenging than Al line cleaning. It is frequently assumed that this difference arises from the fact that vias are small and cylindrical, often with high aspect ratios, whereas Al lines have relatively more exposed area and smaller aspect ratios.

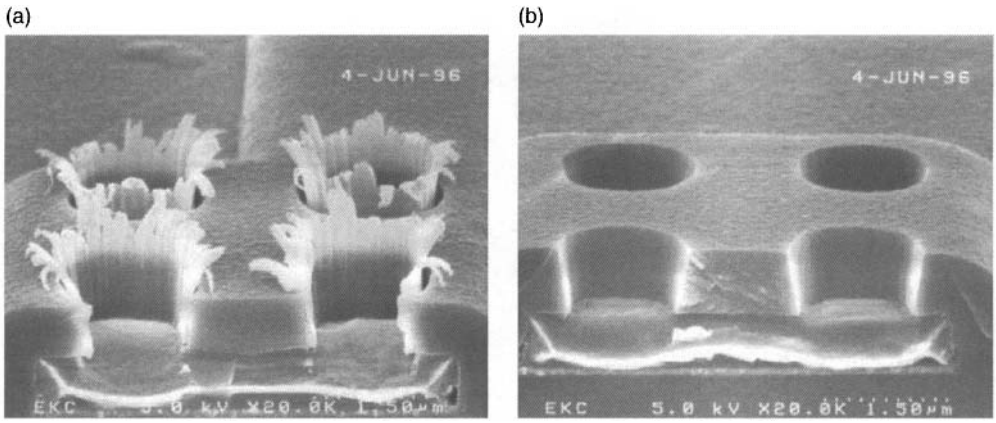



**Figure 9.7.** Scanning electron microscope image of via field a) showing residue remaining after etching and stripping and b) showing residue removal after cleaning. Courtesy of DuPont/EKC Technology (2010).

Thus, the difference in mass transfer between the two cases – the ease with which a cleaning solution can get into and out of the effected spaces – makes the via cleaning more difficult due to the increased time it takes to wet the surface at the bottom of the via feature. However, this is not the dominant reason why via cleaning is challenging. Much more important is that in this case the residues are predominantly formed at the end of via etch when fluorine plasma is impinging on TiN and perhaps Al. Therefore, the residues are comprised of aluminum and titanium fluoride and oxide species [13, 49] resulting from the plasma etch and resist stripping processes.

Representative EDS and AES spectra of via sidewalls embedded with Ti and fluorocarbon residue are shown in Figures 9.8 and 9.9, respectively. The EDS spectra in Figure 9.8a show residue on the sidewall of the via. Data was also collected by the researchers at the bottom of the via that indicated different resides are formed – less fluoride is found at the bottom of the via and the thickness of the residue is less than on the sidewall. Figure 9.8b shows that after $O_2$ plasma stripping, Ti is still present on the sidewall and a significant amount of carbon is still present. Nevertheless, these titanium fluoride species are hard to remove, as evidenced by their high melting points, shown in Table 9.2.

At the top metal level of a typical integrated circuit device, metal bond pads are formed that will ultimately be employed as contact points to connect the finished device to the package. The formation of these pads is very similar to via formation; however, they are larger in size than vias. Fluoride-based plasma is used to etch the passivation dielectric layers to reveal the metal (usually aluminum) pads below. Following oxygen plasma to remove photoresist, the remaining residues are similar to those made during via etching, and are $Al_wTi_xO_yF_z$ in nature. Post-strip cleaning typically is the same for both via and bond pads.

## 9.3 Chemistry Considerations for Cleans Following Etching

Having described the different types of residues formed in the main Al interconnect processes, the next logical step is to discuss the types of wet chemical cleans

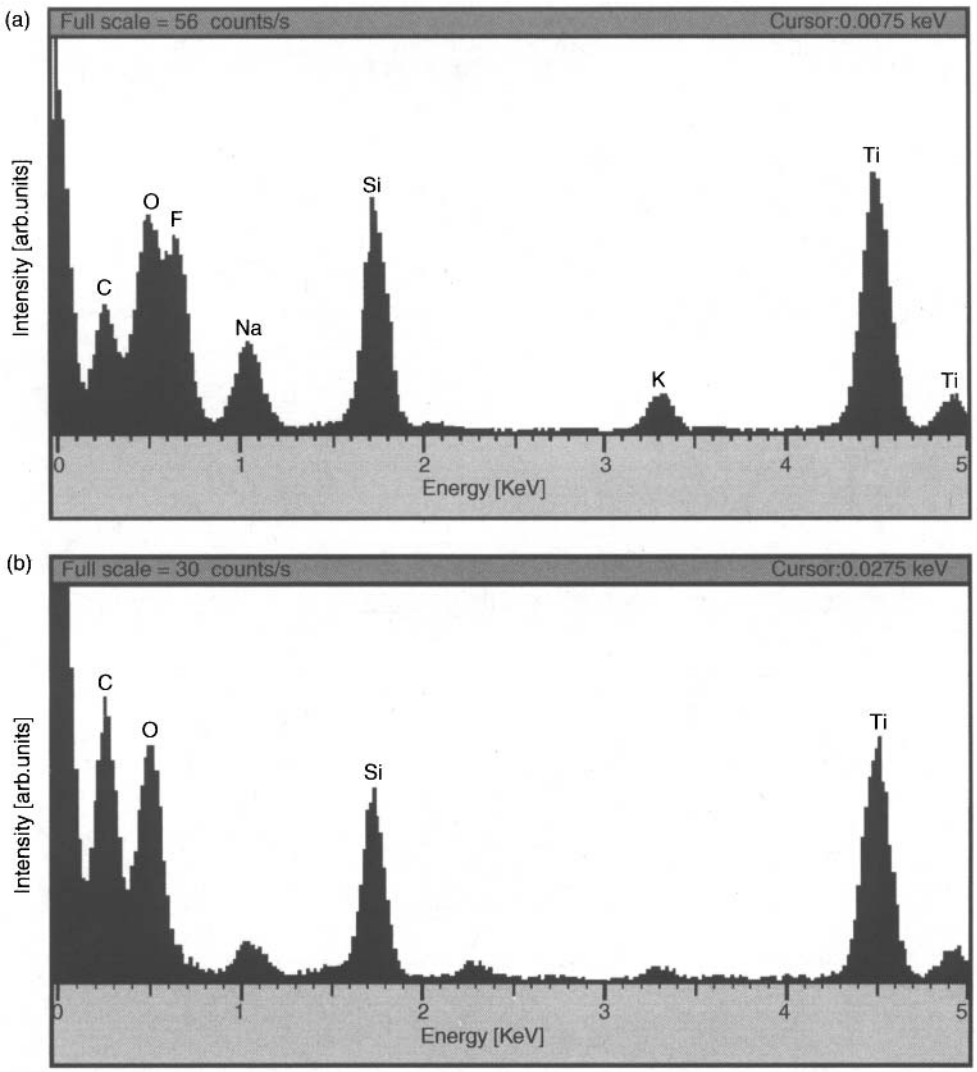



**Figure 9.8.** Example EDS spectra of sidewall via residue a) before and b) after $O_2$ plasma stripping [13]. The Na and K signals probably are due to the sample preparation. Reproduced with permission of ECS – The Electrochemical Society from Song, J., Kim, J., Seo, H., Kim, Y., and Jeon, H., *Journal of the Electrochemical Society.*

that may be used. A summary of the different types of residues formed, described in Section 9.2, is shown in Table 9.3.

The chemical makeup of these residues largely determines the types of cleaning chemicals that are suitable for each process step. Prior to the introduction of formulated chemical blends that were specifically designed to selectively clean the associated residue produced for each process step, progressively longer and hotter solvent treatments were employed. Examples of the chemicals used are N-methyl pyrrolidone (NMP), monoethanolamine (MEA), sulfolane, dimethylacetamide (DMAC), and dimethylsulfoxide (DMSO), the progression of which is discussed in Chapter 5. Due to the increasing complexity of the residue, the solvents employed met with decreasing success owing to the higher degree of anisotropy of the etch process that deposited a thicker polymer, and the increasing prevalence of $O_2$

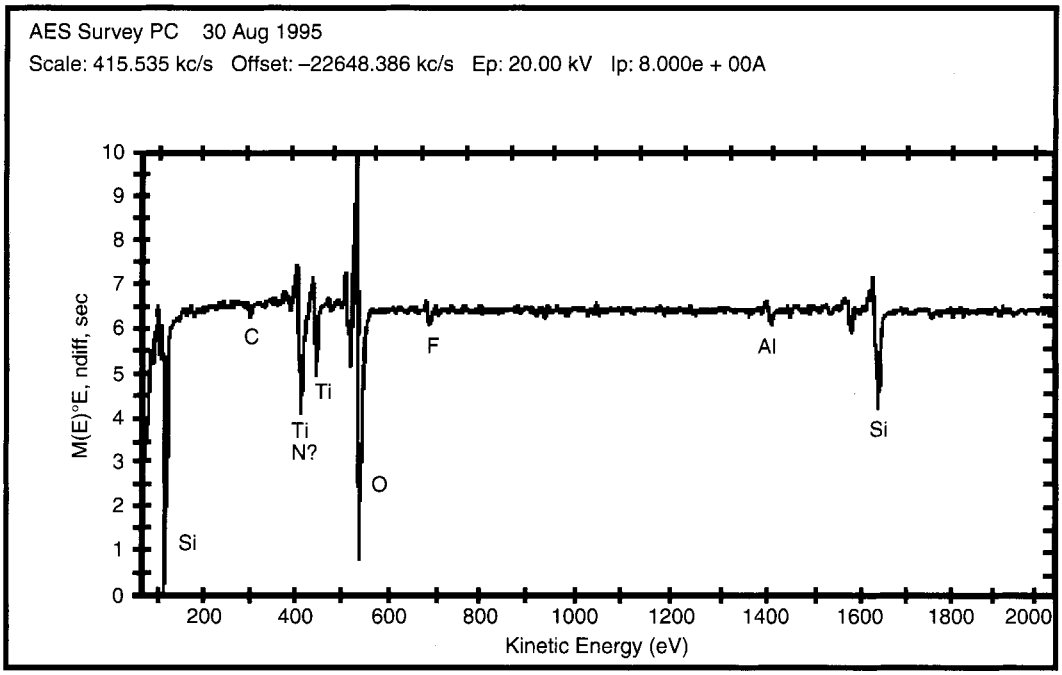



**Figure 9.9.** Example of Auger electron analysis spectrum of sidewall via residue after $O_2$ plasma stripping [49]. Reproduced with permission of ECS – The Electrochemical Society from Wang, Y., Graham, S. W., Chan, L., and Loong, S., *Journal of the Electrochemical Society*.

**Table 9.3.** Summary of residues formed during Al interconnect etch steps.

| Section in Chapter | Process Step | Types of Residues Present |
|---|---|---|
| 9.2.1 | Etchback | W, $TiF_x$ |
| 9.2.2 | Metal Etch | $Si_xO_yCl_z$, $Ti_xO_yCl_z$ |
| 9.2.3 | Via/Pad Etch | $Al_wTi_xO_yF_z$ |

plasma used for photoresist removal. The oxygen plasma chemistries removed the photoresist, but modified the residue, often oxidizing the sputtered metallic species. Thus, the modern wet cleaning chemicals used for the removal of these residues fall into three general categories:

1. Controlled wet etching/selectivity with solutions containing fluoride.
2. Reduction/saponification using solutions containing hydroxylamine.
3. Controlled wet etching/selectivity/oxidation with dilute mixtures of fluoride, acid, and other additives.

Each of these will be addressed in turn.

### 9.3.1 Fluoride-based Cleaning Formulations

There are many fluoride-based cleaning formulations available and they vary primarily by concentration of fluoride, pH, solvent and water content, and the

presence of various metal complexing agents (typically carboxylic acids). The pH of a fluoride-based cleaning solution is a key predictor of its performance. This is due to the well-known speciation of fluoride anion as a function of pH and the differing effects of these species for etching silicon-based materials [50]. Besides fluoride speciation, there are other tradeoffs that must be considered as the pH of a fluoride-containing solution is changed. Under acidic conditions, the activity of fluoride tends to increase possibly leading to loss of oxide and metal, but the bath is stable, as measured by the stability of the pH value [51]. Under more basic conditions it is easier to control metal corrosion and the cleaning efficiency is assisted by the presence of hydroxide ions, which are strong nucleophiles and attack the metal-based residues, but pH stability tends to be worse. Fluoride-based cleans predominately fall in these three sub-classes:

1. Buffered oxide etch (BOE). Originally developed for wet etching of $SiO_2$, BOE is used for post-Al etch cleaning in less demanding technologies. It is referred to as buffered because it is comprised of a classical chemical buffer solution – a weak acid (in this case, HF) in the presence of its conjugate base ($NH_4F$). By varying the concentration of these two species the stabilized pH of the mixture can be tailored to a desired value, desirably impacting the mixture's etching rate [52]. Buffered oxide etch solutions are typically acidic having a pH of >3.4 (the pH of 49 wt% HF). Most BOE have pH values of 3–6 for 5:1 to 10:1 40 wt% $NH_4F$:49 wt% HF where higher fractions of 40 wt% $NH_4F$ increase the pH value. However, the simple nature of the solution and low cost of its components permit point-of-use mixing to a desired pH for process-specific tuning. Surfactants can be added to BOE solutions to allow wetting of high aspect ratio features or hydrophobic surfaces and glycols can be included to regulate the selectivity between doped and undoped silicon oxides. Ready-to-use BOE mixtures are commercially available from JTBaker, KMG Chemicals, and Honeywell Electronic Materials.
2. Dilute sulfuric acid hydrogen peroxide mixtures ($H_2SO_4/H_2O_2$) optionally with very dilute HF added are referred to as dilute sulfuric-peroxide, or DSP (without HF added) [53] or DSP+ (with HF added) [54, 55]. These solutions are advantageous due to the low costs for all of the components and because the blends are very dilute. As with BOE they are conveniently made at point-of-use, allowing for individual concentration tailoring for a specific process, and their high dilution and low cost allow a solution to be discarded after use on a single wafer. This is advantageous for single-wafer processing because it beneficially impacts the cost of ownership and also allows for high wafer-to-wafer consistency.
3. Proprietary formulated blends. There are a great number of commercially available formulated products for aluminum interconnect cleaning available on the market today. All employ a flouride species such as HF, $NH_4F$, or the addition product of these two fluoride sources ($NH_4HF_2$, ammonium bifluoride); water, an organic solvent such as DMAC, DMSO, or NMP; optionally chelating or complexing

agents to assist in metal ion removal and adjust solution pH (e.g., carboxylic acids such as citric acid, aliphatic amines such as MEA), and other proprietary additives. The fluoride chemistries are generally composed of polar solvent, water, fluoride, a buffer agent, and possibly corrosion inhibitor [56].

Subsets 1) and 2) are typically strongly acidic while the proprietary products range from strongly acidic to mildly basic (~8–9). A solution pH just above neutral allows for some cleaning activity to come from the presence of $OH^-$ which is advantageous in these cleaning processes this will be further discussed in Section 9.3.2.

### *9.3.1.1 Applications*

For tungsten etchback and post-Al etch cleaning, fluoride-based formulations, including BOE and DSP+, are effective because they form soluble Ti and W fluorides under acidic conditions. Tungsten fluoride reacts with water to form $WOF_4$ [57], as shown in Eq. 9.10. Several titanium species are water-soluble and $TiO_2$ is slightly soluble in HF solution [58], as shown in Eq. 9.11:

$$WF_6 + H_2O \rightarrow WOF_4 + 2\,HF \tag{9.10}$$

$$TiO_2 + 2\,HF \rightarrow TiOF_2 + H_2O \tag{9.11}$$

Besides etching the metallic residues, the fluoride can etch the aluminum, but $Al_2O_3$ surface passivation precludes all but the most aggressive etching conditions. However, the sulfates in DSP solutions can be quite tenacious and hard to rinse, so may become incorporated into the oxide passivation layer formation during cleaning if hydrogen peroxide is not present.

The fluoride chemistry assists by mildly etching the underlying $SiO_2$ to assist with cleaning by undercutting the residues and lifting them off the oxide surface. For removal of metal line post-etch residues, the fluoride species can be effective due to the predominance of $SiO_x$ as a major component of the residue. Some researchers have speculated that the fluoride cleaning solutions not only undercut the silicon oxide to lift off the residue, but also chemically react with the non-water soluble polymeric material allowing the resulting product to be solvated by the solution [51]. Buffering of the fluoride formulations is necessary to provide consistent etching rates of silicon oxide. Small variations in $F^-$ concentration have shown to have a large effect on etching rates of un-buffered solutions [51]; thus, evaporation or carry-over of rinsing water, may decrease or increase the etching rate, rendering unacceptable process results.

Because of the silicon etching and because the Ti and Al fluoride-based residues are polymeric and tough in nature, via and pad cleaning has proven much more challenging for fluoride-based cleaning solutions. In essence these residues are already fully fluoridated; therefore, a lift-off mechanism dominates for via/pad cleaning in which the solution fluoride attacks the silicon oxide film of the interlevel dielectric. Via and bond pad cleaning applications exist for fluoride-containing cleaning solutions [59], but this is the not the predominant application for these chemistries.

In general, fluoride-based cleaning finds its most popular applications in etch-back cleanup and Al line post-etching cleaning. This is especially true in the latter application due to the nature of the residues, the fast, room-temperature operating conditions and the low cost-of-ownership afforded by most of the products in this class [60]. However, it is important to note that especially for fluoride-based cleans that the plasma stripping process prior to residue cleaning must be 100% effective, because the subsequent wet clean will be not be effective at removing any organic contamination, such as thick residual photoresist that remains after a poor stripping step. However, there are incidences where a fluoride containing chemistry has been proposed for photoresist stripping. [61].

Fluoride-containing formulations have been shown to be successful for cleaning aluminum metal lines with exposed tungsten vias that are susceptible to corrosion when a hydroxylamine chemistry is used for cleaning, discussed in Section 9.3.2. Corrosion inhibitors are used in fluoride-based mixtures [51], such as amines, carboxylic acids, or diols [62]. The tungsten erosion is thought to occur because of galvanic corrosion, as shown in Figure 9.10, and is discussed in detail in Section 9.2.2. This is type of corrosion is also seen in HF when 0.5% copper is included in the aluminum [33] for electromigration mitigation; however, this is not seen when cleaning solution with fluoride, perhaps in part because its in a basic alkaline nature. [32].

### 9.3.1.2 *Process Conditions*

One of the biggest advantages of fluoride-based cleaning processes is that they typically proceed quickly (<1–5 min) under low temperature conditions (20–40°C). These moderate operating conditions are due to fluoride cleaning depending primarily on its strong interaction with Si species; thus, kinetic energy (higher temperatures, long process times) is not required to effect cleaning. For these reasons fluoride solutions are easy to rinse following the cleaning process, as discussed in Section 9.4.1 and are adaptable to a variety of equipment sets, including single wafer [63], spin spray [64], and batch immersion (discussed further in Section 9.4.2).

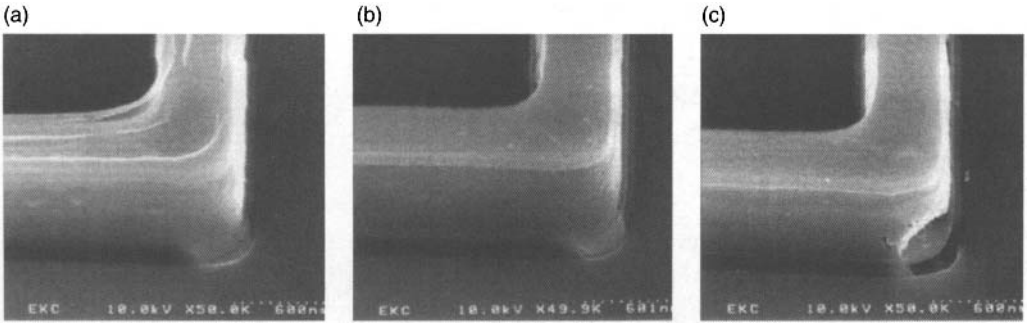



**Figure 9.10.** Scanning electron microscope images of metal lines over tungsten-filled via a) showing residue remaining after etching and stripping and showing residue removal after cleaning illustrating b) an intact tungsten via, and c) a corroded tungsten via. Courtesy of DuPont/EKC Technology (2010).

Typically, the amount of silicon oxide removed increases with $F^-$concentration (more accurately, $HF_2^-$ concentration) and with temperature. Increases in both parameters result in an increase of the oxide etching rate. Fluoride can be added to amine solutions, thus permitting effective modulation of the etching rate of the silicon dioxide in the cleaning solution [65]. Too much oxide removal can be a problem with un-buffered solutions.

The active component concentrations for DSP+ are $H_2SO_4$ ~5–10 wt%, $H_2O_2$ ~5–10 wt%, and HF (50–200 ppm). For these solutions, point-of-use mixing for batch spin-spray and single wafer allows for fresh chemical to be dispensed on the wafer. The temperature must be regulated as the mixing generates heat and can rise to 35°C from ambient in a batch spin spray system. Special pre-cooling is available to regulate the temperature further. However, higher temperatures (55°C) have been reported for batch processing [66]. For DSP+ cleaning, the fluoride concentration is very low (in the ppm regime) and must be kept very stable [63] because the solution is not buffered to prevent overetching of the silicon oxide for both vias and metal lines post-etch cleaning.

Although fluoride-containing formulations are easy to rinse, some special precautions must be taken to neutralize the chemical after the process is complete. It is important that the deionized water (DIW) rinse procedures for formulated fluoride chemistries be optimized: excess water rinsing needs to be avoided because of possible secondary metal corrosion [67]. This is not primarily to prevent corrosion of the aluminum, but to completely remove the by-products of the cleaning process [59] suggesting possible value of an intermediate DIW rinse between two chemical dispense steps. Additionally, it was found that $CO_2$ sparging can have an effect on metal integrity of the aluminum lines, [68] confirming the work of Scully [34]. Generally, most processes only require a single deionized water rinse at the end of the cleaning step.

Bath lifetime of buffered fluoride solutions can be quite long, greater than 12 hours in some cases; however, with single wafer point-of-use processes, the chemicals typically are used only once before being discarded. Many of the proprietary formulated blends, especially the mildly basic formulations (~pH 8), unlike many traditional solvent cleaning chemistries, are tolerant of extraneous water during single wafer and spin spray tool operation. The addition of 5–10 vol% water into many of these proprietary formulations does not significantly increase silicon oxide or Al etching rate, nor impact cleaning performance. In contrast, the loss of water from these formulations in single wafer tools (in cases of recirculated chemical) has shown to increase the oxide etching rates.

### 9.3.2 Cleaning with Hydroxylamine

There are several commercially-available cleaning formulations that rely on the use of hydroxylamine ($NH_2OH$) and these represent the single most successful class of cleaning formulations for aluminum interconnect [69, 70]. Originally developed in the early 1990's [71, 72], most are based on hydroxylamine as the free base (HAFB), although products based on hydroxylamine sulfate and optionally a fluoride component [73] have also been developed. These products usually contain organic primary amines ($R\text{-}NH_2$), water and one of several aromatic chelating

agents that assist in cleaning and aid in the protection of sensitive metals, particularly Ti. As a result, they are quite alkaline (pH 11–12) and under these conditions the hydroxylamine serves as a strong reducing agent and exists predominantly (in dynamic equilibrium) as an anion:

$$NH_2OH + OH^- \leftrightarrow NH_2O^- + H_2O \tag{9.12}$$

This anion ($NH_2O^-$) is a very strong nucleophile and attacks metal-based residues very effectively. Once attacked, the highly oxidized species that comprise the residues are temporarily reduced to a lower oxidation state, breaking bonds in the process. This nucleophilic attack/chemical reduction process drives the cleaning efficacy of the hydroxylamine-based cleaning solutions.

Thus, the primary role of hydroxylamine is to chemically reduce the organometallic species comprising the residues. There are typically 3–4 other components of hydroxylamine-based cleaning products, as follows:

1. Water. Hydroxylamine free base is produced commercially as a 50 wt% solution in water. More water may be added by the commercial suppliers as fits the target cleaning application.
2. A primary amine. The presence of a primary amine serves several purposes. As a good complexing agent, it assists in holding dissolved metal ions in solution. As a moderately strong base, it generates substantial quantities of $OH^-$. This is valuable for cleaning as discussed below. This adjustment keeps the formulation in a high pH regime in which HAFB is a strong reducing agent.
3. A chelating agent. Typically, derivatives of aromatic 1,2-diols are extremely strong chelating agents under basic conditions. Their use also protects metals present at the semiconductor surface, especially titanium.

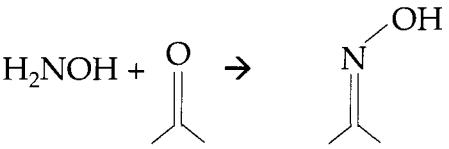
A series of commercially-available cleaning products are available from several companies and these are summarized in Table 9.4.

It is likely that at least two other mechanisms are at work assisting the cleaning process. The first mechanism relies on the presence of hydroxide ion, which is also a strong nucleophile and will assist in dissolving residues. The pH of formulations based on HAFB is typically ~11–12, basic enough to provide a modest lift-off mechanism for residue removal, but not so basic as to severely attack Al, silicon, or silicon oxides. The second mechanism, in case there is any remaining residue after

**Table 9.4.** Summary of hydroxylamine-based formulations.

| | |
|---|---|
| AirProducts/ACT | ACT935™ |
| DuPont/EKC Technology | EKC HDA® Series: EKC265™, EKC270™, EKC270™-T |
| Fujifilm Arch | MS5000™ Series |

a less-than-perfect plasma stripping step, relies on the well-known propensity of hydroxylamine to react with carbonyl groups (if present) to form soluble oximes [74]:




(9.13)

### 9.3.2.1 *Applications*

As with the fluoride-based cleans discussed in Section 9.3.1, hydroxylamine-based chemicals have been employed successfully for etchback, metal, and via/pad cleaning processes. However, the greatest advantage to this approach is revealed in via/pad cleaning processes, because the residues ($Al_wTi_xO_yF_z$ in nature) are very difficult to remove through the use of a fluoride-based chemistry. The mechanism for the residues removal using hydroxylamine is theorized to rely on:

1. The reduction of the metal. Lower oxidation states of metals are usually more water soluble. Additionally, the chemical reduction forces chemical bonds to break during the reductive-elimination process, thereby assisting in residue removal.
2. Complexing the reduced metal center. This occurs by forming a soluble species, using nitrogen-donating chelating agents.
3. Simple dissolution in water [75].

Post-etch residues react differently with fluoride-based and hydroxylamine cleaning solutions. Although the removal is by different mechanisms, it is unclear why one formulation behaves better than others. One theory is that the stripping (and possible the etching) process before the removal is a cause. Polymers that are heavily depleted of carbon, such as those found after a high temperature plasma stripping process, are not removed as quickly in a hydroxylamine chemistry [13] as with a fluoride chemistry. This is because the polymer can be lifted off in a fluoride reaction while hydroxylamine requires residue dissolution. The etching of oxide is low with most hydroxylamine formulations, and therefore the mechanism of lift-off is not as prevalent. Figure 9.11 shows a via after oxygen plasma stripping and then after hydroxylamine cleaning solution to remove the metal-containing residue.

### 9.3.2.2 *Process Conditions*

The powerful cleaning capability associated with hydroxylamine-based chemicals comes with some process trade-offs. In contrast to the recipes used in conjunction with fluoride-based processes, hydroxylamine-based processes are typically quite long (10–30 min) for batch processes and run at elevated temperatures, ~60–75°C. As such, hydroxylamine cleans are not well-suited to single-wafer processing. The elevated temperatures also contribute to the most common failure mode associated with these cleans – water loss from the chemical bath. Since the cleaning mechanism relies on water as a source of hydroxide for cleaning as well

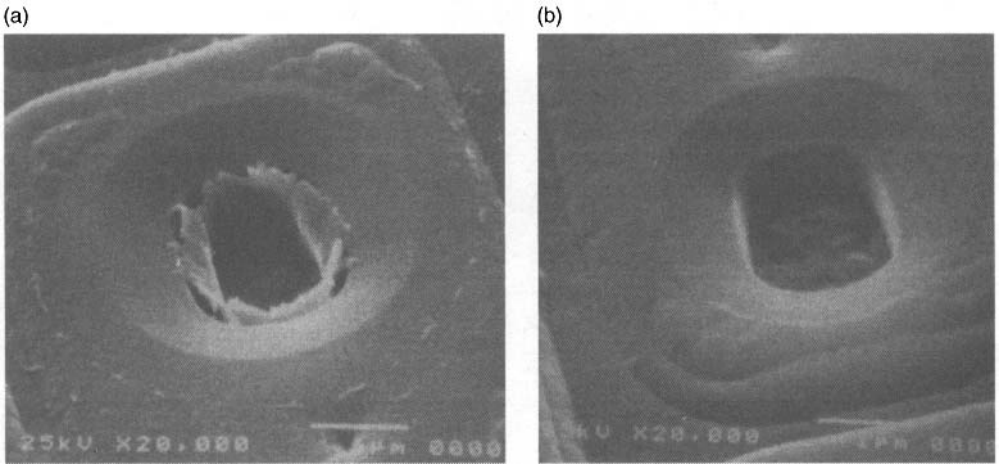



**Figure 9.11.** Scanning electron microscope images of a via over metal a) showing residue remaining after oxygen stripping and b) after processing with a hydroxylamine-based cleaning formulation [75]. Reproduced with permission of ECS – The Electrochemical Society from Lee, W.M., *Proceedings of the Symposia on Interconnects, Contact Metalization, and Multilevel Metallization.*

as forming the hydroxylamine anion, evaporative losses eventually lead to a lowering of a formulation's effectiveness. Alternately, water addition also alters the formulation's effectiveness.

The goal of extending the bath life (typically ~12 to 24 hours) by monitoring by titration or one of a variety of in-line analytical tools to determine the chemical concentration, followed by spiking with the appropriate chemicals, is sometimes performed to help moderate effects from water loss. This technique is general and not limited to water replenishment, although in practice water spiking is the most common. Monitoring may minimize the risks associated with such processes; however, before introducing monitoring, the savings they provide must be assessed, and only if greater than the risk, should be implemented. Other successful approaches to improve bath life include:

1. Operating at as low a temperature as possible while still providing adequate cleaning.
2. Cooling and covering solutions when not in use.
3. Carefully monitoring air/gas flow rates over the cleaning solution to the lowest safe level.

## 9.4 Rinsing/Drying and Equipment Considerations

### 9.4.1 Rinsing/Drying

From a chemical standpoint, there is really only one decision that needs to be made during the rinsing process – whether or not an intermediate (*i.e.*, non-water) rinse is required prior to water rinsing and drying. For the removal of highly aqueous

solutions, especially those that are of acidic or neutral pH, normally a DIW rinse is adequate, for a number of reasons:

1. The pH change seen by the wafer surface will take place very quickly as there is excellent miscibility between water and the cleaning formulation in question.
2. The cleaning formulation is typically run at room temperature and so no viscosity change takes place as there is little temperature drop on rinsing.
3. The direction of pH change (especially from acidic → neutral) allows for formation and preservation of an aluminum passivation layer ($Al_2O_3$) that prevents Al corrosion during the rinse process.

For the removal of solvent-heavy and/or basic formulations – especially those at higher temperatures – an intermediate solvent rinse before the $H_2O$ rinse typically uses isopropanol (IPA), less commonly NMP, and even less commonly DMSO. The reason is that these cleaning solutions are basic, contain amine species, and generate large quantities of hydroxide ion ($OH^-$) at the wafer surface during a straight-to-water rinse, and this $OH^-$ can corrode Al. An intermediate rinse dilutes the amine at the wafer surface and these solvents do not undergo acid-base reactions with water during the final rinse.

Another method of neutralizing hydroxide during a rinse process is to have the wafers placed from the cleaning solution directly into DIW that has been saturated with carbon dioxide ($CO_2$). This generates carbonic acid according to the following reaction:

$$CO_2 + H_2O \leftrightarrow H_2CO_3 \leftrightarrow 2\,H^+ + HCO_3^- \tag{9.14}$$

When saturated, the carbonated water has a pH of ~ 5.5–6.0 making the rinse more effective for hydroxide neutralization, valuable for alkaline, amine-based formulations containing hydroxylamine, where corrosion is caused by a large change in pH (4–5 pH units) when moving the wafers from the alkaline cleaning bath to the neutral DIW rinse [76]. The acidic carbonated water quickly neutralizes the hydroxide and mitigates corrosion.

A water rinse with above ambient temperature should not be used with aluminum metal line or exposed aluminum in the via holes, because even from the diluted cleaning chemical, etching of the metal can occur [77]. This is especially prevalent when chlorine-containing residue is present in the post-etch metal residue, and slightly-acidic DIW is used, forming dilute HCl, that can etch the metal. This corrosion can be latent, occurring hours after the wafers have been processed. Although mobile ions are a concern anytime $SiO_2$ is present, they can typically be rinsed effectively after formulated cleaning with a simple, ambient temperature water rinsing process [78]. For high-temperature chemical processing (>150°C in some cases), care must be taken after the residue removal step to allow the wafers to cool before placing in a rinsing step, as the diluted chemical, if sensitive to water, may form compounds that react with the metal.

There have been some formulated products introduced into Al cleaning processes that were designed to complement or replace IPA as a rinse. One example, called EKC4000™ from DuPont/EKC Technology [79], is an aqueous acidic blend that is intended to neutralize amine species from an alkaline cleaning solution. While this approach has been shown to be successful due to the chemical neutralization it affords, it is not common.

Even for basic cleaning solutions, it is possible to engineer a rinsing process that does not require an intermediate solvent treatment. This relies on excellent physical agitation that removes $OH^-$ very quickly from the wafer surface during the rinsing process. This consideration is important and is discussed in the Section outlining the cleaning equipment, Section 9.4.2.

Isopropyl alcohol drying, typically surface tension gradient (STG) or Marangoni-type drying, is used after the rinsing step for metal lines and vias, although spin spray techniques may also be used. The drying step does not typically cause problems. Watermarks, particles, incomplete drying, and other common problems may occur as with any other drying process, but are usually not related to the previous chemical processing step, although corrosion caused by IPA STG drying after an amine-based cleaning chemistry has been reported [80].

## 9.4.2 Equipment

A typical batch immersion system (wet bench) is composed of a chemical processing bath, a tank reserved for intermediate rinsing (usually a cascade/overflow design), and a final DIW rinsing tank, followed by a drying module. The final DIW rinse tank is normally either cascade/overflow or a quick dump rinse (QDR), in which water is sprayed onto the wafer cassette through a series of nozzles and the water is allowed to fill the tank to the top. After the tank is full, a drain is opened and the water quickly flows out of the tank bottom. This cycle is repeated as many times as necessary – it is referred to, for example, 5X QDR, for five fill/drain cycles.

In the case of batch spray tools, intermediate rinse and water solutions are applied through the same nozzles in the spray chamber as the prior cleaning solution with appropriate modification of the spray recipe (*i.e.*, time, spin speed, flow rate) to ensure the most effective process.

For single-wafer processing, the chemical process, rinsing and drying are all performed in the same module. For most single wafer processing tools, there are many modules on one platform to meet the throughput of the batch processing systems. The same parameters must be optimized as with the batch spin spray tools.

Following the rinse from a batch immersion system and optionally following batch spin spray process, the wafer cassette is commonly placed in a spin-rinse dryer (SRD) in which water and then hot nitrogen gas are delivered to the cassette chamber while the cassette is spinning. This final step is helpful in controlling particulate contamination, and there is room for process optimization of this step to maximize cleaning/drying performance at the lowest cost.

For more advanced technologies, such as high aspect ratio vias, a technique known as surface tension gradient drying is frequently used. First developed in the late 1980's for semiconductor applications, it relies on the Marangoni effect, in which a solvent vapor or spray with a lower surface tension (IPA) displaces a

higher surface tension fluid (water). As the wafer is removed from the water, the thin coating of IPA at the top edge of the solution carries away remaining water from the wafer surface leaving a wafer that is completely dry. This technique is well-known and very popular for advanced Al integration and has been described in detail elsewhere [81].

During the chemical cleaning step, the input of sonic energy into the Al cleaning environment has been extensively explored, largely as a carryover from particle removal processes commonly used in front end of line manufacturing. Briefly, megasonic energy transmitted through transducers that are placed around a tank, or for single wafer processes, in the chuck of a wafer holder or by a megasonic rod, or by a megasonic nozzle causing boundary layer thinning, and sometimes cavitation of the cleaning solution. During cavitation, the very small bubbles that are formed quickly collapse, imparting kinetic energy and heat to the substrate, presumably enhancing cleaning. Process optimization is frequently required as there is a risk of cavitation-induced damage on small features such as aluminum metal lines [82]. Many cleaning tools, both batch [83] and single wafer designs [84] are available with megasonic capability.

## 9.5 Alternative and Emerging Cleaning Technologies

As noted in the onset to this chapter, Al integration has reached a state of maturity in semiconductor interconnect and is gradually being supplanted by copper as the interconnect metal. Since its introduction there have been several developments in Al cleaning processes that focus at least in part on environmental, disposal and related cost factors. Some of these have been discussed already, including the use of cleaning solutions with ever-higher amounts of water and lower concentrations of other active ingredients (*i.e.*, DSP and DSP+; efforts by chemical suppliers to formulate products with increased water content [85]); use of ozone for cleaning, optimization of rinsing processes and other activities associated with minimizing the consumption of deionized water; and dry cleaning methods that minimize liquid waste generation.

Additionally, physical forces to remove the residues have been demonstrated, both using chemical through a megasonic chemical dispense nozzle and with water, sometimes with additives, through a high-velocity jet spray nozzle [81]. The use of the single wafer processing tool is accelerating the use of new nozzle designs to provide physical effects for residue removal to augment the chemical effects. Another example of a single wafer cleaning head where the chemical cleaning, rinsing and drying is done in one assembly that passes over the wafer surface has been reported [86].

Another technique using physical force coupled with chemical reactivity is electrohydrodynamic (EHD) spray in which variable size liquid particles (as small as 20 nm) can impinge on a wafer surface with varying velocities [87]. The advantage is that the particle's kinetic energy combined with the droplets chemistries (a wide range of chemistries can be used as long as they are electrically conductive) can remove PER with extremely small quantities of liquid (<10-15 ml per 300-mm wafer).

Another cleaning/drying technique which received considerable attention from about 1995 through 2005 was the use of supercritical fluids [88]. The most popular of these was carbon dioxide ($SCCO_2$) as a result of its easily accessible supercritical point (pressure and temperature), the relatively benign environmental impact of closed-system $CO_2$ and the fact that carbon dioxide in its supercritical state has zero surface tension and low viscosity, making it very good at wetting semiconductor materials surfaces. Thus, the ability of $SCCO_2$ to penetrate and clean device geometries of high aspect ratio and tight dimensions was expected to be excellent.

As a result of these favorable properties, $SCCO_2$ has been studied in a variety of applications [89], including photoresist spin coating and developing [90, 91], the removal of photoresist after etching [92–94], post-etch residue cleaning [95], and drying [96]. For almost all of these applications, it has been found necessary to formulate the supercritical fluid with additives [97] since carbon dioxide is nonpolar and many of its potential semiconductor applications require some polarity-induced solvency to be effective. It follows that polar additives to carbon dioxide are typically only sparingly soluble in $SCCO_2$ itself limiting the effective concentration range for additives and thus their efficacy; however, IPA is fairly soluble. Other interesting work includes densified fluid cleaning, which is near the supercritical regime. Also Hess has demonstrated resist removal, by adjusting the pH of tetramethyl ammonium hydroxide (TMAH) in $SCCO_2$ [98]. So far as Al cleaning is concerned, it is fair to say that thus far $SCCO_2$ has played only a limited role.

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# 10

# Low-κ/Cu Cleaning and Drying

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*Abstract*
Copper metal interconnects and porous low dielectric constant insulators have been chosen for integration schemes to reduce the resistivity and the capacitance delay in advanced IC devices. The use of these materials within the damascene integration schemes provides substantial challenges to effectively clean features after etching and chemical mechanical polishing. Plasmas etching and striping processes create residues and low-κ damage. Wet cleans can corrode copper and leave moisture and contaminants in the low-κ material. This chapter discusses the challenges and the presents solutions for post-etch stripping, cleaning, residue removal, and post-CMP processing for low-κ/copper interconnect structures. Using the optimum processing conditions and compatible cleaning chemistries are critical for prevention of the dielectric damage, corrosion, and particle removal, without detrimentally impacting the materials. Optimal wet and dry cleaning processes can effectively clean the surface of the remaining photoresist, post-etch residue while doing minimal damage. Chemical mechanical polishing processes require cleaning to remove slurry particles and to preclude oxidation of copper line structures. Pore sealing and dielectric constant recovery processes have been developed to seal low-κ pores and prevent intrusion of performance disrupting moieties.

***Keywords:*** copper, low-κ, porous low-κ, dielectric constant, interconnects, dual damascene, post-etch cleaning, post-CMP cleaning, pore sealing

## 10.1 Introduction and Overview

Copper interconnects integrated with low dielectric constant (low-κ) materials were introduced into high volume manufacturing in the late 1990's. Although this integration scheme addressed the need for faster devices, the use of new materials and the associated manufacturing processes were different than those used for aluminum interconnects. Consequently, many new processing challenges emerged. Stripping the photoresist, post-strip cleaning and residue removal, and post-chemical mechanical polishing (CMP) in particular are critical for successful manufacturing. These cleaning processes must take into account the chemical and

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mechanical sensitivity of these materials, and at the same time, provide adequate process results in reasonable times. This chapter will discuss the challenges in stripping, cleaning, and residue removal for low-κ/copper interconnect structures. Post-etch and post-CMP processing issues are included. Chapter 11 discusses the corrosion and passivation of the copper surface.

### 10.1.1 Copper Interconnects: Background and Applications

The major challenges the integrated circuit (IC) industry faces for back end of line (BEOL) interconnects are the reduction of the wiring resistance and capacitance (RC delay) and the number of electromigration failures [1]. Copper has replaced aluminum as the material of choice for conducting interconnects especially for high performance IC devices because the need for lower resistance wiring and higher reliability. Additionally, interconnect speed, unlike the transistor gate, is determined by the delay in wiring architecture. Thus, the use of copper high-density interconnects to reduce the number of layers when compared to aluminum; nonetheless, 10 or more levels are needed for current logic devices.

Although copper use solves many problems that limit device performance, copper poses manufacturing challenges. For example, integration requires a barrier layer to prevent electromigration that can lead to electrochemically-induced corrosion. Copper is relatively noble and is much more difficult to etch than aluminum, but under some processing conditions copper is susceptible to oxidation and corrosion. Dual damascene integration schemes used for manufacturing IC copper interconnects have been introduced primarily because of the difficulty of etching copper.

Reliability of the structures that contact the transistors to provide electrical interconnects [2] and the integration of the many different materials in the BEOL stack [3] are the keys to producing devices with the necessary performance and lifetimes. New methodologies must be developed to prevent failures due to contamination, incomplete residue removal, and copper corrosion.

### 10.1.2 Low-κ Dielectrics: Background and Applications

Dielectric materials are used as insulators between the metal interconnect features. The reduction of wiring capacitance with copper lines is achieved by using a low dielectric constant material between the metal levels. Amorphous $SiO_2$ has a dielectric constant (κ) of about 3.9 which is too large for current devices; therefore, low-κ materials were developed to meet these permittivity requirements. These new films are less dense than thermally grown or CVD (chemical vapor deposition) $SiO_2$ films and this present a variety of issues for integration and processing.

Various families of low dielectric constant materials have been developed: carbon-doped oxide (CDO), spin-on glass (SOG), porous silica-based film, organic polymers, and fluorine-doped oxide. The International Technology Roadmap for Semiconductors (ITRS) [4] tables show the κ-value for the films for the various process increments; for 22-nm devices, the film is expected to be porous CDO, also known as SiCOH (organosilicate) for the elements it contains, with a effective κ value between 2.4–2.8 and a bulk κ value of 2.1–2.4. Other dielectric films that

may be used for technologies beyond 32 nm include polyarylene ethers, fluorinated polyarylene ethers, and alkoxysilane compounds, both deposited and spun-on. The carbon content is expected to increase with incorporation of pores to further reduce the dielectric content; 10-30 atomic % carbon is typical. Carbon reduces the dielectric constant, but also reduces the mechanical strength due to reduced network continuity [5], and provides a pathway for higher reactivity with oxygen and chemicals used for IC manufacturing processes, such as resist stripping and post-CMP cleaning. Reviews of low-κ materials and properties that are important for interconnect insulators is given in [6, 7].

Porosity of the low-κ films has evolved – integration schemes for 90 and 65-nm devices first introduced porous materials termed ultra-low-κ (ULK) dielectrics. Porous materials can have variable pore sizes from 1 nm to greater than 3 nm, with various distributions of the pores; open or closed with a tight or variable distribution of hole sizes and various densities of the pores, typically 25–30 volume%. The pore size and distribution can affect the dielectric constant and the mechanical strength of the ULK film [8]. The pores also provide a venue for trapping water and, combined with ULK hydrophilicity after wet processing, leads to an increase in the dielectric constant. Some processing issues due to the use of porous materials are being addressed, but many still remain such as their vulnerability to plasma-induced damage, wet processing, and the mechanical strength during CMP.

Integration of low-κ materials also adds manufacturing challenges [9]. For example, the dielectric is mechanically weaker than an equivalent thickness of $SiO_2$, and the high carbon content makes the dielectric less resistant to oxygen plasma processing during stripping and cleaning. To alleviate some of these issues capping layers, both dielectric and metal, have been included in potential integration schemes. However, the dielectric capping layer (*e.g.* SiN or SiC) has a higher dielectric constant than the ULK film creating additional issues with effective κ between metal lines.

An etch stop layer (ESL) is integral to the process. The ESL can be at the top of the low-κ dielectric, at the interface of the dielectric layers forming the via and the trench, and at the bottom of the dual damascene structure. The materials used are TEOS (tetraethyl orthosilicate), SiC, SiN, or SiON, and typically have higher dielectric constants than the low-κ material, as well. Reduction of ESL thickness or the elimination of these layers increases the susceptibility of the low-κ material to cleaning processes.

### 10.1.3 Copper and Low-κ Integration

The combination of new interconnect conductors and dielectrics for BEOL was first proposed in 1995 by Bohr [10], in which he reasoned that the number of interconnects layers would continue to increase; however, practical limits with respect to manufacturing would be reached unless the materials were changed to obtain the required RC delay. Copper and low-κ dielectrics have evolved as the materials of choice to meet these required electric parameters.

Early integration schemes used copper and $SiO_x$-like materials such as plasma enhanced chemical vapor deposition (PECVD) oxide or fluorine-doped oxide (FSG – fluorosilicate glass) that provide a slight decrease in dielectric constant compared

to $SiO_2$. Since aluminum is a subtractive etching process, the same solution was proposed for copper [11]; however, unlike Al, Cu is very difficult to etch. In 1999 Monteiro proposed an alternative method using a damascene process [12] where the copper is inlayed in the dielectric. Since publication, many variations of the damascene process have been used. A typical dual damascene etching and stripping process flow is shown in Figure 10.1 for the via-first process that is covered in Section 10.2. There can be as many as three separate etching processes for the dual damascene process; via, trench, and barrier open. Pore sealing, designed to repair the damage that is caused by the etching, stripping, and the cleaning process is outlined in Section 10.3. The CMP process flow is shown in Figure 10.2, covered in Section 10.4. Reference [13] outlines the various materials and integration needed for low-κ/copper dual damascene processing.

Compatibility of the stripping, cleaning, and surface conditioning steps with the copper and low-κ materials is critical for successful integration. For post-etch

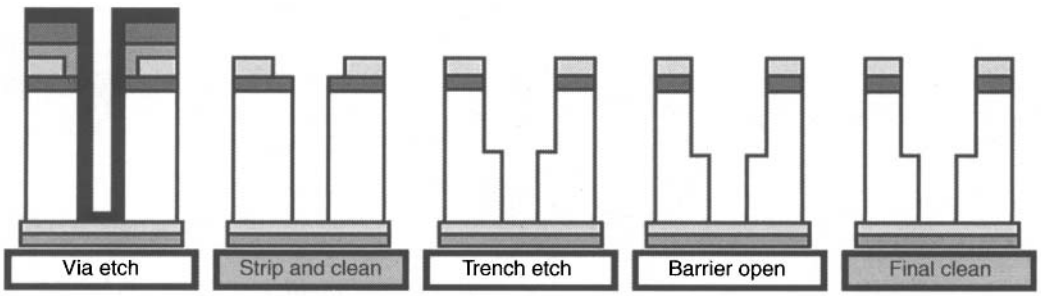



**Figure 10.1.** Cross section schematics of dual damascene of via etch, trench etch, and barrier etch with the strip process flow for a metal hard mask process. Used with permission of the author.

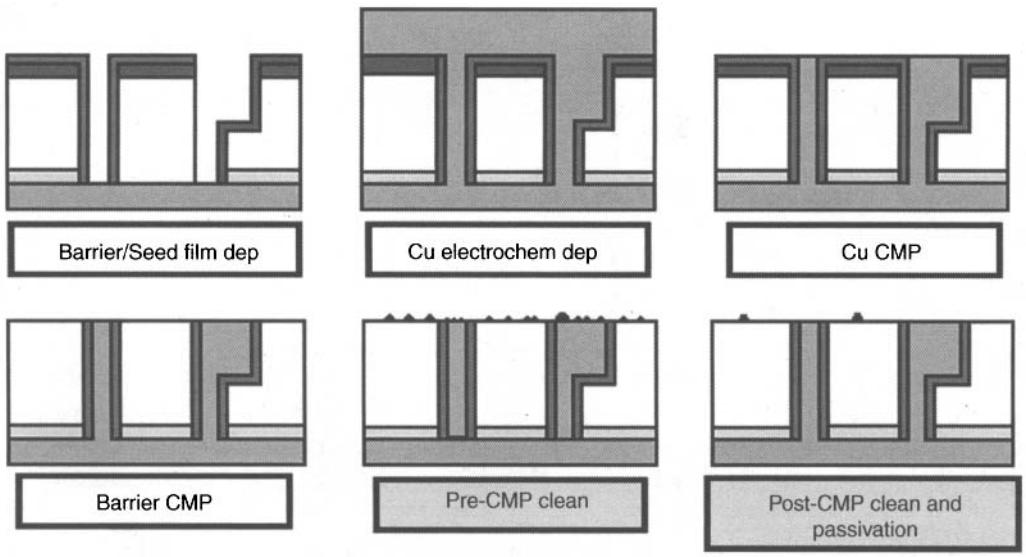



**Figure 10.2.** Cross section schematic of dual damascene with metal deposition and copper CMP with polishing of the etch-stop layer. Used with permission of the author.

stripping and cleaning, plasma and wet processing are the techniques of choice; however, supercritical $CO_2$ ($SCCO_2$) and cryoaerosol processing are also being investigated. For post-CMP processing, wet cleaning is the process of choice and is covered in Section 10.3.

## 10.2 Stripping and Post-etch Residue Removal

The low-κ dielectric via and trench features are delineated by a photolithography process followed by an etching process. After the etching process, the photoresist must be removed. In addition polymer formed by the etching process must be removed. This tenacious fluorine-containing polymer is difficult to remove, and, as the low-κ materials become more carbon-rich and more photoresist-like, stripping and cleaning become more difficult. While the polymer that forms after etching has been well characterized, each etching gas composition and plasma reactor yields residues that are slightly different further complicating the removal process.

Oehrlein has shown that the post-etch residue is composed mainly of carbon and fluorine [14], a highly unreactive combination. Figure 10.3 shows a X-ray photoelectron spectroscopy (XPS) spectrum of post-etch residue on a low-κ surface compared to a fluorocarbon sample showing their chemical similarities [15].

Moore and Meuchel have shown the residue that deposits on the feature sidewall is non-uniform from the top to bottom. While carbon is found at every point on the sidewall, it resides predominantly at the middle to the top of the feature, as well as on the copper surface [16]. Also they have found Cu in the organic residue matrix. Breen and coworkers found that the residue is about 10–20 Å thick primarily deposited on the top surface of the low-κ material with no discernable

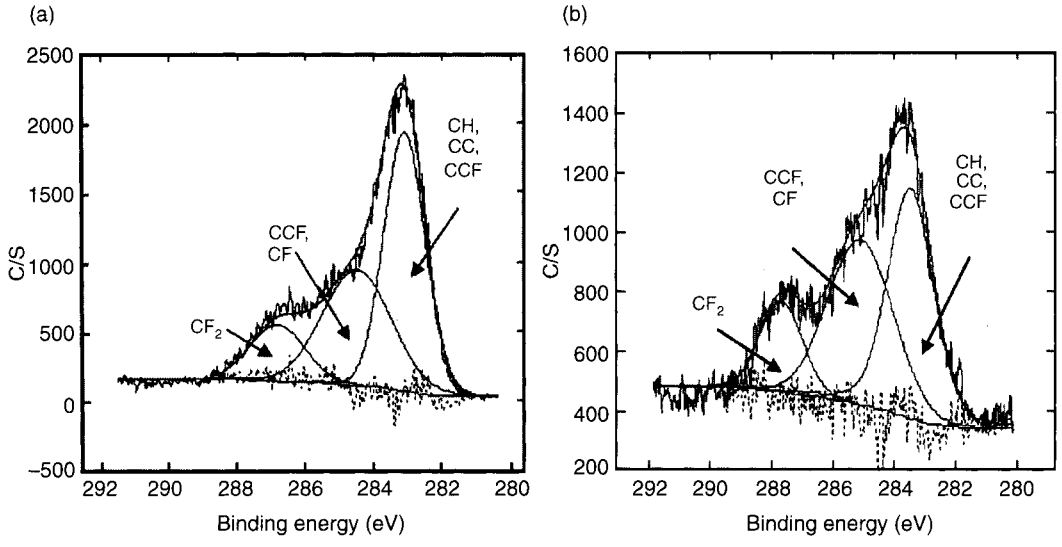



**Figure 10.3.** X-ray photoelectron spectrum of a) residue on the sidewall and bottom of a dual damascene via structure and b) comparison of a fluorocarbon polymer sample obtained from Air Products [15]. Reproduced with permission of ECS – The Electrochemical Society from Levitin, G., Myneni, S., and Hess, D. W., *Journal of the Electrochemical Society.*

deposition on the sidewall [17]. With varying literature reports of residue thicknesses and resulting location within the features it is reasonable to conclude that each integration scheme and etch process will yield different results.

During the etching process, the photoresist is damaged – predominantly dehydrated and cross-linked. The photoactive resists used for different wavelengths of exposure do not show the same behavior [18]. For deep ultraviolet (DUV) photoresist, the researchers observed that degradation is more intense in the top layer where a cross-linked crust is formed. This damage is believed to be due to the reaction of the plasma etching process with the carbon backbone of the organic photoresist. Cross-linked resists are very difficult to remove with wet processing alone. Figure 10.4 shows a cross section of a via with polymer present on the side wall.

Specifically, integration requires successful removal of water from pores, the ability to remove residue from the deep trenches and vias, and the passivation of the surface to prevent corrosion. Overviews of the challenges of low-$\kappa$/Cu stripping and cleaning are outlined by Louis *et al.* [19] and Baklanov *et al.* [20]. The stripping and cleaning process must successfully achieve:

1. Removal photoresist (PR) and BARC (bottom antireflective coating) films.
2. Removal of organic residue, including fluorocarbon compounds.
3. Removal of metallic residues, such as copper oxides.
4. No bowing or other modification of the via and trench profile.
5. No change to the critical dimension of the via and trench feature.
6. No augmentation of the dielectric constant may occur.
7. No corrosion or removal of the metal layers.

Figure 10.5 outline some of the issues with dual damascene post-etch cleaning.

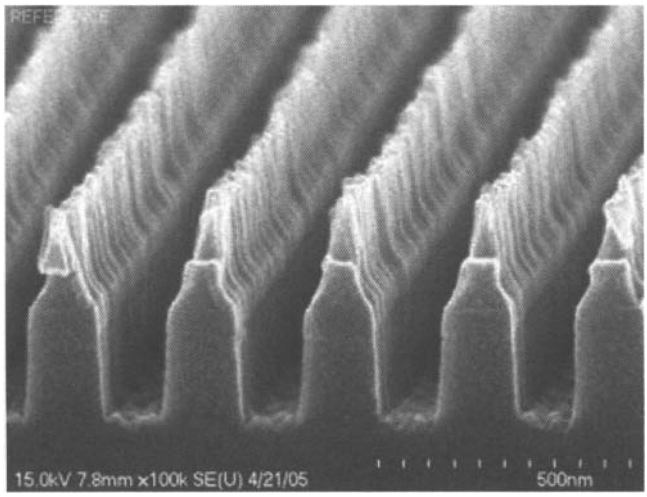



**Figure 10.4.** Cross section of a scanning electron microscope (SEM) image of post-etch residue on the top, sidewall, and bottom of a dual damascene via structure with $\kappa$ = ~2.2. Used with permission of the author.

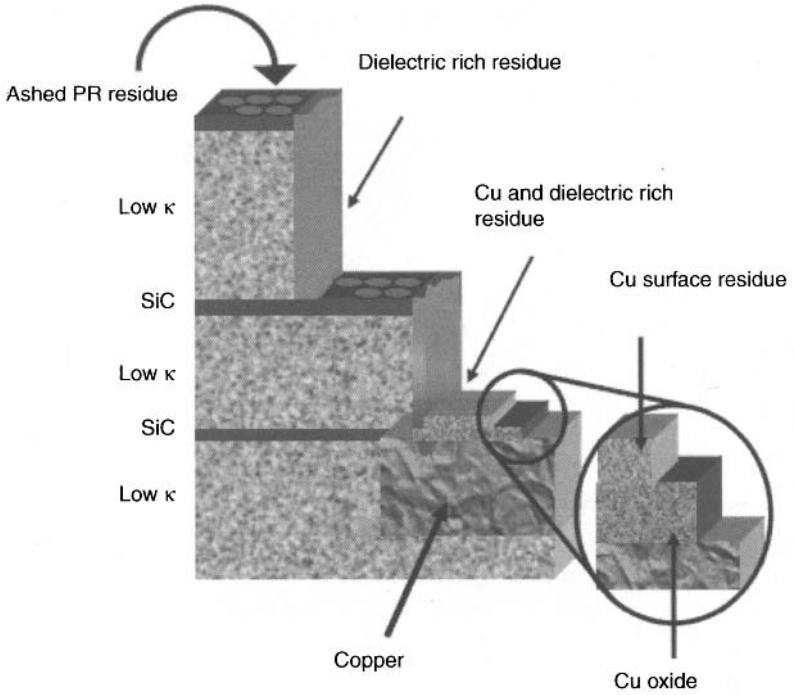



**Figure 10.5.** Schematic of the wafer surface after post-etch and strip cleaning showing issues related to cleaning [21]. Courtesy of DuPont/EKC Technology (2010).

Both plasma and wet processing are used to strip the photoresist, BARC, and remove the post-etch residue. Stripping and cleaning first by plasma then followed by wet cleaning has shown the best results [22]. Care must be taken to prevent damage to the sensitive low-κ material and oxidation of the copper during the cleaning process. As each successive generation of low-κ material is implemented, cleaning becomes more challenging. For current generation porous dielectrics, it is difficult to prevent removal of carbon from the CDO (Si-$CH_3$ groups) and densification of the film because these changes lead to an increase in the interlevel dielectric (ILD) constant.

Water must be completely removed after a wet cleaning process to prevent an increase of the dielectric constant and possible deposition problems due to outgassing that would cause long-term reliability problems [23]. The low-κ films that are hydrophobic before the stripping and cleaning process may become hydrophilic taking up $H_2O$ from the atmosphere, and thus, exhibiting an increased dielectric constant. Baking or annealing sometimes eliminates this problem; however, with porous low-κ materials, this may be a serious concern [24]. Annealing at too high of a temperature promotes the release of hydrophobic Si-$CH_3$ groups forming Si-OH groups that increases the dielectric constant and make the film more hydrophillic [25].

Copper is also affected by cleaning processes. Contamination may be present at the bottom of a via, and consequently, disrupt a low-resistivity contact between metal layers. Sputtering of Cu into the low-κ during photoresist stripping and residue removal may lead to undesirable leakage or, in the worse case, a short

between metal lines. Copper oxidation during stripping or cleaning can deleteriously increase the resistance within lines. A detailed outline of copper corrosion issues and the solutions to address these problems are discussed in Chapter 11.

### 10.2.1 Plasma Post-etch Stripping, Cleaning, Residue Removal, and Passivation

Plasma is used to strip the photoresist and clean the sidewall and bottom of polymeric residue. Both $O_2$ and $H_2$-based chemistries are used for stripping photoresist and removing residuel. Oxygen-based chemistries are preferred due to the faster rate of photoresist removal [24]; however, the $O_2$-based cleaning recipes can cause severe damage to the carbon-rich low-κ materials [26, 27], in some cases, densifying the film [28]. Oxygen plasmas have been shown to density the film, abstract C and create more Si-OH bonds, and absorb $H_2O$, all of which contribute to an increase in the dielectric constant [24, 26]. Additionally, with the formation of Si-OH bonds, the surface of the low-κ dielectric becomes more hydrophilic adsorbing $H_2O$ molecules that are generated during the stripping process [29]. The water molecules can be hydrogen bonded and physisorbed which accounts for the increase in dielectric constant when using an $O_2$-based plasma [30].

In the instances where $O_2$ plasmas may damage the low-κ material, $H_2$-based plasma recipes have shown promise [24, 31–33]. Some of these recipes were first developed for aluminum interconnect delineation cleaning. The addition of fluorine can effectively etch the sidewall and bottom polymer. When the dielectric etch-stop is a metal layer, the reducing chemistries sometimes include F-based chemistries, and may volatilize the metallic contamination or at least render the metal soluble in $H_2O$-based cleaning chemistries. The $O_2$-containing chemistry can oxidize the metal creating non-volatile products that may be insoluble in the subsequent wet cleaning solution. Water is sometimes used as an alternate plasma additive providing oxidizing capability although less than $O_2$ [34]. Inert gases, such as He or Ar, may be added in place of or in addition to $N_2$ [35, 36].

Hydrogen plasma pre-treatments prior to wet cleaning passivates the surface making the subsequent wet cleaning process less destructive to the low-κ material [33]. In $H_2$ plasma treatments the Si-$CH_3$ groups can be replaced with Si-H groups which are less hydrophilic than Si-OH groups but less hydrophobic than Si-$CH_3$ groups [37, 38], although this is not true for all $H_2$ plasma processes. Grill *et al.* showed that hydrogen plasma can significantly changed the bonding structure of CDO low-κ films and the substrate temperature was a key parameter in the changes in the films [39]. Tan *et al.* used XPS to investigate the contaminants deposited on the copper surfaces at the bottom of the trenches and on the dielectric sidewalls before and after stripping and cleaning. Significant Cu, C, F, and O-based contaminants were found on the copper at the trench bottoms and the sidewalls. Using a $N_2/H_2$ plasma process and a post-stripping wet process, the polymer and contaminants were removed [22]. Chang observed that copper diffusion is reduced when $H_2$ plasma passivation is used. The researchers suspected it was due to passivation of the surface preventing interaction with the Cu atoms and minimizing diffusion into the low-κ material (in this case methyl silsesquioxane – MSQ) [32].

Temperatures used to strip and clean the low-κ material can vary. High temperature quickly removes the photoresist and residue and may deter the condensation of $H_2O$ while low temperatures may limit the damage to the low-κ material due to excessive reaction with the dielectric material while the stripping and cleaning process is taking place. Han and coworkers have demonstrated that using a high temperature $H_2$/He stripping processes, high selectivity of MSQ low-κ films to photoresist have been obtained [40]. Biased plasma can provide kinetic bombardment (by ions) that has been found effective in removing residues on the sidewall, bottom, and the crust on top of the photoresist [24]. However, ion bombardment can sputter Cu or any other exposed metal.

Researchers at IMEC have shown that for a 30% porous film the amount of absorbed water can be as high as 15% of the film volume [41]. Figure 10.6 shows the water thermal desorption spectrum for MSQ low-κ; where the amount of water lost from the $O_2$ plasma-processed material is greater than the unprocessed material. Moisture adsorption can be monitored for a specific processing step through the use of $D_2O$ and Fourier transform infrared (FTIR) spectroscopy because the deuterium oxide and deuterated hydroxyls have distinctly different IR adsorptions than $H_2O$ and –OH. Vinogradova *et al.* showed that liquid and vapor $D_2O$ can penetrate $N_2/H_2$ plasma stripped CVD and spin-on low-κ films; however, oxygen stripped films do not show any significant $D_2O$ (and by extension moisture) adsorption [42].

Many plasma chemistries now exist for stripping photoresist, cleaning, and passivating low-κ materials; with modifications of the gas, temperature, and other

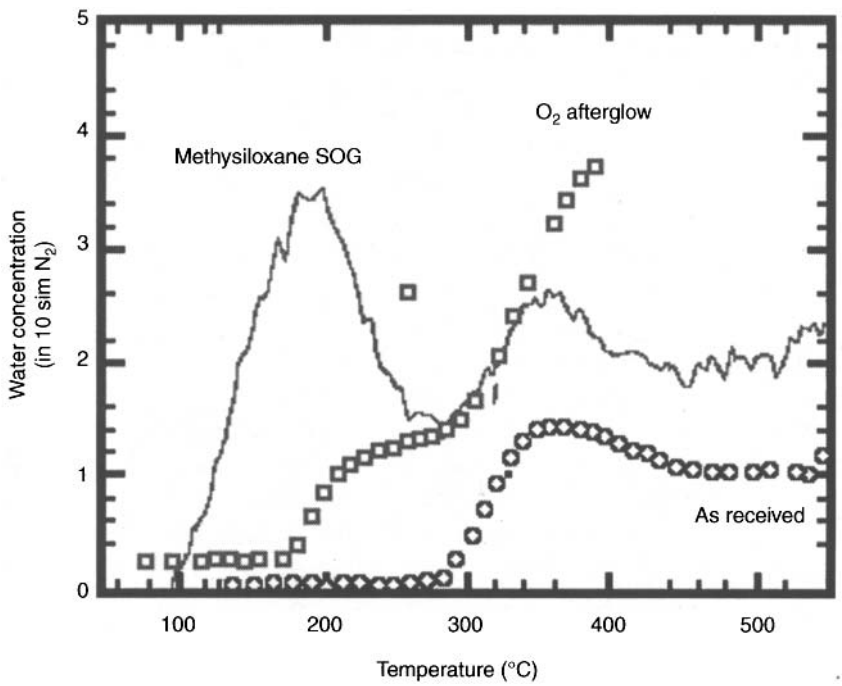



**Figure 10.6.** Water thermal desorption spectrum of untreated and $O_2$ plasma-treated films showing the water concentration [26]. The plasma treated films had significant water absorbed compared to the untreated SOG MSQ films. Reproduced with permission of ECS – The Electrochemical Society from Kondoh, E., Baklanov, M. R., Bender, H., and Maex, K., *Electrochemical and Solid State Letters.*

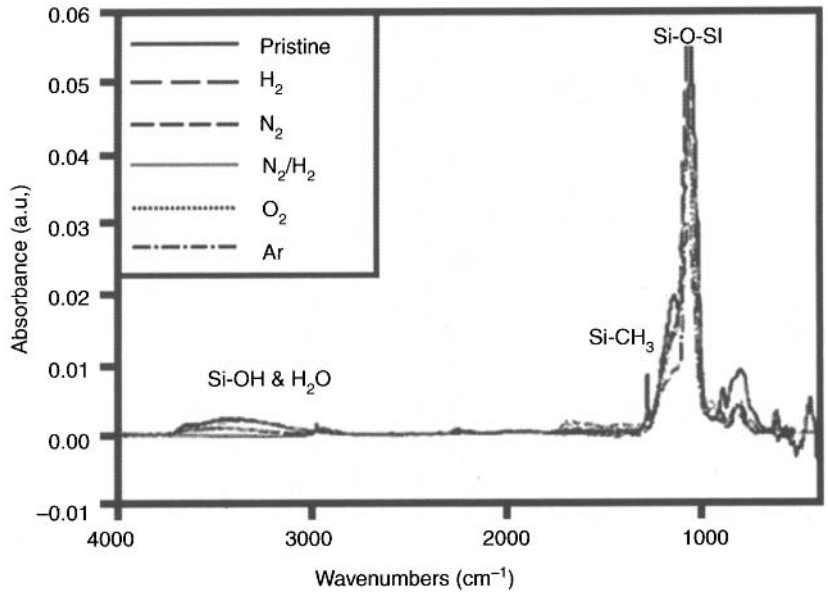



**Figure 10.7.** Fourier transfer infrared spectra of CDO low-κ film after the photoresist pattern has been stripped with various chemistries [38]. Argon has the highest affect on the Si-$CH_3$ bond, while $N_2$ or $O_2$ plasmas have the highest affect on the Si-O-Si bonds. Reprinted with permission from Bao, J., Shi, H., Liu, J., Huang, H., and Ho, P. S., Goodner, M. D., Moinpour, M., and Kloster, G. M., *Journal of Vacuum Science Technology*, B26(1):219. Copyright 2008, American Institute of Physics.

process conditions. Bao and researchers have attempted to explain the interactions of the CDO materials with various plasma gases [38]. They hypothesize that both neutral and charged species play a role in causing damage, and all gases, Ar, He $O_2$, $H_2$, $N_2$, and $NH_3$ caused some degree of damage whether by chemically removing the terminal groups (*i.e.* Si-$CH_3$ to Si-OH or Si-$NH_2$) or breaking bonds (*i.e.* Si-O-Si to Si-OH). Figure 10.7 shows the FTIR spectra of the various stripping chemistries and the effect on the Si-OH, Si-$CH_3$ and other bonds in CDO low-κ film. Note the loss of the –$CH_3$ moiety from Si and the creation of more Si-O-Si bonds increasing the dielectric constant and decreasing the hydrophilic nature of the low-κ material. Worsley *et al.* have shown that ion scattering on sidewalls and trench bottoms create sites that permit ions and radical species to modify low-κ through carbon removal and oxygen incorporation [36].

Removal of the photoresist after the etching process is sometimes performed *in situ* at the same time the etching chamber is cleaned of the built-up organic residue from the etching process. However, transfer of the wafer to an *ex situ* plasma strip system is typically performed for most layers in IC manufacturing. Savas, *et al.* shows results for stripping and cleaning photoresist and residue on low-κ dielectric material using an inductively coupled plasma (ICP) reactor [43]. The researchers believe that the process is efficient at stripping the photoresist without removing or significantly reacting with the organic components of the low-κ material due to the use of a low-pressure, $O_2$-based, ion-activated process. This is similar to what was observed by Worsley for Ar plasmas [36]. Savas *et al.* suggests the process exposes sidewalls to a higher ratio of ion flux than O radicals and reduces

the O diffusion into the low-κ material, thus, preventing removal of the C from the sidewalls. In addition the ion impact effectively seals the sidewalls which inhibit O diffusion into the low-κ [43]. Additional work on stripping low-κ materials in an ICP chamber using various gas mixtures of $N_2/O_2$, $O_2/H_2$, and $N_2/H_2$, was performed by Stucchi *et al.* [44] who found that gases had an effect on the via profile.

Using XPS, Oehrlein and his research team have observed that after $O_2$ plasma treatment the C-F bonds in the residue become Cu-F bonds indicating a loss of carbon, but not of fluorine [14]. They also note that copper oxidation occurs forming a $CuCO_3$ patina and both $Cu(OH)_2$ and CuO.

## 10.2.2 Wet Post-etch Cleaning and Residue Removal and Drying

The porous nature of low-κ dielectric films causes difficulties in wet cleaning and drying. Although plasma processing is used to strip the majority of the photoresist, a wet cleaning step is usually needed after the plasma step to remove residues that the plasma could not remove. Additionally, removal of liquid from the tiny pores is essential for maintaining the dielectric constant [45]. Since water has a dielectric constant of ~73, a small amount of water easily increases the dielectric constants of materials when they have a κ value of ~2. Removing the water from the dielectric is especially important for porous materials as the surface area is large and water could be adsorbed on the numerous hydrophilic sites. Consequently, drying is also important after the wet processing step.

Cracking has been reported on patterned films due to the cleaning solution [46] specifically because of moisture and aqueous solution chemistry. These topics are covered in Section 10.4.

Various types of wet cleaning processes are available to clean the *via* and trench structures – dilute HF (DHF), semi-aqueous solvent formulations, solvent formulations, acid or bases, and those with fluoride additions. This section will cover these cleaning chemicals.

### *10.2.2.1 Dilute Hydrofluoric Acid*

Dilute HF cleaning is one possible solution that can be used for low-κ and copper interconnects. Early in the development of copper processing, DHF was used to clean the metal interconnects within the $SiO_2$ dielectrics after plasma etching [47]. In this case, the post-etch polymer was removed by lift-off, and the CuO (but not $Cu_2O$) film was etched yielding good electrical contacts. This cleaning solution also can be used for cleaning BEOL structures when amines from the semi-aqueous solvent stripping formulation cause poisoning of vias [48]. The same was seen when nitrogen from the SiN barrier film was incorporated into the photoresist [49]. Since the introduction of Cu, DHF has been used due to the ability of HF to remove the residues that contain silicates [50]. However, HF also can remove the sidewall of the via or trench, causing undesirable widening of the feature if plasma etching damage occurs and a SiO-like layer is on the surface.

Dilute HF can remove the $CuO_x$ from the surface with selectivity to Cu [51] especially when de-aerated and at higher pH values (>8, using tetramethyl ammonium hydroxide). De-aeration of the DHF solution is critical when a CoWP or similar

capping barrier layer is used [52]. Galvanic corrosion can take place and, in some cases, it is severe enough to corrode the entire cobalt layer. Mistkawi *et al.* have shown the use of de-aerated DHF combined with $H_2O_2$ reduces corrosion rates by creating a CuO film [53]. Also the researchers found that the copper concentration in the cleaning solution is reduced. Figure 10.8 shows the residue before post-strip cleaning; the dendrite of copper corrosion and the energy-dispersive X-ray spectroscopy (EDS) spectra showing the residue composition.

### *10.2.2.2 Semi-aqueous and Solvent Cleaning*

Various classes of semi-aqueous formulations exist for copper/low-κ cleaning:

1. Fluoride-containing formulations.
2. Acidic aqueous formulations.
3. Semi-aqueous alkaline formulations.
4. Near-neutral aqueous formulations.

Chapter 5 thoroughly covers the various formulations used for cleaning and the evolution of the generation of these mixtures. These formulations are used specifically for cleaning Cu/low-κ via and trench features, in which there is a wide choice of formulations in which to choose to address specific cleaning needs. They are used for a variety of low-κ materials, but primarily CDO or SiCOH films such as deposited by PECVD or spun-on and copper with TaN barrier metal, for example.

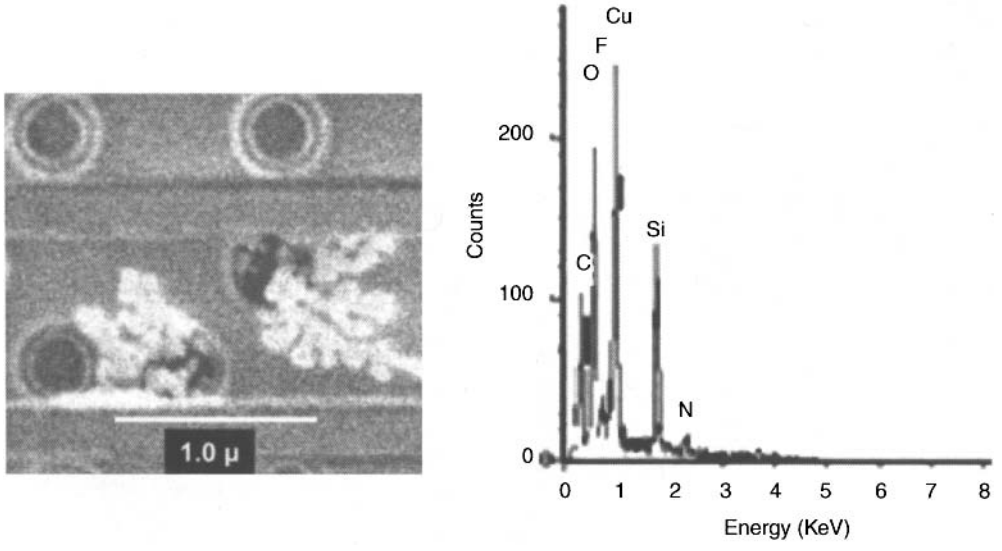



**Figure 10.8.** Cross-section SEM images of contamination on a low-κ *via* surface and the associated EDS image showing a high concentration of copper on the surface in addition to the carbon and fluorine from the post-etch polymeric residue [53]. Reproduced with permission of ECS – The Electrochemical Society from Mistkawi, N. G., Hussein, M. A., Ziomek-Moroz, M., and Rananavare, S. B., *Journal of the Electrochemical Society*.

### 10.2.2.3 *Fluoride-containing Aqueous Formulations*

One class of semi-aqueous formulations contains fluoride ions. This is an extension of dilute HF cleaning with additives to improve the process. These formulations are generally composed of a fluoride source, a polar solvent, water, a buffer, and possibly a corrosion inhibitor [54, 55]. Although the formulation removes residue well, it cannot remove photoresist or BARC. And in most cases, these cleaners were developed for aluminum, but were found to be acceptable for use with copper and low-κ materials. The cleaning performance can be adjusted with different pH ranges, with some fluoride-cleaning formulations being alkaline. These mixtures work well at room temperature and on single wafer tools.

### 10.2.2.4 *Acidic Aqueous Formulations*

Organic and inorganic acids have been used with some success. Some formulations are compatible with copper and low-κ materials – organo-silicate glass (OSG), hydrogen silsesquioxane (HSQ) or MSQ. Research has shown that acetic acid in combination with ozone can remove some types of photoresist [56]. At 22-nm features with a TaN/TiN metal hard mask (MHM) it may be possible to use a blend of UV, $O_3$, and solvent chemistries to remove photoresist.

### 10.2.2.5 *Semi-aqueous Alkaline Formulations*

The use of basic chemistries are specific for clean post-etch Cu residues in the presence of low-κ below 65 nm [57, 58]. The high content of alkalinity in the stripper solution often leads to the hydrolysis of HSQ films forming dangling bonds that can easily react with hydroxide ion ($OH^-$) in wet stripper solutions and form Si–OH bonds. The resultant HSQ film will tend to uptake water and consequently increase both the leakage current and dielectric constant [33]. Additionally, high pH chemistries can promote low-κ delamination, discussed further in Section 10.4.1.

Compared to plasma stripping, solvent-based stripping shows no carbon depletion and no significant increase in κ-value [41]. These semi-aqueous chemistries have shown good removal of residue with no copper corrosion, as shown in Figure 10.9.

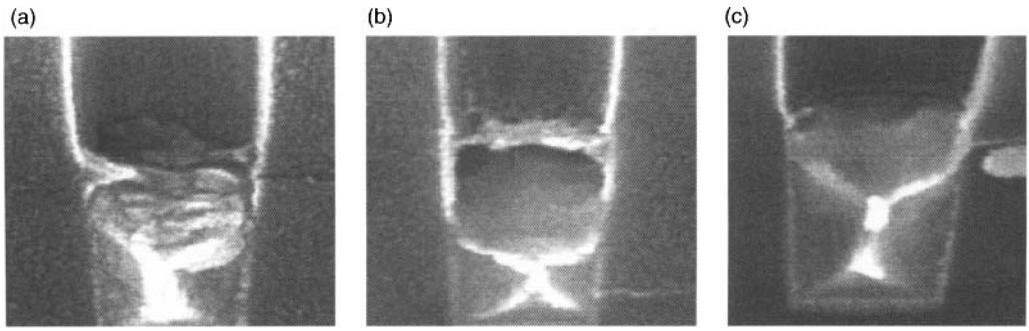



**Figure 10.9.** Cross-section SEM images of the bottom of a copper/low-κ *via* a) after etch and before stripping and cleaning showing post-etch polymer at the bottom and on the sidewalls of the *via*, b) after cleaning showing copper corrosion and article removal of the etch residue, and c) after cleaning with no copper corrosion and complete residue removal [21]. Courtesy of DuPont/EKC Technology (2010).

#### *10.2.2.6 Near-neutral Aqueous Formulations*

Due to the detrimental effects of the alkaline-based chemistry that has a tendency to impact the low-κ material integrity, and fluoride-based chemistries, that can etch the dielectric; a new class of cleaning formulations have been developed based on fluoride. These cleaning formulations use fluoride as the active ingredient, but augment the mixture to provide a near-neutral pH [59].

## 10.3 Pore Sealing and Plasma Damage Repair

Since the advent of porous low-κ dielectrics, issues with their porosity have hampered their integration into BEOL structures – limited mechanical strength, vulnerability to plasma damage, and moisture adsorption. As discussed in Section 10.1, scaling requires the dielectric constant of insulating materials within interconnect structures to decrease. Unless a new class of materials is discovered, the currently used SiCOH materials must include greater fractions of porosity to have the dielectric constants required by the ITRS [4]. Plasma etch processes can expose the pores within the low-κ permitting the intrusion of chemical moieties such as moisture and metal precursors into the low-κ bulk and introducing surface roughness to the feature. In addition to exposing pores, plasma processes can remove carbonaceous species from the dielectric and densify near surface regions leading to an increase in dielectric constant as described in the previous Section [29]. Section 10.2 described the impacts of different plasmas on porous low-κ films. It is worth repeating that the extent of carbon loss, the thickness of densified layer, and additional changes to a film vary with the plasma type, energy, and temperature as well as the specific chemical composition and structure of the low-κ.

### 10.3.1 Pore Sealing

Figure 10.1 details dual damascene processing of low-κ layers through final clean. The existence of pores within the low-κ effects its interactions with these processes. Figure 10.10 depicts the impact of the etch and strip/clean steps on the low-κ pore structure. The pore sizes and the via and trench widths in this figure have been drawn to a common scale – based on 2-nm pore diameters common in current porous low-κ films. The spacing of these pores and their diameters are commensurate with a 26 volume% porous structure. The widths of the etched features are not necessarily representative of a known device structure, but are used to depict the scale of the pores with respect to 32 and 22-nm technologies (Figure 10.10a and Figure 10.10b). In Figure 10.10c, the relative thickness of an ITRS-projected barrier layer is compared to the roughness exposed during etching. Smith *et al.* have shown that the inherent roughness of a plasma treated low-κ transfers to subsequent metal layers [60]; consequently, this roughness affects sidewall scattering in interconnect lines and can limit device performance.

Because plasma etching exposes low-κ pores and damages the near surface material, processes must be developed to seal these pores and to prevent intrusion

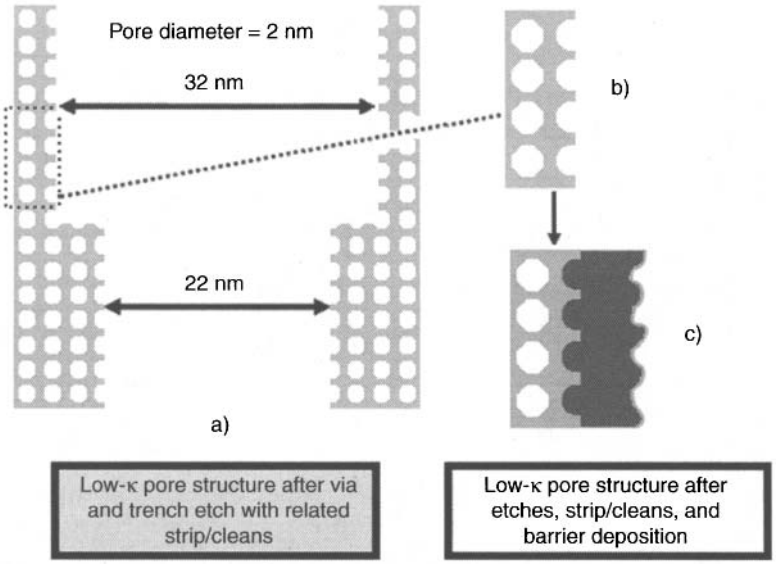

Pore diameter = 2 nm
32 nm
22 nm
a)
b)
c)
Low-κ pore structure after via and trench etch with related strip/cleans
Low-κ pore structure after etches, strip/cleans, and barrier deposition

**Figure 10.10.** A depiction of a porous low-κ structure a) after etch/strip/clean exposing pores, b) magnification of exposed surface roughness, and c) transfer of roughness to barrier layer. Note that pore size, via widths, and barrier thickness are to a common scale. Used with the permission of the author.

of deleterious species plus limit the roughness transfer to barrier and copper layers without significantly increasing the effective dielectric constant and affecting the barrier thickness. Several basic approaches have been reported including: plasma treatments; addition of thin sealing layers; chemical modifications of the etched low-κ; and graded porosity. Each of these processes will be described in this section.

### *10.3.1.1 Plasma Treatments*

In 2004, Abel and Maex reported the use of "minimum plasma process conditions" to seal the surface of several porous low-κ dielectric materials. These "reduced" plasma processes (He, Ar, and $N_2$) showed limited damage to the material. They noted that higher power/bias conditions were necessary to effectively seal films with lower dielectric constants and higher porosities [61]. Their results indicated that the film surface was both chemically and physically modified by the plasma forming a thin "$SiO_2$-like" layer. Also in 2004, Macchi *et al.* reported similar success with $N_2$ and He plasmas [62]. These efforts indicated that less chemically reactive plasma processes following aggressive etching plasmas could effectively close pores. Cui *et al.* and Ollier *et al.* employed reducing and oxidizing plasmas for pore sealing [63, 64]. In these efforts, researchers attempted to control the densification of the top layer of the low-κ. Densification of a low-κ material will increase its dielectric constant; however, this liability is balanced against sealing the film interior against chemical intrusion. Peng *et al.* used ammonia plasma to create a 10-nm

nonporous "skin" layer on the porous low-κ [65]. This skin layer was best formed at 300°C and showed improved resistance to Ta and Cu diffusion. Puyreneir *et al.* reported that $NH_3$ plasma treated low-κ films showed limited diffusion of ethanol vapor [66].

### *10.3.1.2 Thin Sealing Layers*

Perhaps most obvious method of pore sealing would be to deposit a very thin impermeable layer onto the porous low-κ. However, the film must have a dielectric constant that does not negatively impact the effective κ of the film either by its inherent κ or the film thickness. And the deposition method should not damage the underlying low-κ. One of the first methods described was "molecular caulking" using parylene films [67, 68]. These films were deposited using CVD; however, their thickness (5 nm) was as thick as the barrier layer and added a substantial burden on the interconnect width. Silicon oxycarbide and boron carbonitride layers were also shown to be potential pore sealing options [69, 70]. In addition, capping layers with compositions similar to the underlying low-κ ($SiO_2$, organosilanes) have been explored as pore sealing layers [71, 72]. In each of these cases, the sealing effectiveness against increases in dielectric constant must be considered. In recent work, atomic layer deposition (ALD) of a silica-based film has been shown to fill pores without penetrating into the low-κ [73]. This approach has promise because ALD can provide a very controlled thickness, and thus, not increase the feature width.

### *10.3.1.3 Graded Pores*

Intrusion of undesirable species would be severely limited if the low-κ composition had fewer or no pores at its surface. Chang *et al.* describe the development of gradient pore distributions created by electrophoresis using anionically charged polymeric hollow particles dispersed in a UV-curable monomer [74]. These negatively charged particles are attracted toward the anode, and the positions were fixed by UV curing. Creating a dense skin layer *in situ* could be an effective self sealing method; however, no conclusive evidence was provided to confirm effective sealing against moisture or other species.

### *10.3.1.4 Chemical Modification*

Sealing pores by chemically modifying a low-κ surface advantageously maintains via or trench dimensions. Plasmas remove carbon containing groups and create relatively reactive silanols throughout the damaged region. Silylating agents such as hexamethyldisilazane (HMDS) and trimethylchlorosilanes can react with silanols to form trimethylsilyls on the low-κ. Silylation can occur through liquid or vapor exposures, or through the silylating agent dissolved in supercritical carbon dioxide. The addition of trimethylsilyl groups repairs the inherent hydrophobicity of low-κ films, thus, limiting moisture adsorption. Although silylation of low-κ films was first used to repair plasma damage, two research groups showed that silylating a plasma damaged surface with HMDS, alkylchlorosilanes, and alkylalkoxysilanes can prevent water intrusion

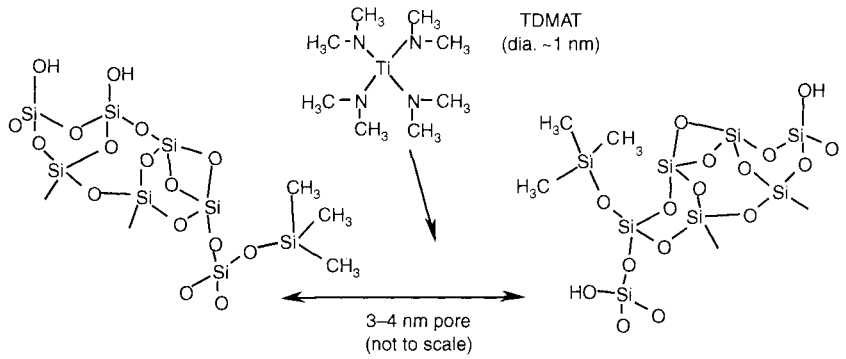



**Figure 10.11.** A depiction of how the addition of trimethylsilyls prevents the intrusion of TDMAT into a low-κ. Used by permission of the author.

in the bulk of the low-κ [75–77]. Furthermore, silylation can prevent the intrusion of metal precursors [76] and metallic species [78]. It has been suggested that trimethylsilyls and larger organic groups sterically hinder the intrusion of deleterious species. Figure 10.11 depicts how a silylated surface might preclude a titanium nitride precursor, tetra(dimethylamido) titanium (TDMAT), from penetrating into a porous low-κ.

More recently, Liu *et al.* reported improved low-κ/barrier interfaces after phenylalkoxysilane and phenylchlorosilane treatments [79]. Silylation methods have also been shown to "smooth" plasma roughened surfaces. Smith *et al.* used a variety of silylating agents to lower surface roughness of plasma damaged low-κ films [80]. Further, subsequent metal layers deposited on these smoothed surfaces were less rough than metal films deposited on non-silylated plasma treated low-κ layers [60].

Another means of chemical modification is to create chemistries on the damaged film surface that are removed during subsequent processing. One such method is the addition of a micellar solution to seal pores exposed at the bottom and sidewall surfaces of an etched low-κ [81]. The solutions are comprised of a combination surfactants including anionic, cationic, and zwitterionic. It is claimed that these micellar solutions can effectively clean etch residues from the porous structure. Another "sacrificial" chemical modification process involves that use of a polymeric porogen that penetrates into the low-κ pores thereby blocking subsequent chemical intrusion. A curing step will decompose the porogen and return the low-κ to its original state [82].

### *10.3.1.5 Determination of Pore Sealing Effectiveness*

There are a number of methods that have been used to study and measure pore sealing. Scanning electron microscopy with EDS has been used frequently to show metal intrusion into a low-κ [17]. Figure 10.12 shows the penetration of titanium moieties into a porous low-κ.

Energy-filtered transmission electron microscopy (EFTEM), scanning transmission electron microscopy (STEM)/Z-contrast high annular field dark field (HAADF), and electron energy loss spectroscopy (EELS) have been shown to

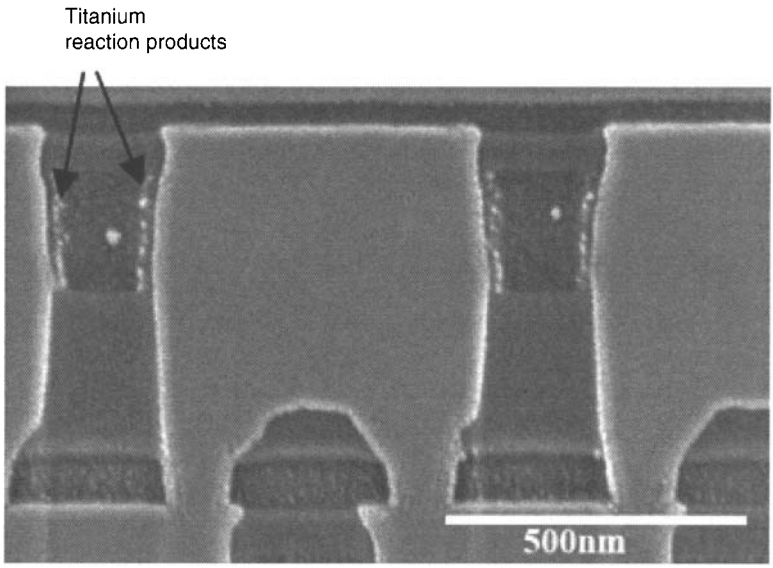



**Figure 10.12.** Titanium penetration into porous MSQ after reaction with TDMAT [76]. Used with the permission of the author.

resolve composition profiles down to a resolution of 1 nm [78]. Residual gas analysis attached to a physical vapor deposition (PVD) chamber has been reported to determine pore sealing effectiveness by measure moisture outgassing of the low-κ [83]. IMEC researchers have described the use of two electrical measurement methods; triangular voltage sweep and time-dependent dielectric breakdown to determine the presence of water and Cu in a dielectric [84]. Deuterium oxide and FTIR have been shown to effectively monitor moisture uptake in low-κ [39]. As previously noted in Section 10.2, D-O IR absorption peaks are found in different regions than H-O stretches; therefore can be used to observe long term changes in moisture content.

## 10.3.2 Plasma Damage Repair

Almost all porous low-κ films are hydrophobic and they can, unfortunately, absorb moisture [85]. This tendency is exacerbated if some of their intrinsic hydrophobicity is lost during plasma exposures. The dielectric constant of these films ($\kappa < 2.5$) is extremely sensitive to absorbed water ($\kappa = 73$); therefore, prevention of water uptake is critical to device performance and reliability. Plasma processes such as etching and photoresist stripping remove hydrophobic organic moieties to a significant depth (up to 40 nm) [75]. Many of the lost organic groups are replaced with silanols that are hydrophilic and enhance moisture adsorption. To prevent moisture uptake, low-κ films are exposed to silylating agents as discussed previously. Exposure can be through vapor and liquid phases or dissolved in supercritical $CO_2$. Ranges of silylating agents have been studied – a number were discussed in Section 10.3.1. The first reported use of a silylating agent used to repair plasma damage was by Chang *et al.* [86]. Subsequently, a number of researchers have

described different methods of restoring the dielectric constant to its value prior to plasma treatment [87–90]. The mechanism of dielectric repair is two-fold: first, removal of water or moisture from the bulk of the low-κ, and second, the replacement of silanols with some hydrophobic (less polar) moiety. The important of water removal is underscored by reports reduced dielectric constants after heating [85].

## 10.4 Post-chemical Mechanical Polishing Cleaning

Chemical mechanical planarization is used for planarizing and smoothing the surface of an array of IC devices by both chemical action and mechanical force. This is accomplished by the interaction of abrasives, chemistries and polishing pads on the wafer surface. After the CMP process there is a variety of contaminants on the wafer that must be removed, plus the copper surface but be passivated to prevent corrosion. A post-CMP cleaning step is critical to remove the contaminants and prevent corrosion.

### 10.4.1 Post-CMP Cleaning Defectivity Challenges

The number and nature of defects on a wafer surface following CMP are strongly dependent on the process and hardware conditions employed (*i.e.* hardware, pad, conditioning, downforce, head rotation), slurry type (selective/ non-selective, acidic/ alkaline, abrasive/abrasive free), hardness of the surface layer, and nature of the hard mask [91, 92]. Defectivity due to post-CMP cleaning can be classified with respect to the type [93], as depicted in Table 10.1 that shows an overview of defects attributed to inadequate post-CMP cleaning processes. Chemically-based defects and contaminants are identified as metallic particles, chemicals, and corrosion damage [94–98]. Figure 10.13 shows an overview of the copper CMP challenges facing the low-k/Cu dual damascene structure.

#### *10.4.1.1 Corrosion*

Galvanic corrosion may be triggered by the different electropotential of the closely packed metals and the aqueous media (slurry and cleaner) during both the CMP and post-CMP cleaning steps. Because of the intrinsic thermodynamic and chemical properties of each material (interconnects: Al, Cu, W; barrier and adhesion layer: Ta, Ti, TiN, TaN; dielectrics: polycrystalline silicon, TEOS, *etc.*), the choice of cleaning chemical becomes very important in preventing uncontrolled and unwanted device corrosion. For instance, for CMP processes with selectivity of Cu to the MHM, the choice of slurry pH is not trivial and the intermediary switch from an alkaline to an acidic blend during the polishing process is dictated by the electrochemical properties of the metals being polished. Generally, an acidic slurry is used to selectively polish Cu (since Cu is in its active region-anode) where the MHM is thermodynamically noble. This is followed by alkaline slurry to polish the metal hard mask. Under these conditions, Cu becomes the cathode, and therefore, is prevented from being etched.

**Table 10.1.** Common defects found in Cu/low-κ post-CMP cleaning processing. Adapted from [93], additions from the author. Adapted with permission of ECS – The Electrochemical Society from Yamada, Y., Konishi, N., Noguchi, J., and Jimbo, T., *The Journal of the Electrochemical Society.*

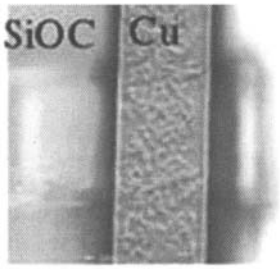
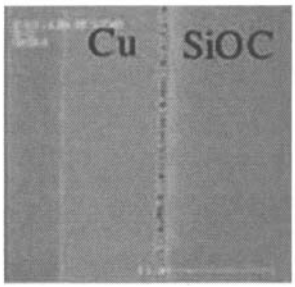
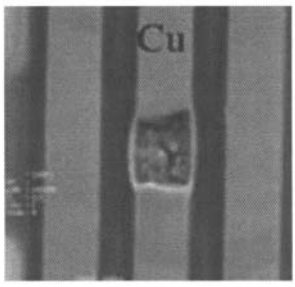
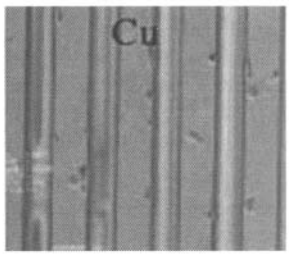
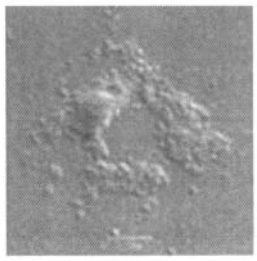
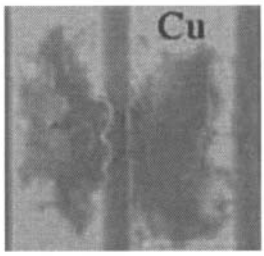
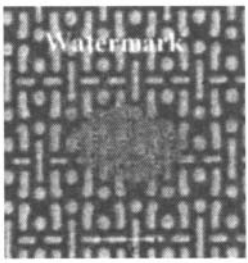
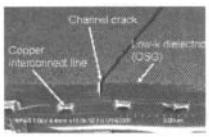
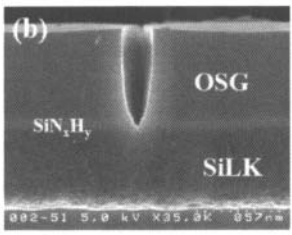
| Defect Type | Impact | Image |
|---|---|---|
| Corrosion: Roughened Surface | Reliability Issues, Poor Adhesion of Next Layer |   |
| Corrosion: Crevice Corrosion | Interconnect Opens, Reliability Issues |   |
| Corrosion: Copper Depletion | Interconnect Opens, Reliability Issues |   |
| Corrosion: Pitting | Interconnect Opens, Reliability Issues |   |
| Residual Slurry | Interconnect Opens, Poor Adhesion of Next Layer, Masking of Etching |  |

**Table 10.1. (cont.)** Common defects found in Cu/low-κ post-CMP cleaning processing. Adapted from [93], additions from the author. Adapted with permission of ECS – The Electrochemical Society from Yamada, Y., Konishi, N., Noguchi, J., and Jimbo, T., *The Journal of the Electrochemical Society.*

| Defect Type | Impact | Image |
|---|---|---|
| Organic Residues | Poor Adhesion of Next Layer, Masking of Etching |   |
| Metallic Contamination | Reliability Issues | |
| Watermarks | Poor Adhesion of Next Layer, Reliability Issues |   |
| Low-κ Crack Propagation | Interconnect Shorts, Reliability Issues | [99]   [100]   |
| Low-κ Delamination | Interconnect Shorts, Poor Adhesion of Next Layer, Reliability Issues | [101] |

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# 11

# Corrosion and Passivation of Copper

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*Abstract*

Copper corrosion has challenged the integrated circuit manufacturing process since its first use in dual Damascene structures in the 1990's. Copper oxides that form on the surface of metallic copper; $Cu_2O$ and CuO, must be removed to achieve good conductivity between the metal layers. Galvanic and electrogalvanic corrosion must be minimized. During processing, corrosion can occur for various reasons, electrogalvanic, by exposure to oxidizing solutions, or simply by exposure to air. Post-etch and post-chemical-mechanical planarization cleaning formulations have been developed to address these challenges, plus clean the post-etch residue from the features or remove the slurry on the wafer. Various corrosion inhibitors are used in cleaning formulations, including azole compounds, diols, and carboxylic acids. These compounds are soluble in aqueous solutions and inhibit corrosion by forming passive films. Once the corrosion is prevented, the compounds must be easily removed from the copper surface and leave little or no post-clean organic residue.

*Keywords:* copper corrosion, copper passivator, copper corrosion inhibitor, benzotriazole, triazole, diol, triol, carboxylic acid, dual damascene, post-CMP clean, post-etch via clean

## 11.1 Introduction and Overview

Copper corrosion and the protection or passivation of copper (Cu) surfaces during cleaning has been a challenge to the integrated circuit (IC) industry since the introduction of Damascene processing. Current back end of line (BEOL) processes use copper for electrical interconnects. To avoid confusion, the terms inhibitor and passivator will be used interchangeably throughout this chapter. A passivated surface is one that will not corrode further. All Cu inhibitors function by forming an insoluble passive film on the surface to prevent corrosion. The insolubility of this passive film is dependent on the solvent matrix. Incorporation of organic solvents in formulations can result in solubility of the passive film, reducing the corrosion inhibitor's effectiveness. Copper passivators are used in many semiconductor applications including some non-cleaning steps, such as chemical-mechanical planarization (CMP).

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Copper is difficult to pattern by dry etching; consequently, an in-lay or Damascene process is used to define Cu patterns on integrated circuits. The dielectric is etched and Cu is electrochemically deposited into the trenches and vias. Consequently, a CMP process is used to define the dielectric and metal pattern by removing excess Cu. Chapter 10 discusses the manufacturing challenges in the industry of copper corrosion and its detrimental impacts on devices. A challenge for passivating or protecting a Cu surface is that Cu has numerous crystallographic orientations (*i.e.* <111>, <101>) and not all Cu passivators equally protect all crystal orientations. A challenge for Cu corrosion inhibitors is to function effectively at various pH values to protect Cu during the cleaning and rinsing process. Another challenge for Cu corrosion inhibitors is to be able to remove the inhibitor in an efficient and cost effective manner in a process-appropriate time. Failure to remove an inhibitor can cause adhesion problems with subsequent material depositions and result in delamination of buried layers due to thermal decomposition of the inhibitor. Severe corrosion of Cu interconnects will result in opens and device failure. Partially corroded Cu lines can cause reliability issues with premature device failure due to current loads exceeding the capabilities of the remaining Cu.

## 11.2 Copper Corrosion

Technology to protect copper has existed for several centuries. Copper and Cu alloys have long been used in boiler, heating, and marine applications where corrosive environments exist. Consequently, a tremendous history for Cu protection is available; however, some techniques cannot be employed for semiconductor applications since these involve the use of other metal ions that are detrimental for semiconductor applications (*i.e.* Na, K, Mo). The use of Cu inhibitors for semiconductor manufacture spans about 15 years. Post-CMP formulations [1] and post-etch residue removal (PER) cleaners [2] designed for use on Cu were introduced in 1995.

### 11.2.1 Pourbaix and Stability Diagrams

The Pourbaix diagram depicts copper speciation over a range of pH and electrochemical potential; therefore, it can be used to determine conditions that promote corrosion. Figure 11.1 shows a Pourbaix diagram for Cu in water without any additional components [3, 4]. The diagram shows the thermodynamically stable species as a function of the surface potential (also referred to as open circuit potential or OCP) of the Cu and the pH of the water. The diagram represents an idealized environment in which the pH is varied from 0 to 20 without adding components.

For the Cu-$H_2O$ system, metallic copper is most stable at low oxidative potentials at all pH values. However, below a pH of about 5 and above a potential of about 0.4 V, $Cu^{+2}$ is the most stable species. In addition, regions exist in which $Cu_2O$ (cuprous oxide), Cu, $CuO_2^{-2}$, or $Cu(OH)_2$ are the stable species. There has been some discussion as to whether $Cu(OH)_2$ or hydrated cupric oxide (*i.e.* $CuO{\cdot}H_2O$)

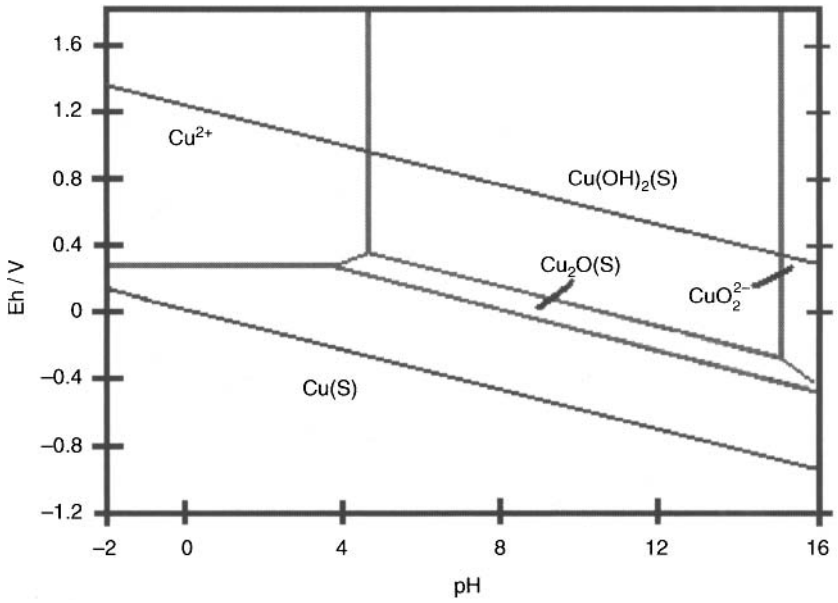



**Figure 11.1.** Pourbaix diagram for the Cu-$H_2O$ system [4]. Drawn with HSC Engineering software [5].

is the exact compound; nevertheless, the oxidation state of copper in either species would be $Cu^{+2}$.

If a Cu chelating or complexing agent is added to the solution, the surface potential for Cu will change; for example, the addition of benzotriazole (BTA), a copper passivating agent, is shown in Figure 11.2. The stability diagram for Cu-BTA-$H_2O$ is quite different than the Pourbaix diagram shown for Cu-$H_2O$. Note that this stability diagram shows a Cu-BTA complex formed at a wide range of pH values with Cu ion concentrations between $10^{-2}$ and $10^{-6}$ M, the BTA concentration is $10^{-4}$ M [6]. Adding other components to a Cu-$H_2O$ system will lead to new aqueous solutions and their corresponding stability diagrams. Other stability diagrams pertinent to copper cleaning are given in reference [7].

Benzotriazole is effective in preventing Cu from corroding by forming a passivation layer of Cu-BTA regardless of pH or $H_2O_2$ concentration in slurry [7, 8]. Many Cu CMP slurries are alkaline and use BTA to passivate Cu. Most barrier slurries are acidic and also contain BTA. Consequently, one aspect of a Cu corrosion inhibitor is to be effective at various pH values. The passivator species participating in film-forming (*i.e.* protonated, deprotonated, or neutral) will vary depending on pH and the quality of the film may depend on pH as well. Note that protonated BTA (which is best represented as $BTAH^+$) cannot interact directly with $Cu^+$. The film formed under acidic conditions is likely not homogenous since it must be composed of at least two BTA species. Under alkaline conditions, deprotonated BTA (best represented as $BTA^-$) can interact with $Cu^+$ and form a chemisorbed, homogeneous film.

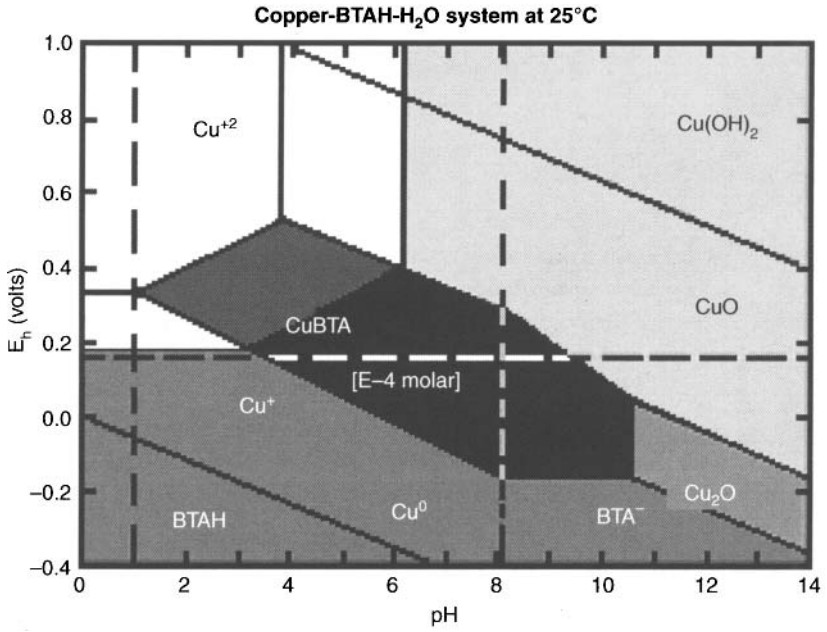



**Figure 11.2.** Stability diagram for the Cu-BTA-$H_2O$ system. Adapted from [6]. Reproduced with permission of ECS – The Electrochemical Society from Tromans, D. J. J., *Journal of the Electrochemical Society*.

Pourbaix and stability diagrams offer guidance when designing a post-CMP or post-etch cleaner; however, they are based solely on thermodynamics and provide no information on kinetics. For example, immersion time in a BTA solution is important, especially at low inhibitor concentrations, to form the protective film [9]. Software is available to calculate stability and Pourbaix diagrams for aqueous and semi-aqueous media which can be useful when describing corrosion in most post-CMP and some post-etch cleaning formulations [5, 10]. When calculations of the stability diagrams for semi-aqueous post-etch cleaners are compared to typical Pourbaix diagrams, there usually is a significant difference observed [11]. Such diagrams are not fool proof because insoluble species can occur due to complexes with components used in semi-aqueous cleaning formulations (*i.e.* Cu-fluoride, Cu-oxalate, Cu-gallate) leading to stable species in pH and potential regions where the Cu-$H_2O$ Pourbaix diagram indicates soluble species occur. Likewise, soluble Cu complexes can occur in semi-aqueous solutions (*i.e.* catechol-Cu, Cu-aminoethanol) leading to corrosion in pH and potential regions that are predicted to be stable in a Pourbaix diagram.

To describe the behavior of cleaning solutions, stability diagrams must be supplemented by measured etch rates and consequent inhibition efficiencies. Because Pourbaix or stability diagrams are based on thermodynamics, kinetic information is necessary to augment this information. In other words, thermodynamics does not predict whether a water soluble species will dissolve in femtoseconds or eons; therefore, etch rates are needed to predict corrosion rates and inhibitor deposition

rates are needed to determine whether film formation occurs fast enough to protect Cu.

## 11.2.2 Copper Corrosion and Oxidation

### *11.2.2.1 Oxidation and Corrosion with Respect to pH*

It is generally known that when Cu is in the presence of an oxidizer, it sequentially oxidizes from $Cu^0$ to $Cu^+$ to $Cu^{+2}$. Copper pennies can be observed to have two different colors – the brighter ones have a cuprous oxide ($Cu_2O$) film and the darker ones have a cupric oxide (CuO) film on their surface. Immersing a bright penny into 5 wt% $H_2O_2$ solution will turn it dark. Likewise, immersing either color penny in a dilute acidic solution (*i.e.* citric acid, oxalic acid, hydrofluoric acid) will result in dissolution of both oxides which will expose a very reflective $Cu^0$ surface. Immersing a penny containing both $Cu_2O$ and CuO in dilute alkaline solutions (*i.e.* $NH_3$, TMAH – tetramethyl ammonium hydroxide) will result in rapid dissolution of the cupric oxide while the cuprous oxide will dissolve more slowly. On the corresponding Cu-$H_2O$ Pourbaix diagram, Figure 11.1, a stable $Cu_2O$ region is observed in which the surface potential and pH solution range from 0 to –0.3 V and 8 to14, respectively.

Researchers have attempted to explain the formation of copper oxides in an aqueous-based solution. They have realized the formation is very complex, based on the pH, the electro-potential of the solutions, and the additives to suppress oxidation. Not only is the morphology complex, but the understanding of the film's passivation and the oxygen diffusion to create these films is important. Feng *et al.* did a thorough analysis of the formation of copper films [12]. They found that different mechanisms of copper corrosion occurred at various pH and also the morphology of the films formed were different. Although the conditions were not exactly the same that would be encountered during IC manufacturing, for example, there was no oxygen control in the water; it is a good indication of the surface states that could be encountered during the cleaning process at various pH values. A summary of Feng's work is shown in Table 11.1. Predominate and minor copper species are indicated along with their structure and hardness.

**Table 11.1.** Selected physical properties of Cu and oxidized Cu species.

| pH range | Species | $CuO_x$ Properties | Hardness (GPa) |
|---|---|---|---|
| 1–2 | Cu | | 1.7 (Cu) |
| 3 | $Cu_2O$ Cu CuO (minor) | Porous | |
| 4–6 | $Cu_2O$ CuO (minor) | Cubic | 4 |
| 6–9 | $Cu_2O$ CuO | | |
| 10 | $Cu_2O$ Cu | Thin, compact | 9 |
| 12–13 | CuO | Monoclinic | |

Feng assessed:

1. pH = 3, corrosion is predominately controlled by diffusion.
2. pH = 4–5, formation of cubic $Cu_2O$ provides a diffusion barrier to copper dissolution.
3. pH = 6–9, $Cu_2O$ is protective, diffusion through this film is the rate-determining step.
4. pH = 10, a thin, hard $Cu_2O$ film is formed leading to spontaneous passivation.
5. pH = 12–13, the surface is covered with a protective monoclinic CuO layer.

Mitikoš *et al.* found that once $Cu_2O$, is formed, it acts as a barrier layer, that inhibits the reduction of Cu(ll), for example when BTA is applied [9].

### *11.2.2.2 Galvanic and Photo-induced Corrosion*

In IC manufacturing, copper is always in the presence of another metal, in most cases a TaN or Ta/TaN barrier, or for newer generation devices, potentially a Co or Ru barrier [13], as shown in Chapter 10. Galvanic corrosion can take place in the presence of two dissimilar metals; consequently, pH, oxygen concentration, and temperature all play a role in the corrosion kinetics. Additionally, the presence of light can lead to photo-induced corrosion [14] and in many cases, equipment suppliers have intentionally designed equipment to process wafers in the dark. Photo-induced corrosion is most likely seen on devices where the presence of p/n junctions in which the corroded lines reside can act as photo-generators in the presence of light [14–16], creating a galvanic cell, as shown in Figure 11.3.

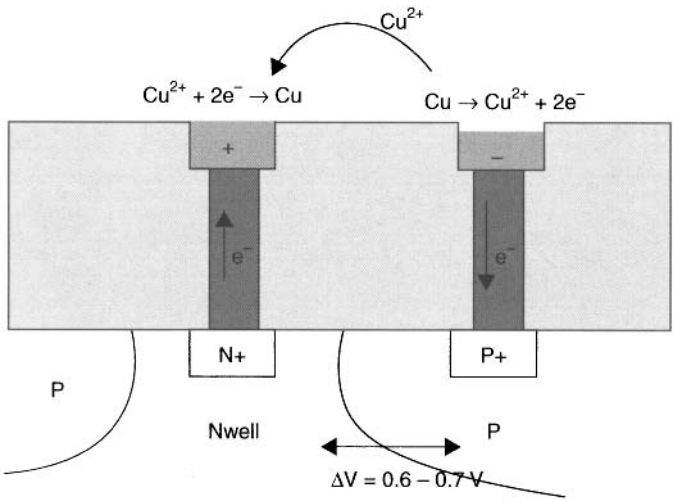



**Figure 11.3.** Copper ion migration from different implanted area, showing pathway for electrogalvanic corrosion [16]. Reproduced with permission of ECS – The Electrochemical Society from Gabrielli, C., Ostermann, E., Perrot, H., and Mége, S., *Proceedings of Cleaning Technology in Semiconductor Manufacturing VIII.*

Dissolved oxygen is typically the cause of metallic corrosion during wet processing [16]. In nearly all cases, dissolved $O_2$ is the oxidizer unless galvanic or electrogalvanic corrosion conditions occur. The two dissolution reactions of copper under electrically neutral conditions are:

$$Cu(s)+2H^{+}(aq)\rightarrow Cu^{+2}(aq)+H_2(g) \qquad \Delta G^{O}=15.53\ \text{kcal/mole} \qquad (11.1)$$

$$Cu(s) + 2H^{+}(aq) + \tfrac{1}{2}O_2(g) \rightarrow Cu^{+2}(aq) + H_2O \qquad \Delta G^{O} = -41.16\ \text{kcal/mole} \qquad (11.2)$$

Mistkawi *et al.* have shown that in acidic solutions the rate of copper dissolution is thus strongly dependent on the oxygen concentration. Copper oxidation from Cu to $Cu^{+}$ is favorable in the presence of oxygen compared to when an oxidizing agent, such as $H_2O_2$, is present, then $Cu^{+2}$ is favorable [17]. Therefore, under these conditions, the dissolution of copper is only thermodynamically favored in the presence of oxygen [18].

There are fundamental methods that can protect metals during semiconductor cleaning:

1. Lowering the dissolved oxygen concentration in the solution using an oxygen scavenger.
2. Forming an insoluble or passive film on the metal surface.

Little data exists indicating that $O_2$ scavengers are effective for protecting Cu. Gabrielli and researchers have shown that oxalic acid in both aerated and deaerated solutions lead to different electrochemical behavior of the reduction of copper [16, 19]. Oxalic acid is both a reducing agent and a chelating agent, and behaves like an oxygen scavenger. Oxygen scavengers are typically reducing agents and easily oxidized. Also, the pH determines their effectiveness due to most of these compounds having a carboxylic acid (-COOH) or hydroxyl (-OH) moiety in their molecular structure (further discussion is found in Section 11.3.1). Consequently, these species readily react with dissolved oxygen in solution and lower its concentration. Flake and coworkers have shown oxygen concentrations are reduced by more than 60% at the Cu-nitride interface and reduced below detectable limits in the bulk nitride layer when BTA is used in the post-CMP cleans, due to film formation and not oxygen scavenging. [15].

All effective Cu corrosion inhibitors form insoluble films on the Cu surface, by interacting with $Cu^{+}$, and prevent further oxidation and dissolution [11]. As will be seen later, one of the most widely used oxygen scavengers, catechol, accelerates Cu corrosion in alkaline semi-aqueous formulations. An explanation for this observation is that the Cu-catechol chelate is solvent or water soluble. Chelating agents form multiple bonds with metal ions. Chelate is Latin for "claw". A well known chelating agent, banned from use in IC fabs, is ethylenediamine tetraacetic acid (EDTA) that is capable of forming four bonds with metal ions.

Additionally, corrosion can be accelerated by other factors. As previously discussed, having two metals with dissimilar oxidation potentials in contact can result in galvanic corrosion. There is a junction potential due to the different oxidation potentials that can drive corrosion. Charging of the metal coupon or

wafer alters the surface potential and thus the propensity for corrosion. If wafers are charged during a previous process, the altered surface potential for Cu during a subsequent cleaning step could promote corrosion, as seen in the previous Pourbaix and stability diagrams. This is called electrogalvanic corrosion (EGC). For example, if a solution has a near neutral pH and a surface potential of −0.5 V, $Cu^0$ would be stable. However, if the wafer has been charged to +2 V, $Cu^0$ is not the stable species and the exposed copper oxidizes to $Cu^{+2}$. Consequently, wafer charging during processing and the persistence of this charge can lead to EGC problems [20–22]. If the charging is not uniform, and it rarely is, then the EGC can vary across the wafer. Optimization of upstream processes with regards to wafer charging has resulted in elimination of EGC. Matz and co-workers have also observed EGC issues in Cu patterns and have altered the pH of the rinse water to minimize the problem [23]. As seen in previous stability diagrams, adjusting the pH or surface potential can move the reaction conditions to a region where the metal is stable or it is oxidized. Lowering resistance of the copper by having reduced copper oxides at the copper-copper interface is also beneficial for via chain resistance [15].

#### *11.2.2.3 Examples of Corrosion – Post-etch and Post-CMP*

Copper corrosion can be observed in IC manufacturing at various levels, such as dual Damascene vias, and post-CMP lines, as shown in Figure 11.4. Figure 11.4a and b show corrosion occurring at the bottom of the via, the void in Figure 11.4c and the dendrite in Figure 11.4d are commonly formed due to electrogalvanic corrosion [24].

### 11.2.3 Corrosion Inhibitor Efficiency

The corrosion inhibitor efficiency, $\Gamma$, in %, is defined as:

$$= 100\% \times \left(1 - \frac{ER}{ER_0}\right) \tag{11.3}$$

where $ER$ is the etch rate with the inhibitor and $ER_0$ is the etch rate without the inhibitor, [11]. The typical values of inhibitor efficiency range from 0% (no effect of the inhibitor) to 100% (a perfect inhibitor). In some cases, the efficiency can also be negative (the "inhibitor" acts as an accelerator and promotes etching). It is also necessary to specify the solvent matrix when stating the inhibitor efficiency of a particular corrosion inhibitor. An inhibitor with 100% efficiency forms an insoluble film. An accelerant forms a soluble film. Degrees of solubility result in efficiencies that vary from 0 to 100%. Consequently, inhibitor efficiency will vary with the solvent matrix used in the cleaner. Lastly, it is necessary to specify how the etch rates were determined since the method used can influence the results. As an example, static etch rates are typically significantly lower than etch rates determined with agitation. It is best to determine etch rates using conditions that mimic real process conditions.

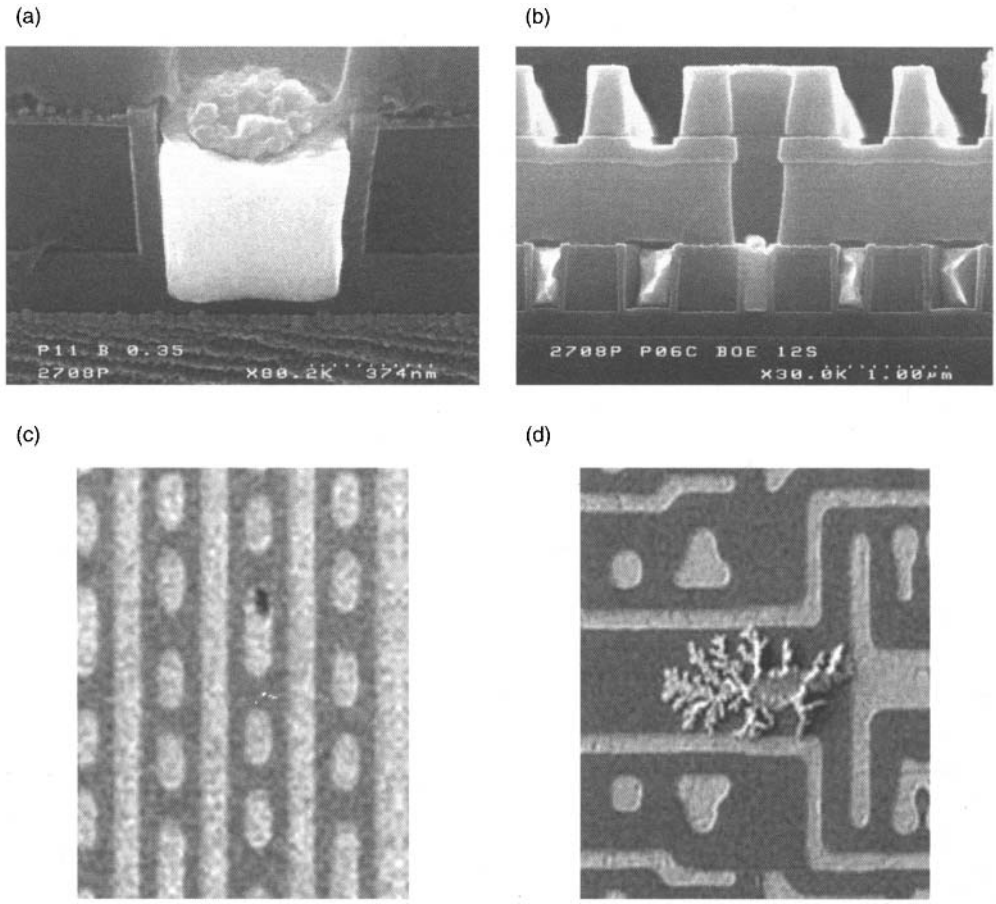



**Figure 11.4.** Examples of copper corrosion (a) and (b) dual Damascene post-via etch [25], (c) post-copper CMP void [24], and (d) post-copper CMP dendrite [24]. (c) and (d) Reproduced with permission of ECS – The Electrochemical Society from Petitdidier, S. Mellier, M., Guiheux, D., and Juhel, M, *ECS Transactions*.

## 11.3 Copper Corrosion Inhibitors

There are numerous Cu corrosion inhibitors used in various industries (*i.e.* marine, boiler, and automotive), but many are not applicable for semiconductor applications for a variety of reasons. A long list of Cu corrosion inhibitors can be found in literature from Drew Marine [26] and reviews are given in references [27, 28]. This chapter will only focus on those applicable to IC manufacturing applications – in particular Cu corrosion inhibitors found in various commercial products. Because IC manufacturing has stringent requirements, they must be available in high purity without significant trace metal contamination, provide a high degree of Cu protection at a reasonable concentration, possess sufficient solubility in the cleaner solvent matrix, and be available at a reasonable cost.

Typical Cu corrosion inhibitors for IC applications including azoles, diols, carboxylic acids, and mercaptans will be discussed with respect to their strengths and weaknesses. Inhibitor performance is strongly dependent on the solvent used, the

solvent concentration, and co-solvent additions. It is very important when discussing corrosion inhibitor efficiency to specify not only the method used to generate etch rate data, but also the solvent matrix tested.

Research has shown there is a strong dependence of the corrosion inhibition efficiency on the formulation matrix including the nature of the chemical (inorganic *vs.* organic acid) and the concentration, in addition to the process parameters such as agitation speed and temperature [29–31]. Ernur also investigated the galvanic corrosion of Cu features and noted that the integrity of Cu features could be affected by the barrier metal (Ti, Ta, W) and Cu line width for both isolated and semi-dense areas.

These dependencies partly explain why there are so many choices for Cu corrosion inhibitors. Some are ineffective in certain solvent matrices because they form a soluble film.

### 11.3.1 Azole Corrosion Inhibitors

Many nitrogen-containing cyclic molecules have the ability to inhibit Cu corrosion. Studies have included corrosion inhibition with respect to their electronic properties – because the nitrogen atoms, offer electron pairs to the unoccupied atomic orbital [32, 33]. The azoles described in this section are aromatic indicating they have delocalized electrons that may participate in bonding with other molecules or atoms. The interaction is with $Cu^{+}$ through the non-bonding electrons on the nitrogen atoms. The most commonly encountered azoles are shown in Table 11.2. Each azole will be discussed with respect to their effectiveness, attributes, and drawbacks for use in Cu cleaning solutions in a variety of aqueous and semi-aqueous solvent matrices.

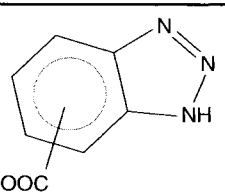
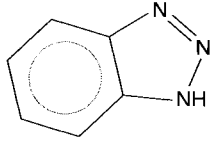
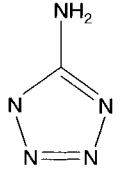
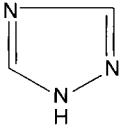
#### *11.3.1.1 Benzotriazole*

Benzotriazole (BTA), is most likely, the best known and most widely used Cu corrosion inhibitor within the semiconductor industry and can be found in many Cu slurries, Cu passivating rinse baths, BEOL post-etch cleaners, and resist developers. Use of BTA for copper passivation can be traced back to the 1960's and Cotton's pioneering work [32, 34]. Extensive literature can be found on the Cu-BTA passivation, too numerous to include in this chapter.

Benzotriazole can form passivating films at both low and high pH since it can act as an acid by donating a proton from the protonated nitrogen or as a base by accepting a proton on one of the unprotonated nitrogens. The passivating film formed at pH $\leq$ 7 tends to be thick, non-uniform in thickness, precipitated, and physisorbed [9]. At high pH (*e.g.* pH > 7), the films tend to be thinner, more uniform in thickness, chemisorbed, and more protective [8, 35–40]. Additionally, BTA has been shown to improve organic residue removal during resist development or BEOL stripping [1] and BTA prevents dissolution of the copper in recessed areas during the CMP process [41].

High inhibition can be achieved at fairly low BTA concentrations (~ 0.02%). However, BTA complexes are sparingly soluble in aqueous media over the entire pH range (alkaline, neutral, and acidic) which is a technical hurdle since remaining

**Table 11.2.** Azole corrosion inhibiting agents.

| Azole inhibitor | | Structure | Strengths | Weaknesses |
|---|---|---|---|---|
| BTA | Benzotriazole |  | BTA can donate a proton in alkaline solutions or accept a proton in acidic solutions. Readily available and relatively inexpensive. | Difficult to remove. Thermally decomposes into numerous products. Creates a hydrophobic Cu surface causing water marks. Does not protect all Cu crystallographic orientations. |
| CBTA | Mixture of 4- and 5- carboxybenzotriazole |  | Like BTA, it can accept or donate a proton, depending on the pH of the solution. CBTA has a carboxylic acid group which can also provide corrosion inhibition. | Expensive and not readily available. Results in a hydrophobic Cu surface leading to water marks after rinsing. Does not protect all Cu crystallographic orientations. |
| 5-ATA | 5-Aminotetrazole |  | Cu corrosion inhibitor has found use in slurries and some BEOL post-etch cleaners. 5-ATA can act as both an acid, by donating a proton, or a base, by accepting a proton. Results in a hydrophilic surface. | Expensive and not readily available. Does not protect all Cu crystallographic orientations. |
| TAZ | 1,2,4-triazole |  | Found in BEOL post-etch cleaners as well as Cu post-CMP cleaners. Like BTA, CBTA, and 5-ATA, TAZ can also act as an acid or a base, depending on the solution pH. Results in hydrophilic Cu surface. Protects all Cu crystallographic orientations. Easily removed, compared to BTA. Sublimes at reasonable temperatures. | Expensive. High purity product is difficult to obtain. |

carbon-based impurities on Cu devices may lead to serious electrical and integration failures (*i.e.* tool contamination, adhesion issues, increased line resistance) such as described by Yamada *et al.* [42].

The influence of solution pH and the film formation on Cu for several triazoles will be examined in more detail.

#### *11.3.1.2 Carboxybenzotriazol*

Another Cu corrosion inhibitor found in a widely used, commercially successful BEOL post-etch cleaner is carboxybenzotriazole, CBTA, which is related to BTA [40]. The commercially available and less expensive product is a mixture of the 4- and 5-carboxy isomers. Carboxybenzotriazole has shown the ability to protect both Cu and Al in acidic, water, and dimethyl acetamide- (DMAC) containing solvent matrices. However, when used in a solvent matrix of water and 2-aminoethanol at high pH, CBTA does not provide protection for all Cu crystallographic orientations and yields a hydrophobic surface resulting in watermarks and rinsing problems. As with catechol, this is an example of how a corrosion inhibitor in one solvent matrix can perform brilliantly and fail in a different solvent matrix.

#### *11.3.1.3 5-aminotetrazole*

Another azole that can be used in Cu slurry [43], CMP corrosion inhibitor [44], and BEOL post-etch cleaners is 5-aminotetrazole (5-ATA). Similar to the azoles discussed previously, it can act either as an acid or a base depending on the pH of the solvent matrix. There is no published data detailing the film formation characteristics of 5-ATA; however, it is reasonable to assume it has properties similar to that for 1,2,4-triazole (TAZ). 5-ATA in an alkaline test solvent matrix did not provide Cu protection for all crystallographic orientations; however, it did provide a hydrophilic Cu surface resulting in elimination of watermarks which could explain the molecular orientation on the Cu surface. The benzo-containing molecules (*i.e.* BTA and CBTA) appear to have the benzene group above the Cu surface that results in a hydrophobic surface after treatment [45, 46]. Both BTA and CBTA have low water solubility; however, both 5-ATA and TAZ have significantly higher water solubility because they do not have a hydrophobic benzene group. The actual orientation of either TAZ or 5-ATA on the Cu surface is not yet known.

#### *11.3.1.4 1,2,4-triazole*

1,2,4-triazole is used for Cu protection in commercially available formulations [47] that are used as either a post-CMP cleaner or as a buff solution after dilution with water. TAZ has been shown to protect all Cu crystallographic orientations and provide a hydrophilic surface after treatment eliminating watermarks. Researchers at IBM have also shown TAZ to form complexes with Cu oxide films and dramatically reduce the copper dissolution rate [48]. They have shown that TAZ has some unique characteristics with respect to the effect of pH on the azole species present, and the effect on film formation, plus important information on the ability to remove the passivator film.

### 11.3.1.5 *Influence of Solution pH*

Azole compounds have unique properties in that they can act as either an acid or a base depending on the pH of the solution – they can either donate a proton or accept a proton. Figure 11.5 contains a plot of the relevant species of BTA (*i.e.* $BTAH^+$, BTA, or $BTA^-$) as a function of pH showing the $pK_a$ based on how easily the base dissociates.

$$BTAH_2^+ \underset{-H^+}{\overset{+H^+}{\rightleftharpoons}} BTAH \underset{+H^+}{\overset{-H^+}{\rightleftharpoons}} BTA^- \tag{11.4}$$

The $pK_a$ is defined as:

$$\frac{K_a = [H^+][B^-]}{[HB]} \tag{11.5}$$

$$pK_a = pH + \log\left(\frac{[HB]}{B^-}\right) \tag{11.6}$$

At the pH that is numerically equal to the $pK_a$, the concentration of the acid and the conjugate base are equal.

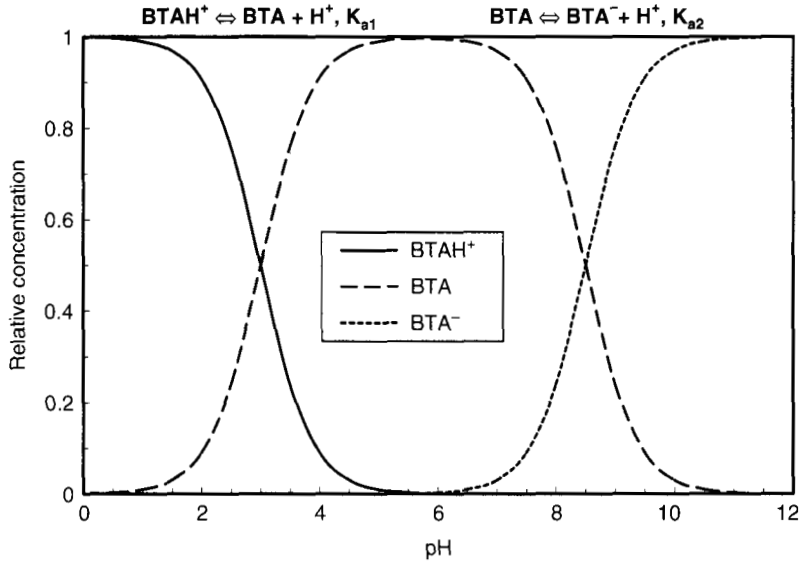



**Figure 11.5.** Benzotriazole species versus pH. The dominate species at pH values below $pK_{a1}$ is $BTAH^+$, above $pK_{a2}$, $BTA^-$ is the dominate species, and between $pK_{a1}$ and $pK_{a2}$, BTA is the dominate species. Used with permission from the author.

The interaction of BTA species with metals is through the non-bonding electrons on the nitrogen and open *d*-orbitals of the metal ion. For example, the interaction between $BTAH^+$ and $Cu^+$ is not obvious; however, the interaction between $BTA^-$ and $Cu^+$ is similar to other chemical interactions between positive and negative ions.

At low pH BTA forms thick, precipitated, physisorbed, and non-uniform films on Cu [8, 35–38, 40]. At high pH, BTA forms thinner, chemisorbed, uniform, and more protective passivating films on Cu [39]. Figure 11.6 contains data for BTA deposition on Cu at a pH = 5 and 11 [46] obtained in an electrochemical cell using a quartz microbalance (QMB) [49]. The film deposition at pH = 11 is faster and the resultant film is 25% thinner than that deposited at pH = 5. The deposition curve for BTA deposited at low pH suggests at least two mechanisms based on the break in the curve near 1 minute. The deposition curve for BTA in alkaline solutions indicates a single mechanism asymptotically approaching a limiting value of about 50 Å under the conditions tested.

Benzotriazole has several obvious drawbacks: it does not protect all crystallographic orientations of Cu [50]; it produces a hydrophobic Cu surface causing rinsing problems; and it usually forms overly thick films when deposited at low pH [51] making removal difficult. Carboxybenzotriazole also produces a hydrophobic surface and does not protect all Cu crystallographic orientations. The data for 5-ATA appears better – the contact angle for deionized water (DIW) after treatment, discussed later in the chapter, is considerably lower than that for BTA or CBTA;

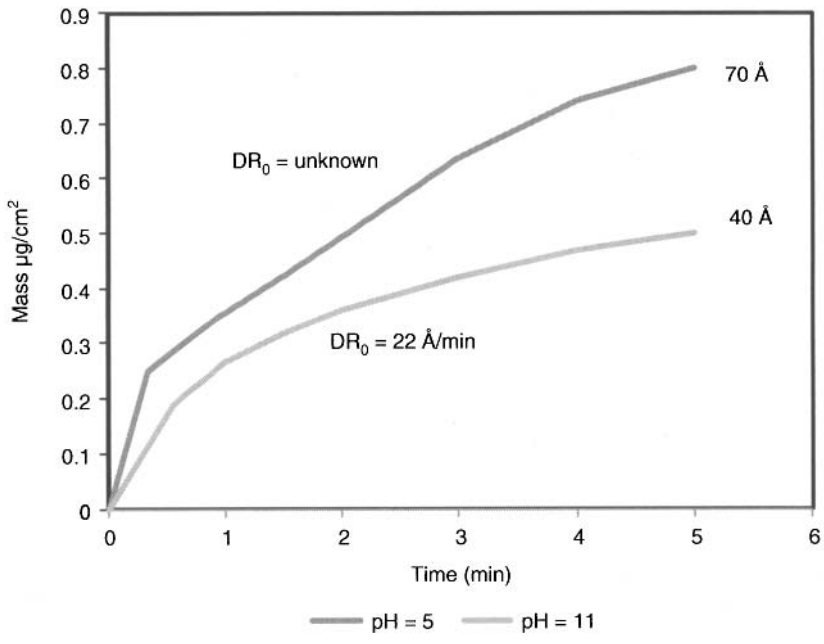



**Figure 11.6.** Benzotriazole film deposition kinetics on Cu at pH = 5 and 11 determined using a quartz microbalance in an electrochemical cell. The solution consisted of 1000 ppm of BTA in water. $DR_0$ is the deposition rate. The graph is based on data from [46]. Used with permission from the author.

however, it also does not protect all Cu crystallographic orientations. TAZ appears to protect all Cu crystallographic orientations and yields a hydrophilic surface to aid cleaning and rinsing eliminating the need for expensive and hazardous alcohol rinses. TAZ also has another unique property that has been exploited when designing a commercially available Cu post-CMP cleaner and will be discussed in Section 11.4.

Figure 11.7 describes TAZ speciation as a function of pH. Below $pK_{a1}$, $TAZH^+$ is the dominate species; $TAZ^-$ is the dominate species above $pK_{a2}$, and between $pK_{a1}$ and $pK_{a2}$, TAZ is the dominate species. Figure 11.8 contains TAZ deposition data at pH = 5 and 12 acquired with a QMB in an electrochemical cell [46]. Under similar deposition conditions, the film thickness for TAZ is less than 50% compared to BTA. The initial deposition rate is about 25 Å/min, at pH =5, similar to that observed for BTA deposited at pH = 11. The film appears self limiting – there are no breaks in the deposition curve implying a single mechanism and the film thickness asymptotically approaches a limit of about 35 Å for the deposition conditions tested. At pH = 12, the film has a slower deposition rate but appears self limited at about 20 Å approaching a self assembled monolayer (SAM) [46].

Because TAZ protects all Cu crystallographic orientations and provides a hydrophilic surface, this compound could be an ideal Cu corrosion inhibitor. The film formed by TAZ appears to be significantly thinner than that formed by BTA under similar conditions. As mentioned previously, one problem with BTA is the removal of the passivating film. The QMB can be used to investigate film removal as well as film deposition. Figure 11.9 depicts QMB results of BTA film removal in a citrate solution with pH = 4. Use of a citrate solution for a post-CMP clean is not uncommon. However, the time necessary to remove a 75-Å thick BTA film would be more

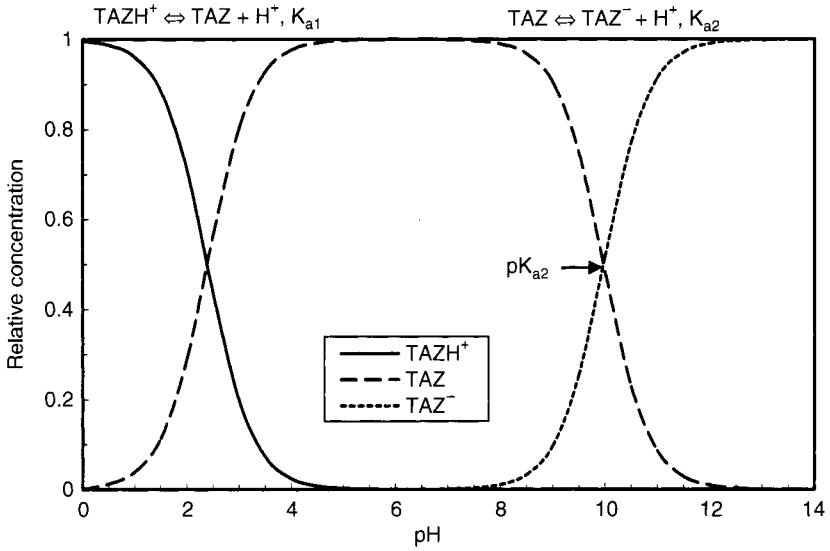



**Figure 11.7.** 1,2,4-triazole species versus pH. The dominant species below $pK_{a1}$ is $TAZH^+$, above $pK_{a2}$, $TAZ^-$ is the dominant species, and between $pK_{a1}$ and $pK_{a2}$, TAZ is the dominant species. Used with permission from the author.

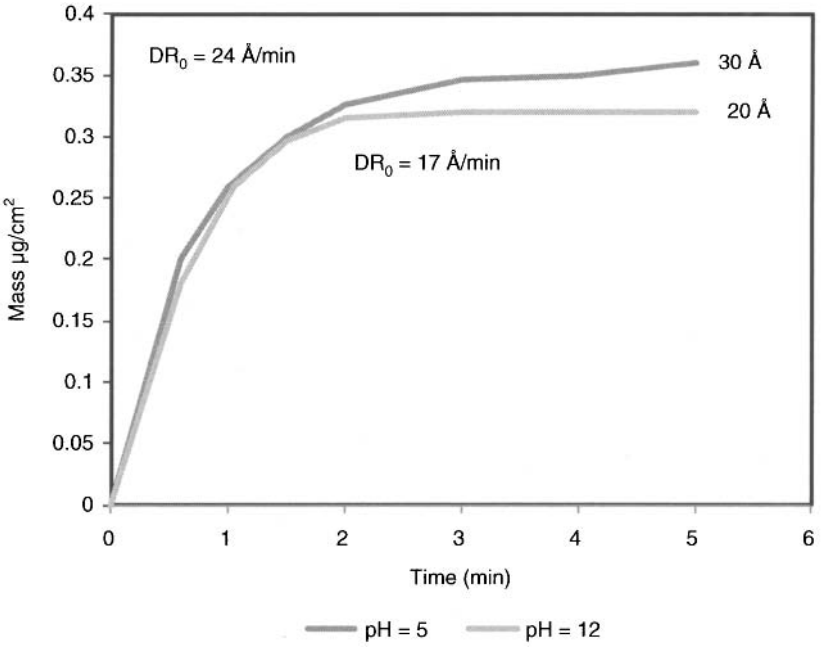



**Figure 11.8.** 1,2,4-triazole film deposition kinetics on Cu pH = 5 and 12 determined using a QMB in an electrochemical cell. The solution consisted of 700 ppm of TAZ in water. The film is notably thinner than that for typical BTA films (40–70 Å). The graph is based on data from [46]. Used with permission from the author.

than 3 minutes. The typical IC processing allowable cleaning time is one minute or less; consequently, a significant portion of the BTA film would remain on the Cu explaining the implementation of surfactants – to remove the particles generated by the BTA residue or reduce the metal contamination concentration [52, 53] and costly alcohol drying techniques needed to control watermarks [54].

In Figure 11.9, QMB data shows that BTA removal by an oxalate solution is significantly faster than that for citrate. However, an oxalate solution of pH = 4 also removes the underlying cuprous oxide resulting in Cu corrosion during wafer staging. Cu corrosion during wafer staging has been correlated to a decrease in time dependent dielectric breakdown (TDDB) [46]. Nonetheless, a 100 Å thick BTA film would be removed in less than a minute with an oxalate solution.

One other criterion needed for an effective post-CMP cleaner is an understanding of the impact of pH on zeta potential. At pH = 4, most materials and particles have equal and positive zeta potentials, so particle removal would be compromised with an acidic citrate or oxalate solution. To produce large negative zeta potentials for typical process layers and particles, a much higher pH is needed. Figure 11.9 contains QMB data for BTA film removal using a dilute TMAH solution. The BTA removal rate is equivalent or better than that achieved with an oxalate solution. The underlying cuprous oxide film is also removed at this pH. Methods to deal with preserving the underlying cuprous oxide layer to provide corrosion protection during wafer staging is presented in Section 11.4.2.

If the OCP for the Cu in the cleaner is set at a value less than the reduction potential for cuprous oxide, then the film will be preserved if it is not soluble in

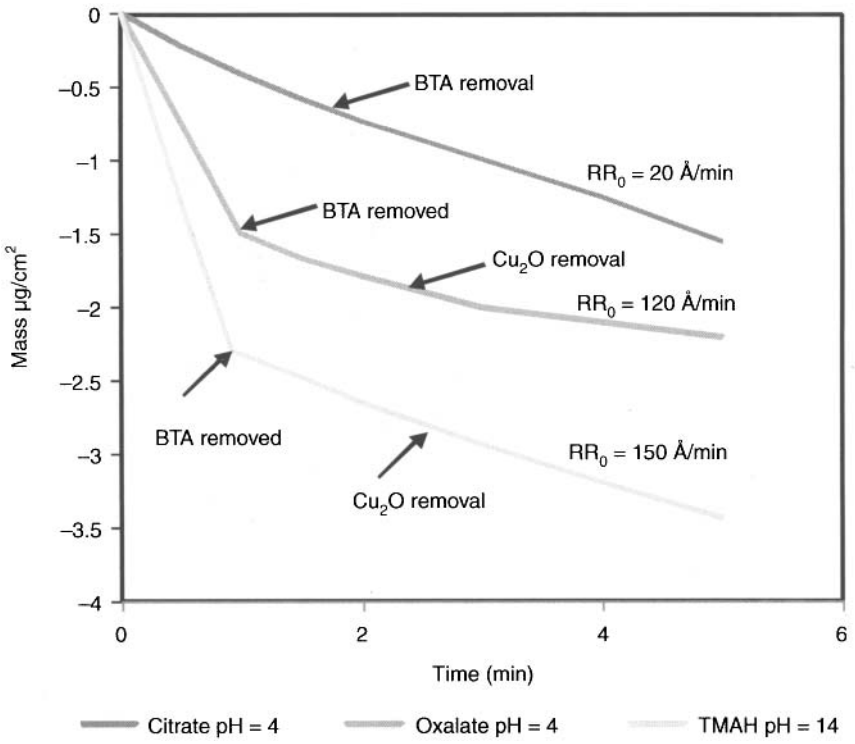



**Figure 11.9.** Quartz microbalance data for the removal of BTA with various solution. (a) Removal of BTA with citrate solution. The pH of the solution is increased with ammonium hydroxide. The time necessary to remove a 75-Å BTA film is more than 3 minutes. (b) Removal of BTA with oxalic acid solution. The pH of the solution is increased with ammonium hydroxide. The time necessary to remove a 75-Å BTA film is more than 1 minute. (c) Removal of a 150-Å thick BTA film with a dilute TMAH solution at pH = 14. This solution also removes the underlying cuprous oxide film. The graph is based on data from [46]. Used with permission from the author.

the solvent matrix [46, 55]. Adding a reducing agent may be sufficient to lower the OCP to the point where cupric oxide would be removed (or reduced) while cuprous oxide would be retained [46]. Examples of that approach are discussed in Section 11.4.2 where the function of each of the post-CMP cleaner components will be detailed. Section 11.4.1 performs a similar dissection of commercially available BEOL post-etch cleaners and explains the function of each component.

Figure 11.10 contains QMB data for TAZ removal by the same oxalate solution shown in Figure 11.9. The TAZ removal rate is at least two times faster than that for BTA under similar circumstances. A process time of about 5 seconds would be sufficient to remove a TAZ film that was 20-Å thick. Similar to the results shown in Figures 11.9, the cuprous oxide is also removed but this may be prevented with additives, such as ascorbic acid. However, the most successful second generation post-CMP cleaners have pH values with ranges ~7 [56] and above. Acidic citrate solutions are considered first generation cleaners and are now used either as pad cleaners or in conjunction with an alkaline cleaner to provide the most satisfactory surface preparation.

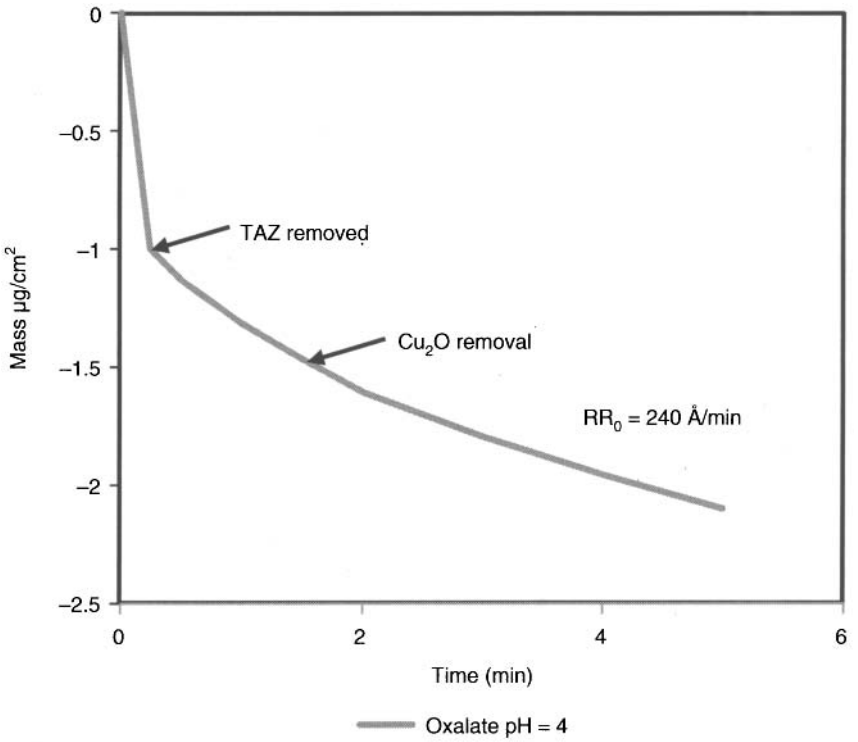



**Figure 11.10.** Quartz microbalance data for the removal of 1,2,4-triazole and cuprous oxide removal with an oxalic acid solution. The pH of the solution is adjusted with ammonium hydroxide. A 20-Å thick TAZ film is removed in 5 seconds. This solution also removes the underlying cuprous oxide. The graph is based on data from [46]. Used with permission from the author.

Figure 11.11 contains electrochemical data showing the displacement of BTA by TAZ. The initial 200-Å thick BTA film was removed and replaced with a 20-Å thick TAZ film. The overall process time can be decreased for a thinner BTA film. Extensive analyses of processed wafers indicated that a typical post-CMP wafer has a BTA film that is about 75-Å thick [78].

### *11.3.1.6 Process Results of Azole Cleaning Solutions*

Figure 11.12 contains scanning electron microscope (SEM) images of Cu after post-CMP cleaning using test formulations with different azole corrosion inhibitors [78]. The composition consists of water, 2-aminoethanol, ascorbic acid, and TMAH [78]. Equimolar amounts of the different corrosion inhibitors are added to the base formulation and evaluated for cleaning, corrosion inhibition, and wettability of the treated Cu surface. The inhibitors tested are BTA, CBTA, 5-ATA, and TAZ. Some of these did not protect all crystallographic orientations – including BTA, the most commonly used Cu corrosion inhibitor. Of the compounds tested, TAZ cleaned best and protected all Cu crystallographic orientations in this solvent matrix.

An example of the organic residue left after BTA passivation is shown in Figure 11.13; this residue can take the form of thin-layers or agglomerations. Energy-dispersive x-ray spectroscopy (EDX) of these residues shows a signature

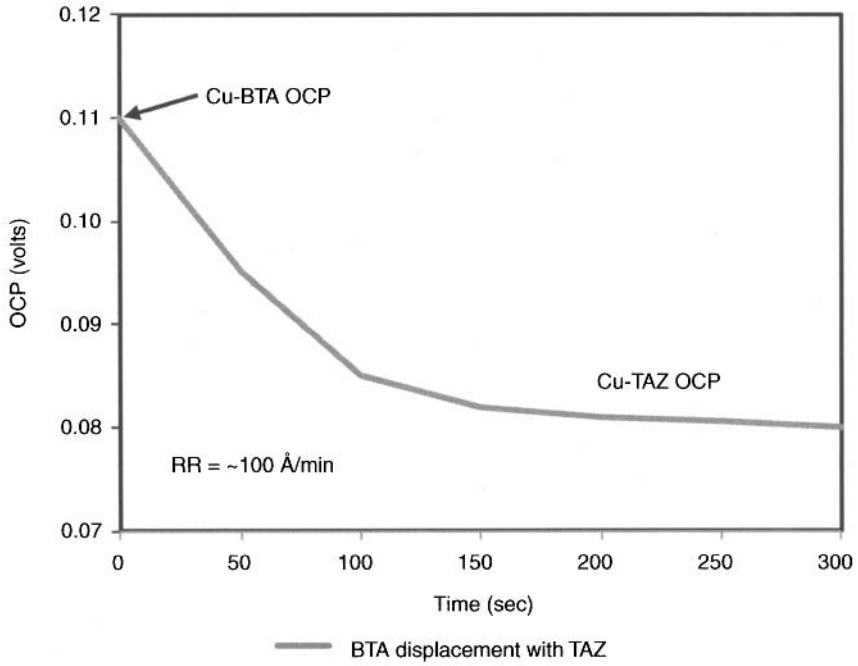



**Figure 11.11.** Open circuit potential measurements over time showing the displacement of a 200-Å thick BTA film by a 20-Å thick TAZ film. The BTA removal rate was about 100 Å/min. The graph is based on data from [46]. Used with permission from the author.

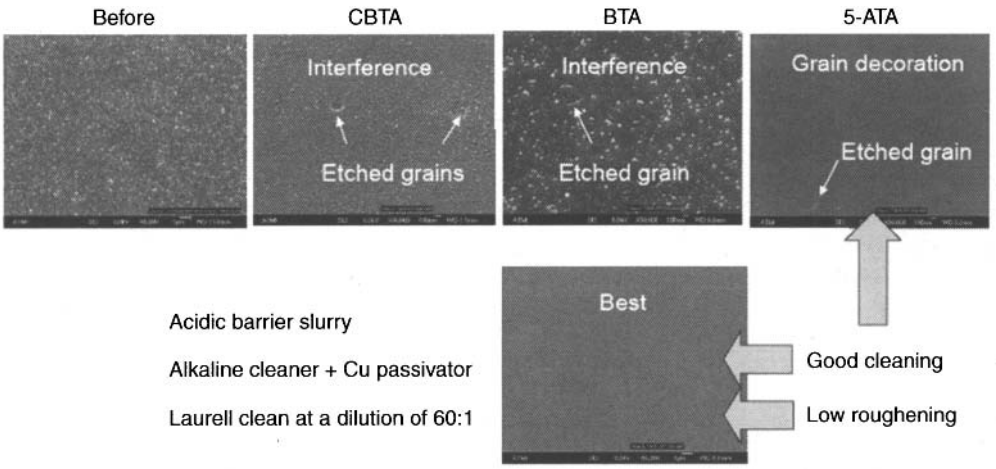



**Figure 11.12.** Scanning electron micrograph images showing post-CMP cleaning and the impact of the Cu inhibitor used in the cleaner which consisted of water, 2-aminoethanol, TMAH, and ascorbic acid. Some inhibitors did not protect all Cu crystallographic orientations. Compiled and based on data in [46]. Used with permission from the author.

of carbon [57], that is detected only on the copper areas of the wafer. The researchers observed that addition of surfactant to the BTA post-CMP cleaning solution increased the number of carbon-containing defects. By either reducing the amount of surfactant or BTA, the number of defects was reduced.

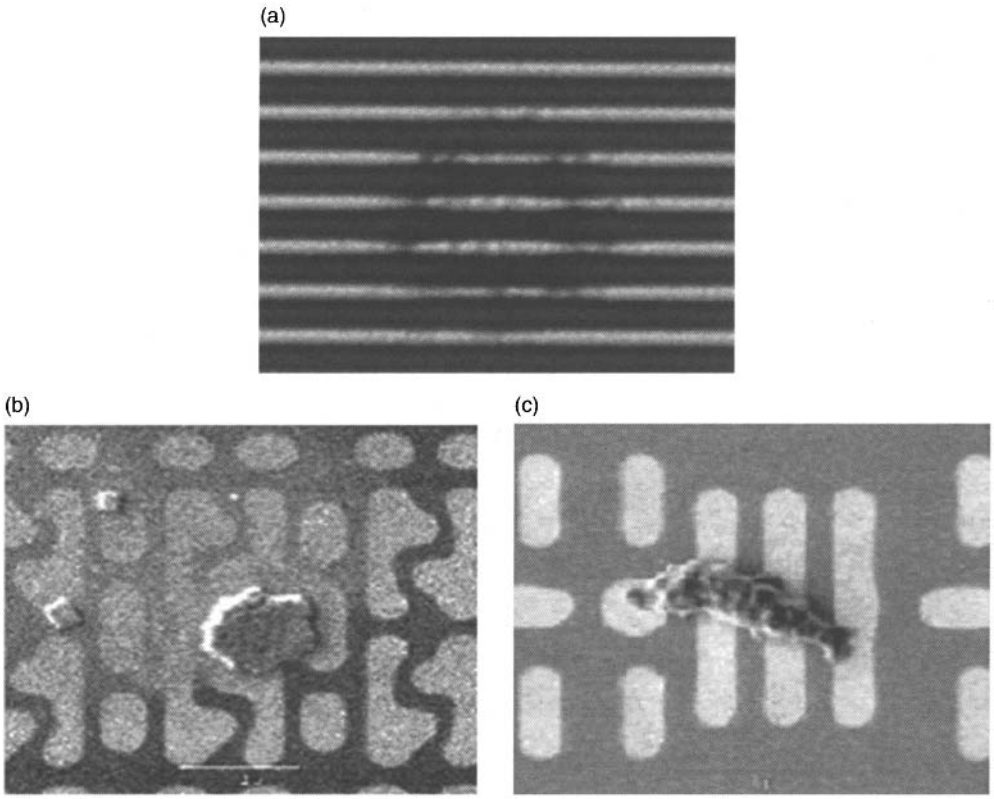



**Figure 11.13.** Examples of organic residue on post-copper CMP surface, all show the EDX signature of BTA. (a) Used with permission from the author. (b) and (c) [46]. Reproduced with permission of ECS – The Electrochemical Society from Peters, D., Bartosh, K., Tran, C., and Watts. C., *Electrochemical Society Transactions*.

The contact angle for DIW after cleaning is also very different for the four formulations, as shown in Figure 11.14. When comparing formulations that cleaned better than others, the best cleaners typically have a low contact angle. In order to adequately clean a surface, it must be wetted. Hydrophobic surfaces are well known to be difficult to clean. Thus, surfactants have been used as additives to lower the surface tension of solutions intended for use on hard to wet films [52].

## 11.3.2 Oxygen Scavengers

The Cu corrosion inhibitors used for IC applications do not scavenge $O_2$; instead they form a passivating film. Researchers have shown that the efficiency of an inhibitor is very dependent on the solvent matrix and is metal specific. Data from Cobratec [58] readily addresses this point. Even though they are highly efficient inhibitors for other metals, two of the most efficient oxygen scavengers, 1,2-dihydroxybenzene (catechol) and 3,4,5-trihydroxy benzoic acid (gallic acid), function as accelerators increasing Cu etch rates in an alkaline semi-aqueous solvent matrix, due to their solubility and $Cu^{+2}$ complexing capabilities [1, 11, 59]. Under acidic conditions, dissolved molecular oxygen may no longer be the oxidizer in aqueous or semi-aqueous solutions. The oxygen in water can be reduced and act

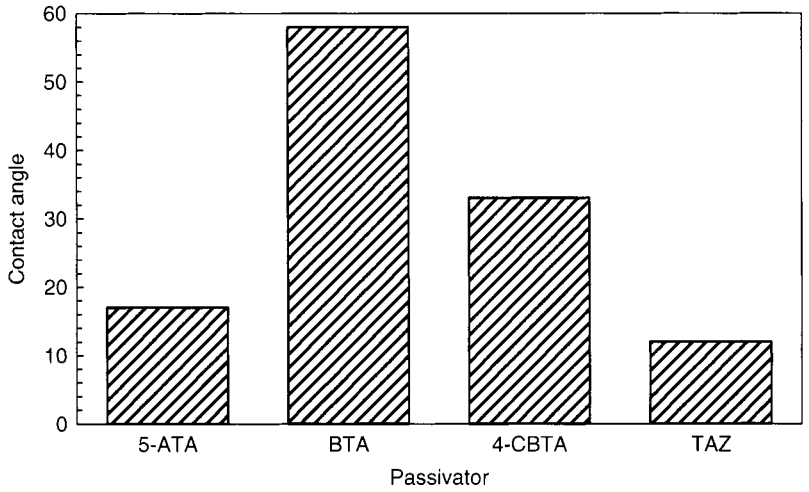



**Figure 11.14.** Variation in DIW water contact angle on Cu after treatment with different Cu corrosion inhibitors for the formulations shown in Figure 11.12. Used with the permission of the author.

as the oxidizing agent to promote metal corrosion. Consequently, oxygen scavengers are typically ineffective in acidic cleaning formulations.

### 11.3.3 Diols, Triols, and Carboxylic Acids

This section examines several diols, triols, and carboxylic acids that have demonstrated Cu corrosion inhibition in several solvent matrices. Table 11.3 and 11.4 contain the structures for these compounds that will be discussed in this section. There are other compounds in these categories that could be tested (and many have been) for Cu applications; however, many are not available with the requisite purity or are extraordinarily expensive making them unlikely candidates for inclusion in IC applications. It is possible that another less demanding technology (*i.e.* disk drives, photovoltaics, MEMS-mechanical electrical micro structures) may benefit from their use if trace metal contamination were the only issue.

The compounds in Table 11.3 and 11.4 interact with metal films much in the same way as azoles – the deprotonated acid can chemisorb onto oxidized metal surfaces producing an insoluble passivating film to prevent further oxidation of the metal [11]. The interaction is through the deprotonated carboxyl or hydroxyl groups and open *d*-orbitals of the metal ion. Some of the acids listed have $pK_a < 4$, so they may work effectively in neutral or slightly acidic formulations. In general, carboxylic acids appear to be more effective when the solution pH is at least three units above the $pK_a$ [11].

Other similar classes of compounds include α-hydroxy acids that contain both a hydroxyl and an acid group, such as glycolic acid [60].

#### *11.3.3.1 Corrosion Inhibition Efficiency*

One aspect of diol/triols and carboxylic acids that is not generally true for azoles is that they can often provide protection for other metals – most notably Al.

**Table 11.3.** Diol and triol corrosion inhibitors.

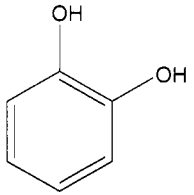
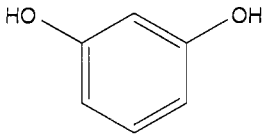
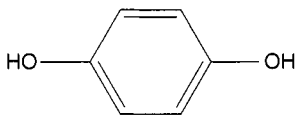
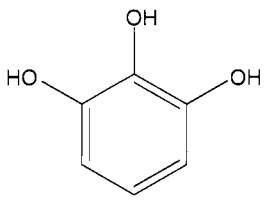
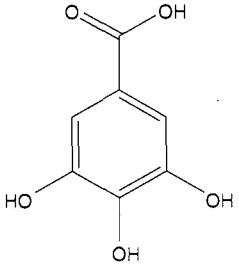
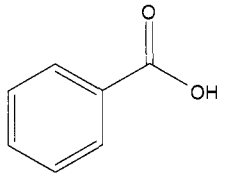
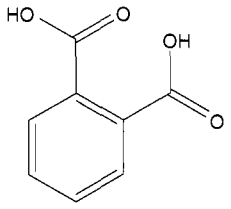
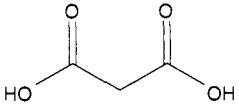
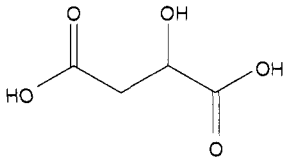
| Diol / Triol | | Molecular Structure | Comments |
|---|---|---|---|
| Catechol | 1,2-dihydroxy-benzene |  | When catechol is in an alkaline solution, both hydroxyls can be deprotonated yielding an excellent chelating agent for metal cations. Catechol is a good oxygen scavenger. |
| Resorcinol | 1,3-dihydroxy-benzene |  | Like catechol, when resorcinol is in an alkaline solution, both hydroxyls can be deprotonated. Unlike catechol, deprotonated resorcinol cannot chelate with metal cations. Unlike catechol, resorcinol is not an oxygen scavenger. |
| Hydroquinone | 1,4-dihydroxybenzene |  | Like its isomer relatives, catechol and resorcinol, both hydroxyl groups can be deprotonated in alkaline solutions. Like resorcinol, deprotonated hydroquinone cannot chelate with metal cations. Hydroquinone is an oxygen scavenger. |
| Pyrogallol | 1,2,3-trihydroxybenzene |  | In alkaline solutions, pyrogallol can be completely deprotonated and it can effectively chelate with metal cations. Pyrogallol is an extremely effective oxygen scavenger. |

**Table 11.4.** Carboxylic acids corrosion inhibitors.

| Carboxylic Acid | | Molecular Structure | Comments |
|---|---|---|---|
| Gallic | 3,4,5-trihydroxybenzoic acid |  | Much like pyrogallol, in alkaline solutions, gallic acid can effectively chelate with metal cations when its hydroxy groups are deprotonated. Additional interaction can occur through the carboxylic acid group. Gallic acid is an effective oxygen scavenger. |
| Benzoic | Benzoic acid |  | Benzoic acid cannot chelate with metal cations but is a strong complexing agent when in alkaline solutions and the carboxylic acid is deprotonated. Benzoic acid is not an oxygen scavenger. |
| Phthalic | 1,2-dicarboxybenzene |  | Phthalic acid is a strong chelating agent for metal cations in alkaline solutions but has very low solubility in aqueous formulations. Phthalic acid is an effective oxygen scavenger. |
| Malonic | Malonic acid |  | Malonic acid can be a strong complexing agent for metals in alkaline solutions. Malonic acid is not an oxygen scavenger. |
| Malic | Malic acid |  | Malic acid can be both a complexing and chelating agent for metal ions at high pH. Malic acid is not an oxygen scavenger. |

Consequently, it is possible to design a cleaning solution containing a single corrosion inhibitor that would work equally well on Cu and Al.

Figure 11.15 shows Cu and Al inhibitor efficiency data for various diol/triols, carboxylic acids, 8-hydroxyquinoline, and BTA in a solvent matrix consisting of DMAC and water with choline hydroxide to raise the pH to ~11 [11]. Diol/triols and carboxylic acids tend to work best when they are deprotonated – hence the alkaline test solvent matrix. Typically, an efficiency of 95% (Section 11.2.3) or higher is needed to be considered an excellent corrosion inhibitor. Resorcinol and hydroquinone provide the best inhibition for Cu – approximately 93%. All of the solutions provide excellent inhibition for Al.

The Cu corrosion inhibition efficiency for three isomeric inhibitors; catechol (–103%), resorcinol (93%), and hydroquinone (93%) indicate that steric hindrance plays a role in efficiency. Resorcinol and hydroquinone act as Cu corrosion inhibitors in this solvent matrix, but catechol and gallic acid act as an accelerator, as shown in Figure 11.15. At high pH, catechol and gallic acid, another acid with a negative efficiency, are deprotonated and can chelate with $Cu^{+2}$ very effectively. Only the dianion of catechol can chelate with $Cu^{+2}$ one to one in the isomeric series. Besides catechol, other molecules such as pyrogallol, gallic acid, phthalic acid, and malic acid have adjacent groups (either hydroxy or carboxy) that can be deprotonated in alkaline solutions and consequently chelate with metal cations. The monocarboxylic acids cannot chelate, but are strong complexing agents for metal cations and can form polymeric passivating films. Solubility is inversely proportional to molecular weight; consequently, polymeric passivating films tend to be insoluble.

Both resorcinol and hydroquinone dianions appear to form a polymer-like structure where each $Cu^{+2}$ ion is complexed to two anions [11]. The effective molecular

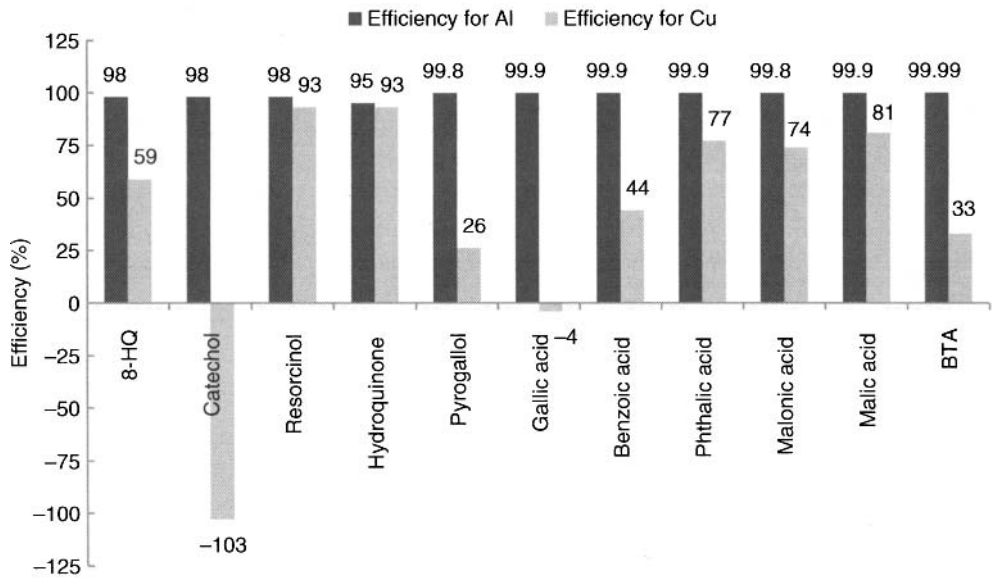



**Figure 11.15.** Corrosion inhibitor efficiency in a solvent mix of DMAC and water with choline hydroxide to raise the pH to about 11. Equimolar amounts of inhibitor were used for each test. Based on reference [11]. Used with permission of the author.

weight of the resorcinol- or hydroquinone-Cu complex is much higher than that for the catechol-Cu complex resulting in lower solubility in this solvent matrix.

Deprotonated catechol can chelate with $Cu^{+2}$ and dissolve acting as an effective Cu ion scavenger on a dielectric. Catechol and gallic acid may effectively remove Cu ions on dielectric films; however, it is unknown whether they can substantially affect the Cu ion distribution within the dielectric film. The use of post-CMP cleaners containing gallic acid has been shown to cause a pronounced improvement, as much as three orders of magnitude, in TDDB [78]. This suggests that gallic acid may be lowering the Cu ion concentration within the dielectric film as well as removing surface contamination.

Some corrosion inhibitors, such as gallic acid, in alkaline solutions are excellent chelating agents for $Cu^{+2}$ but not for $Cu^{+}$. Thus, it is possible to oxidize Cu, selectively dissolve CuO, and leave $Cu_2O$ as a protective film without resorting to using Cu corrosion inhibitors [78]. Consequently, if gallic acid or catechol is added to dilute TMAH solution, pH = ~12, it is possible to selectively dissolve a cupric oxide film and leave the underlying cuprous oxide film virtually untouched [78].

The efficiency is positive for Al with BTA and all the acids tested in the solvent matrix. However, BTA for Cu in this solvent matrix shows poor efficiency compared with the carboxylic acids. The data implies that the passivating film is partly soluble in the solvents used. Additional data for benzoic acid and Cu is shown in Figure 11.16 [61]. An explanation for the increase in etching rate with increasing DMAC concentrations is that the Cu-benzoate film is partly soluble in DMAC and less soluble in water. If it were totally soluble, the efficiency would be zero. Since it is partly soluble, the efficiency is greater than zero but less than 1. The method used to determine the etch rate can influence the data. Based on the data with the solvent matrix used in Figure 11.4, BTA would not be chosen as a Cu inhibitor; however, there are

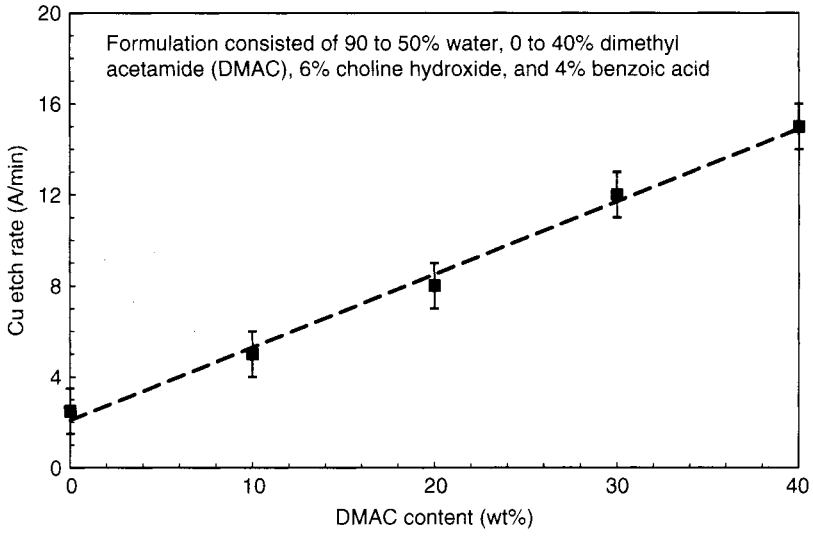



**Figure 11.16.** Variation in Cu etch rates with DMAC content. The complex formed with the benzoic acid anion and $Cu^{+2}$ is soluble in DMAC but less soluble in water. Used with permission of the author.

numerous cleaning formulations that contain BTA, and they have been proven to be effective because they use a different solvent matrix.

### 11.3.4 Mercaptans

This section discusses sulfur-containing Cu corrosion inhibitors; mercaptans. These compounds are not stable over a wide pH range, so their use may be more restricted compared to azoles or carboxylic acids. Under acidic conditions, mercaptans may be reduced producing sulfur as a precipitate; consequently, they are better suited for alkaline formulations. The thio group is a strong acid, and the thiolate ion is very reactive since sulfur is a stronger nucleophile than oxygen. Thiols are analogs of alcohols and are soluble in organic solvents.

A mercaptan species that has been investigated for corrosion inhibition in the IC industry is 2-metrcaptobenzimidiazole (2-MBI) which is shown in Figure 11.17. There are derivatives of 2-MBI that also may have capabilities as Cu corrosion inhibitors. They include carboxylic acid and amino derivatives; however, a major problem with mercaptans is their low solubility in aqueous formulations. The S-H bond is somewhat covalent due to the small electronegativity difference between hydrogen and sulfur, so there is little hydrogen bonding either to water or other mercaptans [62]. They have a lower boiling point than their alcohol analogs due to a lack of hydrogen bonding. The literature for applications to semiconductor manufacturing is scant if nonexistent. Lastly, issues have been noted for obtaining sufficient purity for applications to IC manufacture. Significant trace metal contamination (high ppm levels) is common in commercially available, affordable product. If a fraction of a percent (*i.e.* 0.1% by weight) in a formulation is used, the trace metals may be in the high ppb level and still not acceptable depending on which trace metals are present.

## 11.4 Copper Cleaning Formulations

This section will discuss the formulations of cleaning products used on Cu applications. Both post-etch and post-CMP cleaners will be examined. In particular, their components will be listed, and their function will be noted. In many cases, a component may serve several functions, for example, solvent and complexing agent or corrosion inhibitor and chelating agent. The formulation must reliably clean and be tolerant of minor, but typical, process variations. The product

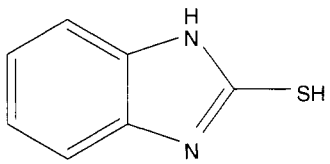



**Figure 11.17.** Structure of 2-mercaptobenzimizidazole (2-MBZ). Passivation film formation can occur through both nitrogen atoms and the sulfur atom. Both protons are acidic and can be removed at high pH; 2-MBZ is not stable under acidic conditions.

must have an appropriate bath life if it is recirculated and reused; so its cleaning capabilities must be tolerant of small changes in composition. It cannot contain banned substances (*i.e.* carcinogens, mutagens, high toxicity) nor can it contain high levels of typical trace metals. Surfactants are typically banned due to bioaccumulation, and indiscriminate chelating agents (*e.g.* EDTA) are banned since they accumulate heavy metals from the waste stream.

The general requirements for post-etch and post-CMP cleaners are similar; however, it is rarely necessary to deal with particle removal during post-etch cleans. The residue that must be removed tends to be polymeric and not particulate in nature. Post-CMP cleaners, on the other hand, must deal with removal of particles since the major contamination is slurry and CMP debris, both particulate contaminations. Additionally, during a post-CMP clean the Cu passivator may have to be removed or problems downstream may occur. Designing a post-CMP cleaner tends to be more difficult than designing a post-etch cleaner since both particle and polymer removal must be addressed. Another distinction between post-etch and post-CMP cleaners involves the fact that post-CMP cleaning is performed one wafer at a time whereas a batch or a single wafer process can be used for post-etch cleaning. Thus, a post-etch cleaner designed for both a batch and single wafer process is preferred from a commercial standpoint. It is easier to design a post-etch cleaner for a single wafer application and then dilute it to work on a batch process where the immersion time is on the order of 10–30 minutes instead of 1 minute or less. The typical process time for a post-CMP cleaner is 1 minute. The last distinction between designing the two types of cleaners is that post-CMP cleaners are typically run at room temperature and diluted 30 to 100:1 at time of use with high purity water whereas post-etch cleaners are typically run undiluted and heated.

### 11.4.1 Post-etch Cleaners

Prior to deposition of copper barrier material after trench and *via* definition of the dual Damascene structure, stripping to remove the photoresist, and the post-etch residue, the standard practice for IC manufacturing for removing airborne molecular contaminates (AMC) and Cu-oxides is argon ion sputtering of the Cu surface in a plasma chamber. Some integration schemes also call for a reductive plasma process to reduce any copper oxides to $Cu^0$ before deposition of the barrier material ensuring a clean Cu surface beneath the barrier layer.

As previously discussed, the common approach to corrosion inhibition for Cu is forming an insoluble passivating film. A chelating or complexing agent that differentiates between $Cu^{+2}$ and $Cu^{+}$ can selectively remove cupric oxide but not cuprous oxide. Use of a post-etch cleaner that effectively removes Cu-ion contamination from dielectric surfaces can have a positive impact on TDDB performance [63]. Additionally, removing the severely oxidized copper at the bottom of the *via* and/or trench structure improves the *via* chain resistivity [40]. Care must be taken to remove the oxidized copper, not etch the copper, and leave a passivating film that can be removed before the next metal layer is deposited. The low-$\kappa$ material must not be attacked nor the dielectric constant affected. Chapter 10 outlines the potential integration structures for copper integration.

The post-etch cleaning solution must not only passivate the surface but adequately remove the residue; in some cases it must also strip the photoresist. The cleaning formulation must remove the residue that is formed, whether it is from sputtered copper, fluorinated residue from the etching process, or any other contaminant that may be present. The solution must also be able to effectively wet high aspect ratio features and hydrophobic surfaces.

This section discusses the components in some typical BEOL Cu post-etch cleaners that have been commercially available for about 10 years. The compositions can be found in patents and MSDS (material safety data sheets) to assist in assessing the components. A good overview of the post-etch cleaning formulations used for dual Damascene copper in the presence of low-κ material is given in [64] which reported the cleaning results with semi-aqueous fluoride-containing, TMAH-containing, phosphate-containing products, and several organic acids. The electrical data and metal contamination data showed the fewest problems with organic acids, specifically with the alpha-hydroxyacids.

All the formulated solutions used for dual Damascene post-etch cleaning are semi-aqueous, either alkaline [65] or acidic [66] in composition, some contain fluorides [67] and some are fluoride-free. To offset the high cost of single wafer tools and to lower the cost of ownership (CoO), commodity chemicals, included dilute mineral acids, bases, and dilute HF (DHF), are used by some IC manufacturers [68]. Key formulation components and their function can be found in Chapter 5.

One of the first commercially available products, Air Products ACT-970, is still in use today as a post-etch cleaner and is used for both Cu and Al high volume manufacture (HVM). ACT-970 is an alkaline formulation that contains an organic solvent (a secondary alkanolamine), water, and two common corrosion inhibitors; a carboxylic acid and an azole [2]. Carboxylic acids can be effective corrosion inhibitors in alkaline solutions for Al, and azoles are effective for Cu, as described previously. N-methyl ethanolamine, a secondary amine was selected to minimize Si etching that is readily observed in primary alkanolamine (*e.g.* ethanolamine) and water mixtures [2]. Alkanolamines are effective metal complexing agents that assist in the removal of metal ions from dielectrics and have been used for IC cleaning formulations for some time as discussed in Chapter 5. Water is required to dissolve both gallic acid and BTA even though neither has significant solubility in water. Some formulations, such as ACT-970 are designed for batch applications at elevated temperatures of 60–70°C and likely will not perform well in single wafer applications. Typical process times are 20–30 minutes.

Other commercially available products, such as NE products from ACT-Air Products, are designed to operate at room temperature and are acidic. Some of these formulations consist of water, a water-miscible organic solvent, a fluoride source, and a buffer for pH stability [69]. Fluoride-containing compositions typically are used at room temperature because of fluoride aggressiveness. A review of fluoride-containing cleaning products and their effect on the removal of copper oxides to expose the copper metal is given in reference [69, 70]. A possible two-step cleaning processes has been proposed for semi-aqueous fluoride products. The first step involves the conversion of the post-etch resides into fluoride-containing residues which are dissolved in the water rinse step [71].

Buffering agents are used to maintain the pH of the BEOL post-etch cleaner over the life of the bath. Some products contain a simple acetic acid buffer which is comprised of glacial acetic acid and ammonium hydroxide in equimolar amounts to set the pH at 4.75, the $pK_a$ for acetic acid [69, 72]. The post-etch residues removed tend to be acidic in nature and without a buffer system to maintain pH, the pH of the stripper decreases with time. This alters the oxide and metal etch rates over time, potentially shortening the bathlife of the product and increasing the CoO. Typical bathlifes of more than 48 hours are obtained in both batch and single wafer applications. Bathlifes of significantly longer than 48 hours are reported for single wafer applications [69].

Most products use an amide which is a polar, water miscible organic solvent known to dissolve organic and inorganic materials, much like dimethylformamide, but lacking the carcenogicity and severe toxicity [65–67]. Water is necessary to dissolve the fluoride during manufacture and also the fluoride salts produced during application [69, 72].

The water miscible organic solvent is used to dissolve organic residues-like residual photoresist or organic residues remaining after an incomplete plasma stripping process. Copper or Al corrosion at a pH of about 5 is negligible, so there is no need to add a corrosion inhibitor. Another example of a cleaning solution is ATMI ST-250, which contains fluorides. The organic solvent post-etch used is a tertiary amine. It also contains a chelating agent for removing metal ion contamination. Typical batch process conditions for ST-250 are 20 to 60 minutes at 45°C. Slightly elevated process temperatures are needed for ST-250 due to its high viscosity at room temperature causing recirculation issues. ST-250 does not contain a buffer and suffers from a shortened bath life due to pH drift. Problems can result from the reaction of the fluorides and the amine – generating by-products during manufacture that result in particles.

Single wafer applications are limited due to the inability of some single wafer tools to heat the stripper and to the fact that the formulations developed for batch processing were not aggressive enough for sub-one minute process times. Current generation single wafer formulations include semi-aqueous fluoride products that can be used between 20°C to 35°C to meet the stringent time constrains for single wafer tools [73]. These products have an unusual feature; addition of water (accidental or deliberate) does not significantly affect the etch rates of silicon dioxide dielectric.

### 11.4.2 Post-CMP Cleaners

Post-copper CMP cleaners must remove the copper oxides without extensively etching the metal, passivate the copper surface, not affect low-κ dielectrics, and remove the slurry and any extraneous particles that are on the wafer surface after the CMP process. Most if not all of the Cu-ion contamination on a dielectric after a Cu-CMP process is in the form of $Cu^{+2}$ that is due to the use of $H_2O_2$ and the acidic composition of many copper CMP slurries.

This section discusses post-CMP cleaner formulations. The component's functions are explained. As mentioned in Section 11.3.1, all the component information was collected from materials in the public domain (*i.e.* patents, company literature,

presentations, company web sites, MSDS sheets). Unlike post-etch cleaning formulations, water is the major component (*e.g.* > 85% by weight) in post-CMP cleaners.

Post-CMP cleaner solutions are used in roller and other types of brush boxes, immersion baths, buff stations, spray garage, and as pad cleaners. Some products are alkaline [74] while other products are acidic [2, 75] or have pH = ~7 [56]. In many post-CMP brush cleaning applications, the process of record (POR) uses an alkaline product in the first brush box (BB1) followed by an acidic product in BB2, or the converse. The typical approach uses the alkaline product first to aid in particle removal since all abrasives and most process materials have a large negative zeta potential at a pH =10 or greater resulting in repulsion to aid particle removal. On the other hand, abrasives and most other materials have a weak, positive zeta potential at acidic pH values making particle removal more difficult and requiring excessive mechanical cleaning assistance, such as megasonic energy to achieve acceptable particle removal efficiency (*e.g.* for slurry removal) [76]. It was thought, but never definitively proven, that the acidic clean aided in metal ion removal. It is true in general that metal ions tend to be more soluble in acidic solutions than in alkaline solutions. Oxidation kinetics is also typically quite different in the two pH extremes. To be able to wet the copper effectively, especially with the BTA complex on the surface, surfactants have been used [45]. Most post-CMP cleaner components intentionally serve multiple purposes.

The alkaline pH of some products is set by using an organic strong metal ion-free base, such as TMAH. Many commercially available products contain an amine, either a primary alkanolamine or a tertiary alkanolamine, both of which are water soluble organic solvents, as discussed previously. They can function as a solvent to help solubilize organic post-CMP residues like BTA. They can also assist in removing Cu ions from a dielectric since amines readily complex with metals, especially Cu [77]. They can also act as a buffer to maintain pH upon dilution. A carboxylic acid can also serve several purposes in cleaning formulations. It can readily complex with metal ions under alkaline conditions [77]. It is also a reducing agent and can limit the OCP achieved for a Cu surface, strongly impacting the corrosion potential. As an example, some cleaners readily dissolve cupric oxide (CuO), but do not dissolve cuprous oxide ($Cu_2O$) resulting in a less reactive surface after cleaning [46]. The acidic cleaners will remove both copper oxides leaving a significantly more reactive Cu surface after cleaning. Consequently, limits have been set for the maximum queue time for wafers after post-CMP cleaning prior to the next process step to minimize yield loss due to Cu corrosion. In some cases, that is a few hours at most. Products have been developed that provide more than two-weeks queue time without Cu corrosion, thus having a significant impact on cost of manufacture (CoM) [46, 78]. Data presented in Figure 11.12 showed TAZ displacing BTA. Using a TAZ-containing solution in either the buff station or a brush box will result in removal of BTA and deposition of a thinner, more easily removed passivating film that protects Cu from corrosion. The displacement of BTA also aids cleaning by providing an undercut and liftoff mechanism without attacking the substrate [78].

Some acidic products are carboxylic acid-containing solutions that contain a corrosion inhibitor or chelating agent (EDTA), some use ammonia to slightly adjust the pH, and some contain a surfactant. Electroclean (EC) is one of the most widely used acidic post-CMP cleaners [79]. Adding a fluoride source to the carboxylate

solution provides a mechanism for reduction of silica particle size and is equivalent to an undercut and liftoff mechanism to aid particle removal. Recall that acidic solutions typically result in a weak positive zeta potential; therefore, some enhancement is needed for acceptable particle removal. Carboxylates tend to be good complexing agents for Cu [77]. Ammonia is added to adjust the pH. Other products are mixtures of carboxylic acid complexing agents in water. In general, as seen in Section 11.3.3, carboxylic acids are good complexing agents for metals.

Reliability of the surface after post-CMP cleaning is critical. Yamada [42] investigated the impact on TDDB of several post-CMP cleaners (acidic and alkaline), with and without a BTA passivation step. They found that the growth (alkaline clean) or regrowth (acidic clean) of a non-uniform $CuO_x$ passivation layer during the rinsing step was leading to TDDB degradation. TDDB degradation was observed in the case of acidic post-CMP cleaning without BTA passivation step, explained in terms of non-uniformity of the $Cu/CuO_x$ surface. Also, TDDB degradation was suggested to originate from the emission of Cu ions by electrochemical reaction with oxygen and moisture [80] during queue time [81, 82]. Impurities and copper ions left over on the patterned features can lead to the formation of a leakage path between adjacent Cu lines during subsequent thermal processes which are sources of early dielectric failure [83].

Formulated products for post-CMP cleaners will continue to evolve. Some Cu inhibitors (*e.g.* BTA) and surfactants interfere with selective Cu plating of capping layers (*e.g.* CoWP) and cannot be used for those technologies [60, 84]. Numerous alternatives are available to deal with galvanic corrosion, deposition interference, and non-galvanic corrosion of the new materials being introduced. Introduction of cleaning functions in the polish process (*e.g.* buff with cleaning products instead of slurry) has eased the burden on post-CMP cleaning and has proven to provide cleaner, particle-free, hydrophilic, passivated Cu surfaces, the goal from the beginning.

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# 12

# Germanium Surface Conditioning and Passivation

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*Abstract*
Germanium is a candidate to replace silicon as channel material for the gate electrode. Due to the aqueous solubility and the thermal instability of $GeO_2$, cleaning solutions commonly used for Si are ineffective and must be adapted to this material. Hydrogen passivation of the Ge surface, as compared to Si, is more difficult to achieve and the H-terminated Ge surface is very unstable. Various methods are being used to stabilize the Ge surface; such as, oxidation of the Ge to stoichiometric $GeO_2$, oxynitridation, and even nitridation of the Ge substrate. Oxide-free Ge-surfaces can also be achieved by using HCl or other treatments, but even these are prone to reoxidation. Sulfur-containing passivation is shown to prevent interaction of the Ge channel with the $HfO_2$ gate. Metal and particle removal can be achieved using highly diluted cleaning solutions. This chapter discusses the various methods to passivate the surface and the surface analysis results.

*Keywords:* germanium, hydrogenation, oxidation, (oxy)nitridation, surface passivation, sulfur passivation, germanium passivation

## 12.1 Introduction

### 12.1.1 Germanium Use in Integrated Circuit Transistors

John Bardeen, Walter Brattain, and William Shockley received the Nobel Prize in 1956 for their research on semiconductors and their discovery of the transistor effect. The first transistor was made in 1947 of germanium. Germanium brought science another Nobel Prize; in 2000, Jack Kilby received the Nobel Prize in Physics for his invention of the integrated circuit. He focused his work on Ge. Despite these advances, Ge was replaced by Si in the 1960's. One of the major drawbacks of Ge is the high water solubility and thermal instability of its oxide ($GeO_2$). In that respect, Si and $SiO_2$ outperform Ge and $GeO_2$. However, progress in semiconductor science called for the reduction of device dimensions allowing a higher density of transistors on a chip. Consequently, the continuous downscaling

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of the device dimensions raised the need for replacing $SiO_2$ with a high-κ (high dielectric constant) material in the late 1990's. Hafnium oxide ($HfO_2$) and other Hf-based films have been introduced as the new gate dielectric material for high performance microprocessors [1]. However, the advantage of using Si because of its superior oxide properties is no longer applicable, opening new possibilities for other substrate materials. The main reason for switching back to Ge is the higher electron, and in particular, the higher hole mobilities compared to Si [2].

The Ge processing can be performed in a Si processing line, but the processes must be fine-tuned to take into account some peculiarities associated with the Ge technology that require alternative approaches for wafer cleaning, surface passivation, shallow junction formation, and contact technology. This has triggered a world-wide research activity to investigate the potential of Ge for future 22-nm and below technologies. The feasibility to use the Czochralski crystal growth technique to fabricate 300-mm Ge substrates has been demonstrated, but thin Ge films on a Si substrate such as Ge-on-Si and Ge-on-oxide have a greater potential. Different fabrication approaches such as wafer bonding, epitaxial growth, and Ge condensation have been successfully explored and optimized.

Besides its potential for scaling, Ge may also be used for the fabrication of alternative devices such as nanowires, tunnel field effect transistors (FET), and quantum dot single-electron transistors. Germanium was historically the semiconductor material at the beginning of the microelectronic revolution, and may be the emerging material for future devices as the microelectronic roadmap continues.

### 12.1.2 Gate Stack Interface Preparation and Passivation

Metal-oxide-semiconductor field-effect transistors (MOSFET) incorporating Ge channels are an attractive option for increasing complementary MOS (CMOS) logic performance since Ge offers bulk electron (and hole) mobilities approximately three times higher than Si [3]. Arguably, the main issue that has prevented the fabrication of competitive Ge-based devices is the poor electrical quality and low chemical stability of $GeO_2$ gate dielectrics on Ge as compared to $SiO_2$ on Si. With the recent advent of production-worthy hafnium-based high-κ gate dielectrics ($HfO_2$ or HfSiON) for Si-based CMOS logic for 45- and 32-nm devices [1], such deposited dielectrics offer new opportunities for Ge-channel devices as well. In this chapter the current knowledge regarding the impact of surface pretreatment prior to high-κ deposition on the electrical quality of Hf- and Al-based dielectrics on Ge will be discussed.

### 12.1.3 Need for Passivation

High mobility channel materials such as Ge and III/V have gained much interest because of their promising bulk mobilities compared to Si. However, the surface of the semiconductor does not reflect these bulk properties because there is a sharp rupture of the original bulk crystal that creates dangling bonds. These dangling bonds are responsible for the presence of interface states in the band gap that will trap carriers resulting in a drop in mobility. To achieve successful passivation these broken covalent bonds must be removed. One method to restore these bonds is to

adsorb a hetero atom [4]. However, the valence of this atom should be such that it can eliminate unpaired electrons at the surface; in the case of Ge(100), removal of the unpaired electrons would create a defect free bandgap [5]. Nevertheless, the deposition of the high-κ will again change the charge distribution in these surface bonds and can create interface states. Therefore, both the surface preparation and the choice of the high-κ will play a crucial role in the passivation process.

## 12.2 Germanium Cleaning

Several methods of Ge surface cleaning have been reported in literature. Sputtering with $Ne^+$ and $Ar^+$ was one of the initial cleaning procedures [6, 7]. Because sputter damage occurs inducing surface roughness, subsequent annealing is required [8]. An alternative way of cleaning is by forming a passivation layer that can be thermally desorbed in ultra-high vacuum (UHV). The most commonly used passivation layer is $GeO_2$. The cleaning procedures differ for the preparation of this passivation layer; options include wet chemical oxidation with $H_2O_2$ [8–12] and dry oxidation with $O_2$ or UV/$O_3$ (ultraviolet)/ozone) [8, 10, 13]. Cleanliness is specified in terms of producing epitaxial deposition-ready Ge surfaces. However, at the time of publication, no reports have been found on cleaning Ge surfaces with respect to metallic and particle contamination. In order to remove metallic and particle contamination, highly diluted cleaning mixtures have been introduced.

For Si-based technology, most surface conditioning and cleaning procedures are based on wet chemical treatments [14–16]. In this section, wet chemical cleaning procedures for the removal of metallic and particle contamination from Ge surfaces are discussed. However, before discussing cleaning procedures in wet chemistries, the compatibility of Ge is covered.

### 12.2.1 Wet Chemical Compatibility and Etching Rates: A Historical Perspective

The main difference between Ge and Si with respect to wet chemical compatibility is the difference in stability of their native oxides in water. At the electro-potential-pH equilibrium, also called the Pourbaix diagram, for the Si-$H_2O$ system at 25°C, it is clear that the stable form of Si is $SiO_2$ over the entire pH range [17, 18]. For the Ge-$H_2O$ system at 25°C, $GeO_2$ will be formed in $H_2O$ over the entire pH range [19]. The Pourbaix diagram of the Ge-$H_2O$ system is shown in Figure 12.1.

At neutral pH both Si and Ge behave similarly $SiO_2$ is in equilibrium with dissolved $H_2SiO_3$ and $GeO_2$ with $H_2GeO_3$. The difference arises because at equilibrium $SiO_2$ is insoluble while $GeO_2$ is highly soluble. Laubengayer *et al.* reported three different $GeO_2$ phases: one amorphous and two crystalline (hexagonal and tetragonal) [20]. The amorphous and hexagonal phases are very soluble while the tetragonal phase has much lower solubility in water. The solubility of hexagonal $GeO_2$ is 4.53 g/l [21]. Naturally occurring $GeO_2$ is found as the hexagonal or amorphous phase. The solubility of the tetragonal phase of $GeO_2$ is <0.005 g/l; however, it does not naturally occur [22].

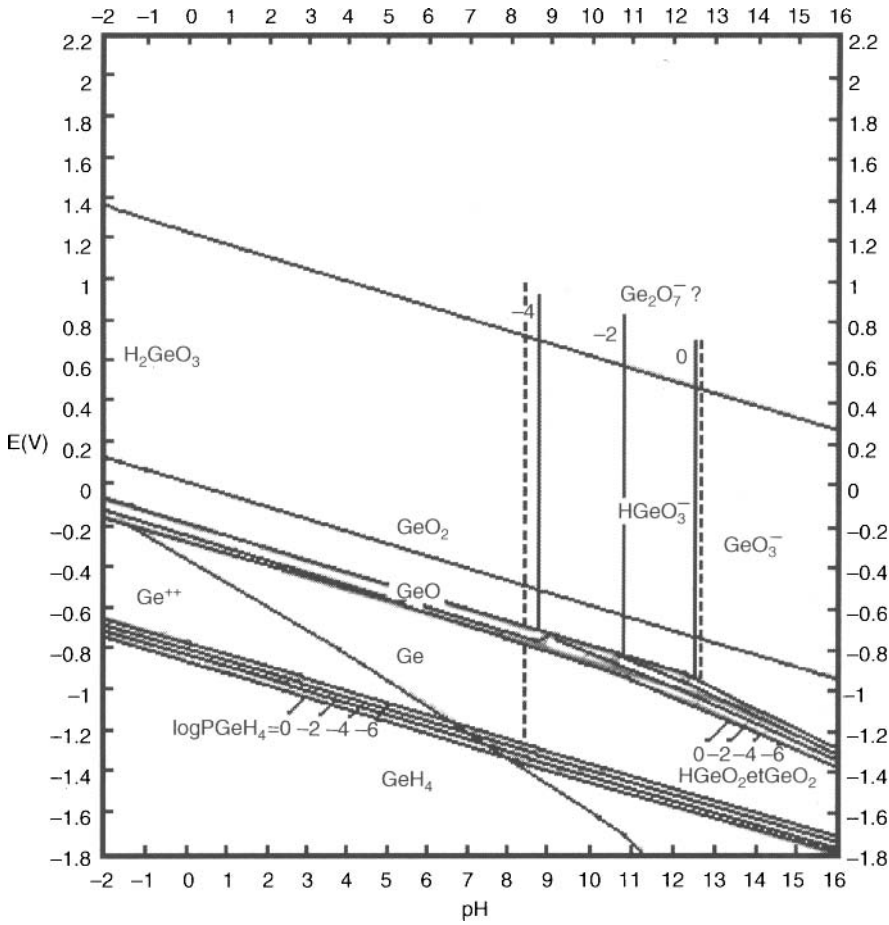


**Figure 12.1.** Potential-pH equilibrium diagram for the system germanium-water, at 25°C. Reprinted with permission from Pourbaix, M., *Atlas of Electrochemical Equilibria in Aqueous Solutions*, p. 468, National Association of Corrosion Engineers (NACE) International, Cebelcor, Houston, Texas (1974).

Early literature can be found on the etching behavior of Ge. Harvey *et al.* studied the dissolution of Ge in $H_2O$ containing dissolved oxygen [23]. They found the etching rate of Ge to be 0.018 nm/min for the <100> surface in air-saturated water at 30°C. When saturated with $O_2$, the etching rate was 0.022 nm/min, and in $N_2$-saturated $H_2O$ the etching rate is close to 0 nm/min. They concluded that in order to etch Ge dissolved $O_2$ is needed. Although the absolute values of recent etching rate results of Ge in $H_2O$ [24, 25] differ from the results reported by Harvey *et al.*, the trend is similar.

When adding an oxidizing agent ($H_2O_2$) to the solution, high etching rates can be obtained, as shown in Table 12.1. In 1962 Cerniglia and Wang [26] studied the dissolution of Ge in $H_2O_2$ containing solutions. They observed at concentrations of $H_2O_2$ between 3–30 wt%, the rate was largely dependent on the pH. At low pH, the rate is constant, but at a certain threshold pH, and depending on the concentration of $H_2O_2$, there is a steep increase. Both Batterman [27] and Camp [28] focused

**Table 12.1.** Etching rates of germanium.

| Reference | Chemistry | Surface Orientation | Etching Rate (μm/min) |
|---|---|---|---|
| Batterman [27] | $HF:H_2O_2:H_2O$ 1:1:4 with agitation at 30°C | <100> and <110><br><111> | 4.4<br>6.0 |
| Camp [28] | $HF:H_2O_2:H_2O$ 1:1:4 with agitation | <100><br><111><br><110> | 3.8<br>4.5<br>6.0 |
| Cerniglia and Wang [26] | $H_2O_2$ 30 wt% no agitation | <111> | 0.125 (pH = 3)<br>0.250 (pH = 7)<br>1.2 (pH = 9) |
| Primak [34] | $H_2O_2$ 1.5–3 wt% with stirring | <100><br><111> | 0.025 (pH = 5)<br>0.030 (pH = 5) |
| Ehman [30] | $x:H_2O_2:H_2O$ ($x$ = 0.75 M:1:4) with agitation (x = complexing agent) | <100> | 0.1–0.4 |
| Kawaga [31] | $H_3PO_4:H_2O_2:H_2O$ 4:1:5 no stirring at 30°C | <111><br><100><br><110> | 0.20<br>0.43<br>0.55 |
| | $H_3PO_4:H_2O_2:H_2O$ 1:6:3 no stirring at 30°C | <111><br><100><br><110> | 0.18<br>0.28<br>0.3 |

their study on the superoxol etchant; 1:1:4 HF (49 wt%):$H_2O_2$ (30 wt%):4 $H_2O$ [29]. Ehman *et al.* [30] studied the influence of the complexing agent in the system $x:H_2O_2:H_2O$, where $x$ could be tartaric, acetic, citric, oxalic acid, HF, HCl, or mannitol. He divided the complexing agents in two groups depending on the reaction mechanism – the agents that react in a 1:1 ratio with Ge and the agents that react in a 2:1 ratio (2 complexing atoms:Ge atom). A study of the $H_3PO_4:H_2O_2:H_2O$ system was carried out by Kawaga *et al.* [31]. Germanium etching by using $HNO_3$ as the oxidizing agent was studied by Schwartz *et al.* and Irving [32, 33]. As can be seen in Table 12.1, the etching rates studied have values in the order of 0.1 to >>1 μm/min. These etching rates are very high; however, for a suitable cleaning process, a lower etching rate is required.

### 12.2.2 Wet Chemical Compatibility and Etching Rates: Recent Results

Because the semiconductor industry is focused on Si processing, the etching chemicals targeting cleaning and surface conditioning for Si have been used on Ge. However, the difference in physical properties of $SiO_2$ and $GeO_2$ make this transfer impossible. The aqueous-based RCA cleaning process developed in the

1970's [35–37] is based on oxidizing Si to stabilize it in $H_2O$, and depending on the amount of $NH_4OH$ or HCl added, the Si etching rate could be very well controlled [14]. However, oxidizing Ge will make it highly soluble in $H_2O$ and adding a complexing agent yields very high etching rates. The original SC-1 (standard clean-1) solution consists of $H_2O$:$H_2O_2$:$NH_4OH$ at a ratio of 5:1:1 and at a temperature of 75–80°C. The removal rate of Si in this solution is 0.82 nm/min; however, Ge will be removed at a rate of 278 nm/min at room temperature [25]. The original SC-2 (standard clean-2) solution consists of $H_2O$:$H_2O_2$:HCl at a ratio of 6:1:1 at a temperature of 75–80°C. A comparable ratio 7:1:1 of this solution etches Ge at ~200 nm/min at room temperature [25]. Unfortunately, these etching rates are too high for effective cleaning of Ge and research is ongoing to design new etching processes.

Etching rates for Ge <100>, tabulated for several chemistries, are reported in Table 12.2 [25]. The values are expressed in nm/min, and the detection limit is calculated based on the longest dip time in the solution. The etching rates for both SC-1 and SC-2 at their original concentrations are unacceptably high for cleaning applications. By diluting the oxidizing agent by a factor of 1000, the etching rate is reduced by a factor of 100. For example, the 5:1:1 SC-1 solution has a rate of 275.5 nm/min, and the diluted 50000:10:1 SC-1 solution has a rate of 1.26 nm/min. Depending on the application, addition of $NH_4OH$ or HCl to modify the pH of the solution is possible. The etching rate is less dependent on these complexing agents than on the oxidizing agent [24]. When no oxidizing agent is added, most of the solutions do not etch or slowly etch the Ge substrate.

### 12.2.3 Metal Deposition on Germanium

Even though a thorough assessment of the etching rates for germanium has been performed, additional understanding of the removal process and chemicals for metallic, organic, and particulate contamination is needed. Therefore, the deposition behavior of metals will be discussed in this section, and a comparison will be made to silicon.

Extensive studies pertaining to metal contamination deposition on Si can be found [38, 39] and is thoroughly discussed in [40]. It was known that the surface contamination depends on the available surface sites for metal adsorption. Surface silanol groups exchange $H^+$ with metal ions according to:

$$\text{Si-OH (s)} + M^{n+}\text{ (aq)} \leftrightarrow \text{Si-O}M^{(n-1)+}\text{ (s)} + H^+\text{ (aq)} \qquad (12.1)$$

This mechanism is described by several groups [41–44]. The maximum number of surface sites on a $SiO_2$ surface is less than $8 \times 10^{14}$ /cm$^2$. The pH plays a major role in the surface adsorption of metal ions on the Si surface, as shown in Equation 12.1. Using this reaction, the adsorption behavior of metal ions on the Si surface is described by the Langmuir adsorption isotherm [44]:

$$\sigma_{surface} = \frac{K\left[M^+\right]\cdot\sigma_0}{\left[H^+\right]+K\cdot\left[M^+\right]} \qquad (12.2)$$

**Table 12.2.** Etching rates of germanium using different chemistries [25]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Brunco, D. P., Meuris, M., Uwamahoro, O., Van Steenbergen, J., Vrancken, E., and Heyns, M. M., *ECS Transactions*.

| Chemistry | Wafer Type | Etching Rate (nm/min) | DL (nm/min) |
|---|---|---|---|
| SC-1 $H_2O$:$H_2O_2$:$NH_4OH$ | | | |
| 20:4:1 | P | 420 | 0.8 |
| 20:4:1 | N | 390 | 0.8 |
| 5:1:1 | P | 275.5 | 0.6 |
| 500:10:1 | P | 99.7 | 0.6 |
| 5000:10:1 | P | 34 | 0.1 |
| 5000:10:1 | N | 29 | 0.1 |
| 500:1:10 | P | 25 | 0.6 |
| 50000:1000:1 | P | 14.1 | 0.2 |
| 5000:1:1 | P | 4.8 | 0.1 |
| 5000:1:10 | P | 2.63 | 0.2 |
| 5000:15:1 | N | 2.18 | 0.2 |
| 1000:0.1:1 | N | 1.35 | 0.08 |
| 50000:10:1 | P | 1.26 | 0.2 |
| 5000:1:1000 | P | 1.23 | 0.01 |
| 2778:0.1:1 | N | 0.63 | 0.1 |
| 1667:0.1:1 | N | 0.26 | 0.08 |
| SC-2 $H_2O$:$H_2O_2$:HCl | | | |
| 7:1:1 | N | 229 | 0.8 |
| 7:1:1 | P | 155 | 0.8 |
| 100:2:1 | N | 93.8 | 0.2 |
| 10000:200:1 | N | 91.6 | 0.2 |
| 1000:2:1 | N | 23 | 0.2 |
| 1000:2:1 | P | 10 | 0.2 |
| 5000:10:1 | P | 9.81 | 0.2 |

**Table 12.2. (cont.)** Etching rates of germanium using different chemistries [25]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Brunco, D. P., Meuris, M., Uwamahoro, O., Van Steenbergen, J., Vrancken, E., and Heyns, M. M., *ECS Transactions*.

| Chemistry | Wafer Type | Etching Rate (nm/min) | DL (nm/min) |
|---|---|---|---|
| 5000:1000:1 | P | 9.67 | 0.2 |
| 10000:20:1 | P | 8.87 | 0.2 |
| 5000:1:50 | N | 3.7 | 0.2 |
| 1667:1:15.3 | P | 3.56 | 0.2 |
| 10000:1:1 | N | 3.3 | 0.2 |
| Other Chemistries | | | |
| HCl 0.1 M | P | 0.003 | 0.01 |
| HCl 1 M | N | 0.003 | 0.001 |
| | P | 0.004 | 0.003 |
| $H_2SO_4$ concentrated | P | 0.016 | 0.006 |
| $HNO_3$ 0.5 M | | 0.0022 | 0.001 |
| $HNO_3$ 1 M | P | 0.004 | 0.001 |
| $HNO_3$ 0.1 M | P | 0.14 | 0.013 |
| $HNO_3$ 0.01 M | P | 0.15 | 0.009 |
| $H_3PO_4$ concentrated | P | 0 | 0.0004 |
| HF 10 wt% | | 0 | 0.001 |
| BOE 7:1 ($NH_4F$:HF) | N | 0 | 0.014 |
| | P | 0.06 | 0.014 |
| $NH_4OH$ 1 M | N | -0.598 | 0.011 |
| | P | -0.5155 | 0.011 |
| $NH_4OH$ pH = 9 | P | 0.02 | 0.01 |
| $NH_4OH$ pH = 10 | P | 0.02 | 0.001 |
| $NH_4OH$ pH = 11 | P | 0.29 | 0.007 |
| $H_2O$ | P | 0.0065 | n/a |
| | N | 0.0053 | n/a |
| $H_2O$ (bubbling $N_2$) | N | 0 | n/a |
| $H_2O$ (bubbling $O_2$) | N | 0.005 | n/a |
| $H_2O$ (bubbling $O_3$) | N | 4 | n/a |

**Table 12.2. (cont.)** Etching rates of germanium using different chemistries [25]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Brunco, D. P., Meuris, M., Uwamahoro, O., Van Steenbergen, J., Vrancken, E., and Heyns, M. M., *ECS Transactions*.

| | | | |
|---|---|---|---|
| $H_2O$ 70°C | P | 0.192 | 0.019 |
| | N | 0.096 | 0.019 |
| Mixtures | | | |
| 1:1:1 HF:$HNO_3$:$H_2O$ | P | 717 | 0.2 |
| 3: 1 HCl:$HNO_3$ | P | 149 | 0.1 |
| 10:1 $H_2O$:$H_2O_2$ | N | 20.8 | 0.8 |
| | P | 12.5 | 0.8 |
| 500:1 $H_2O$:$H_2O_2$ | P | 6.8 | 0.2 |
| 1667:1 $H_2O$:$H_2O_2$ | P | 4.38 | 0.2 |
| 3:1 $H_3PO_4$:$HNO_3$ | P | 3.4 | 0.04 |

Where $[M^+]$ and $[H^+]$ are the concentrations of metal and hydrogen ions, respectively, and $\sigma_0$ denotes the total amount of available adsorption sites, unoccupied and occupied by ions. The factor $K$ is the ratio of the equilibrium constants of metal and hydrogen adsorption where:

$$K = K_{M^+} / K_{H^+} \tag{12.3}$$

An investigation showed that a similar mechanism for Ge occurs and predicts lower metal deposition at low pH values [45]. However, metal deposition behavior for Ge is different from Si, whereas on Si, the deposition is governed by the pH, as described in Equation 12.2. Figure 12.2 shows the comparison between the metal deposition behavior for Cr ions on a) Si and b) Ge surfaces. As can be seen in the graphs, the deposition of metal ions on Ge is not dependent on the pH of the bath. Also for Si, the deposition is limited by the surface reaction, thus at high bath loading, the surface reaction sites are saturated. On the other hand for Ge, at low bath loading, the deposition is governed by the diffusion of the metal ions in the solution; all metal ions reaching the surface will react and deposit. Eventually, at higher loading the deposition becomes reaction limited. These results indicate that metal removal will be more difficult from a contaminated Ge surface than a Si surface.

## 12.2.4 Metal Removal from Germanium

In order to remove metals from the Si surface, the SC-1 and SC-2 cleaning processes were developed [35, 36] and an overview is given in [46]. Another concept

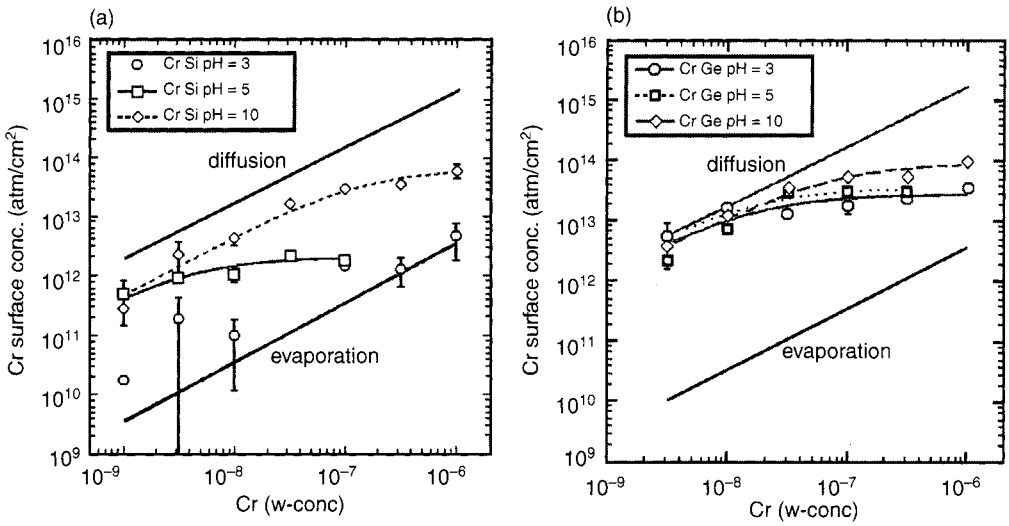


**Figure 12.2.** Metal deposition behavior on a) Si and b) Ge for Cr atoms from baths at different pH values. The straight lines depict the diffusion and evaporation limits which describe the maximum and minimum levels that can be achieved starting from a bath with a certain ion concentration [45]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Onsia, B., Struys, K., Rip, J., Vos, R., Meuris, M., Mertens, P., and Theuwis, A., *Electrochemical Society Transactions*.

was introduced by Meuris *et al.* This process removes metals and particles for the Si surface with low losses of substrate material [15].

For Ge, removing metals and particles is still under investigation. Removal of metals was studied in several cleaning mixtures: SC-1, HCl, and HF [45]. Figure 12.3 shows the metal contamination levels after using SC-1 cleaning mixtures. Several metals were tested: K, Ni, Zn, Ca, Fe, Cr, and Ti. The metal removal is divided in two categories: Ni, Zn, and Ca that are hard to remove, and Ti, Fe, and Cr that are easier to remove. For Ni, Zn, and Ca, the contamination on the wafer is constant as a function of etching depth and drops at a certain threshold. An etching depth of 25 nm is needed to reduce the initial contamination by a factor of 100. Titanium, Fe, and Cr are easier to remove in SC-1 solutions; the contamination drops gradually as a function of etching depth. About 10-nm substrate removal is sufficient to reduce the metal contamination level by a factor of 100. However, 10-nm of substrate loss is unacceptable.

Figure 12.4 shows the removal of metals in solutions at low pH and in HF-containing solutions [45]. The pH was varied between 1 and 5.7 by adding HCl. Different HF concentrations were tested between 0.5 and 5 wt%. Figure 12.4a shows that at lower pH values lower contamination levels can be reached; however, complete removal is not achieved. This could be expected from the deposition behavior; the deposition of Cr was minimally effected by the pH. Figure 12.4b shows that by using 5 wt% HF to remove the metal contamination, all metal contamination could be reduced by a factor of 100, and most metal levels are below the detection limit. Results from Table 12.2 show that HF does not etch the Ge surface – etching rates are <0.01 μm/min. Thus, complete metal removal can be achieved using HF without etching the substrate.

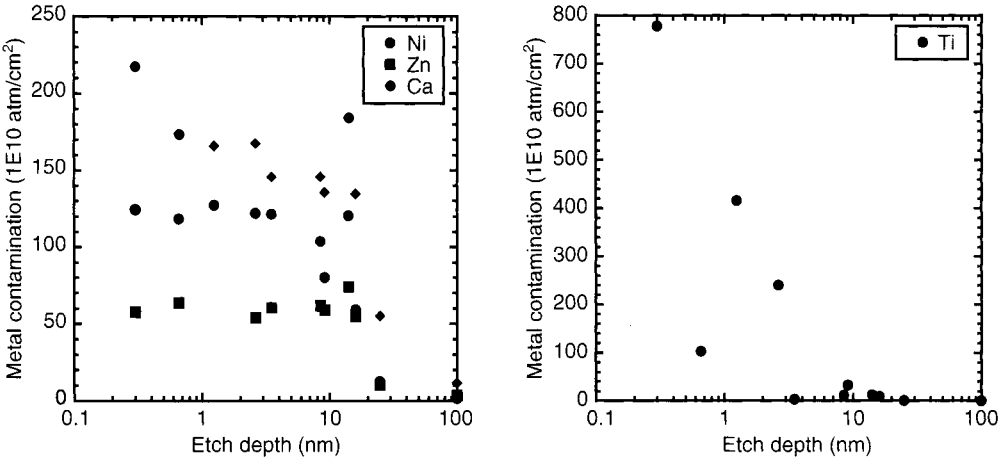


**Figure 12.3.** Metal contamination after using SC-1 cleaning mixtures as a function of etch depth; a) metal contamination level of Ni, Zn and Ca on the Ge wafer and b) metal contamination level of Ti on the Ge wafer [45]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Onsia, B., Struys, K., Rip, J., Vos, R., Meuris, M., Mertens, P., and Theuwis, A., *Electrochemical Society Transactions.*

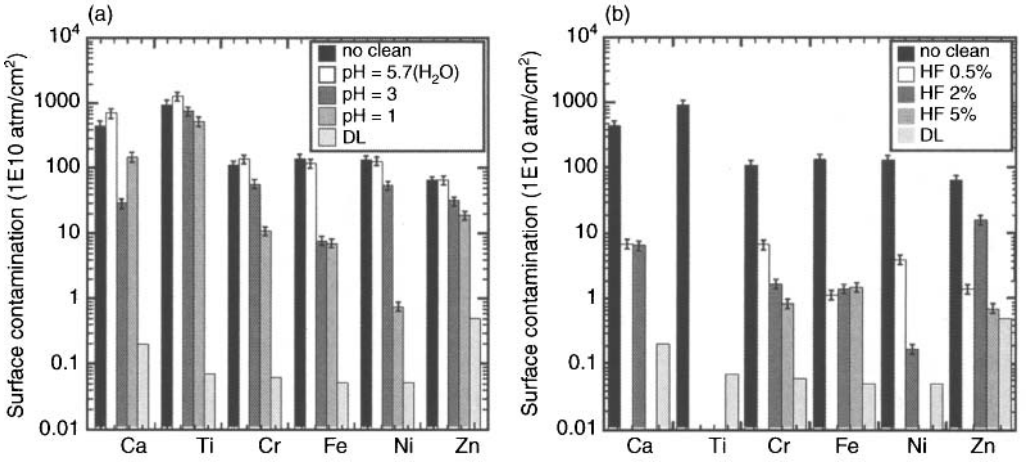


**Figure 12.4.** Metal contamination after dipping Ge wafers in a) acidified solutions and b) HF-containing solutions. The pH was varied by adding HCl to the bath. Hydrofluoric acid concentrations were varied between 0.5 and 5 wt%. The dip time was 5 minutes [45]. Reproduced with permission of ECS – The Electrochemical Society from Sioncke, S., Onsia, B., Struys, K., Rip, J., Vos, R., Meuris, M., Mertens, P., and Theuwis, A., *Electrochemical Society Transactions.*

## 12.2.5 Particle Deposition on Germanium

In contrast to metal deposition and removal, Ge exhibits comparable particle deposition and removal properties towards Si. This originates from the fact that the Ge surface shows an isoelectric point around pH = 2 similar to what is found for Si surfaces [47]. The data were collected from zeta potential measurements on Ge particles. Particle deposition behavior was studied for silica

and alumina particles on Ge [47]. Two regions for particle deposition can be distinguished:

1. The region where van der Waals interactions govern the deposition.
2. The region where electrostatic interactions are dominating the interaction between the particles and the surface.

Below pH = 2 and above pH = 12, van der Waals forces are dominant and deposition of the particles occurs because these forces are always attractive. Between pH = 2 and 12, the electrostatic interactions are dominant, and in this region the behavior of alumina and silica particles reflects the zeta potential of the Ge surface.

As shown in Figure 12.5, the silica deposition is a function of pH [47]. The particle deposition is expressed in terms of normalized surface concentration *i.e.* the ratio of particle surface density and the initial particle concentration in the solution. The expression corresponds to the thickness of the diffusion boundary layer; the distance over which diffusion takes place in the time frame studied. The pH of the solutions was varied by adding HCl or NaOH. Below pH = 2, particle deposition occurs due to van der Waals attraction. Above pH = 2, no particle deposition occurred. Since silica particles are negatively charged above pH = 2, this indicates that the Ge surface also exhibits a negative charge above pH = 2.

In Figure 12.6 [47], alumina particle deposition as a function of dip time is shown. The particle deposition is expressed in percentage of surface coverage. The deposition is studied at several pH values ranging between pH = 2 and 9. Figure 12.6 shows that diffusion-limited deposition occurs between pH = 2 and 8.5. Because of electrostatic attraction the alumina particles are positively charged in this pH region. At pH = 9, alumina particles are negatively charged and electrostatic repulsion is observed. These observations indicate that the Ge surface is negatively charged between pH = 2 and 9.

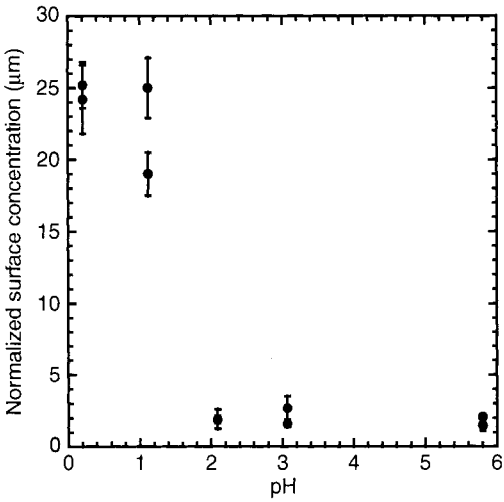


**Figure 12.5.** Normalized surface concentration of silica particles on the Ge surface as a function of pH [47]. The immersion time is 120 seconds. Used with permission of IMEC.

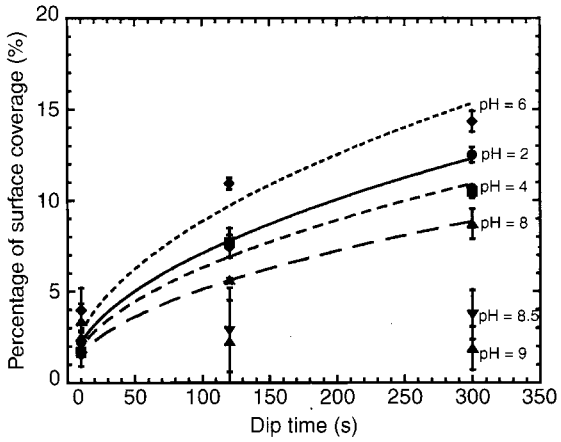


**Figure 12.6.** Relative surface coverage as a function of immersion time at different pH values of alumina particles [47]. Straight and dotted lines represent fittings based on diffusion limited deposition. Used with permission of IMEC.

## 12.2.6 Particle Removal from Germanium

When no physical forces are used, particle removal can only be achieved by undercutting the particle by etching the underlying film to overcome the van der Waals forces and thus detach it from the surface [15, 48]. Once the particle is detached, redeposition can be prevented by tuning the pH of the solution. Depending on the particles to be removed, the particle removal efficiency (PRE) is a function of etching depth and pH. In Figure 12.7 PRE is shown for silica particles using

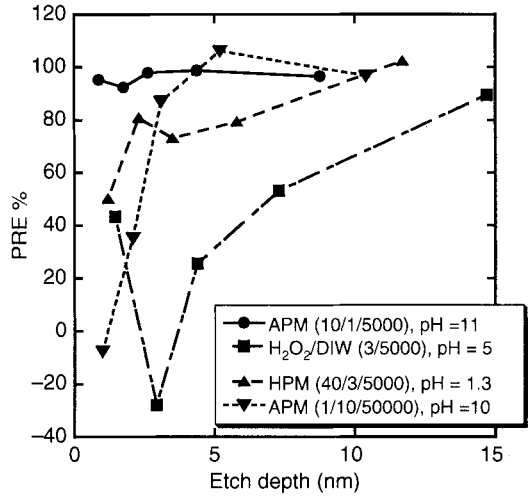


**Figure 12.7.** Particle removal efficiency of silica particles from Ge using • APM (SC-1) (5000:1:10) ▼ APM (50000:10:1) ■ $H_2O_2$/DIW (3:5000), and ▲ HPM (SC-2) (5000:3:40) [47]. All solutions have an etching rate ~3 nm/min except APM (50000:10:1), which etches at a rate of 1.3 nm/min. APM is ammonium hydroxide hydrogen peroxide mixture and HPM is hydrochloric hydrogen peroxide mixture. Used with permission of IMEC.

solutions at different pH values but with the same etching rate [47]. The PRE is plotted as a function of etch depth. Except for the $H_2O_2$/DIW (deionized water) solution, all solutions show a good PRE as a function of etching depth. At high pH repulsion forces are present between the silica particles and the Ge surfaces. An etching depth of 3 nm is sufficient to detach the particles from the surface. This corresponds to earlier reports on Si [15, 48].

Particle removal from Ge surfaces is comparable to Si surfaces since both substrates have an isoelectric point around pH = 2. Using only chemical cleaning, an etching depth of 3 nm is needed to remove particle contamination from the Ge surface. For blanket substrate cleaning, this would be sufficient. With more stringent conditions for material loss required for Si processing other cleaning solutions are used to remove particles as well as physical forces. However, physical forces have not yet been explored for particle removal from Ge. Using megasonic energy, spray technology, or brush scrubbing potentially could yield good particle removal with minimal substrate loss.

## 12.3 Surface Passivation and Gate Stack Interface Preparation

In this section, germanium surface passivation processes are reviewed; the properties of the passivation layer as well as their implementation in high-κ gate stacks. First, the lower thermodynamic stability of native oxides on germanium compared to silicon, which has important implications for high-κ/channel interfacial layer thickness and stability are discussed. Then, the current knowledge for the leading germanium passivation methods oxidation, nitridation and oxynitridation, hydrogenation, chlorination, sulfur passivation, and silicon passivation are reviewed. A good review of germanium in gate stacks is given in [49].

### 12.3.1 Thermodynamic Stability of Native Oxides

Germanium dioxide ($GeO_2$) is thermodynamically less stable than $SiO_2$, when comparing its smaller standard Gibbs energy of formation at room temperature to Si ($GeO_2$: −261 kJ/mol; $SiO_2$: −428 kJ/mol, per O atom [50]). This plays an important role in gate stack formation as it determines the thermodynamic tendency for native oxide formation during high-κ deposition or subsequent thermal processing. On Si, interfacial $SiO_2$ is usually observed at the channel/high-κ interface even if initially oxygen-free H-passivated Si surfaces are used. Silicon oxidation is caused by the precursors during the growth process [51–53] though such oxidation can be kinetically hindered at sufficiently low growth temperatures [54] and/or by excess oxygen in the high-κ layer, such as the formation of hydroxyl groups during high-temperature processing [55]. Given the lower thermodynamic driving force for $GeO_2$ formation, less interfacial native oxide is expected on Ge channels under similar processing conditions.

### 12.3.2 Oxidation

Germanium oxide is chemically more complex and less stable than silicon oxide. All soluble and insoluble phases have been studied using Raman and infrared (IR) absorption spectroscopy [56, 57]. The characteristic fingerprints, the longitudinal [Im(-1/ε)] and transversal [Im(ε)], where ε is the complex dielectric function of the medium, optical modes of $GeO_2$, have been identified at 857 and 930 $cm^{-1}$ (Figure 12.8).

X-ray photoelectron spectroscopy (XPS) has also been used to identify the various oxidation states upon oxidation of Ge(100) and Ge(111) surfaces under UHV

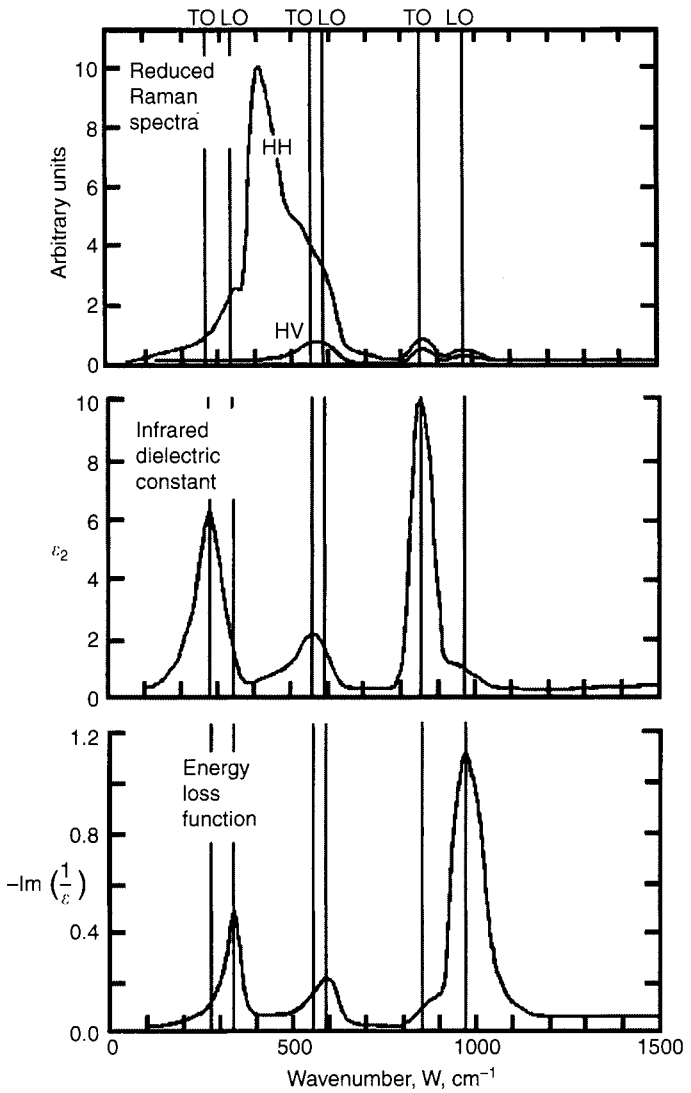


**Figure 12.8.** Comparison of reduced Raman spectra of bulk v-$GeO_2$ with the experimentally determined transverse energy loss function, $\varepsilon_2$, and the longitudinal energy loss function Im(-1/ε) [57]. Reprinted figure with permission from Galeener, F.L. and Lucovsky, G., *Phys. Rev. Lett.*, 37(22):1474 (1976). Copyright 1976, American Physical Society.

conditions [58–60] showing the formation of a +2 oxidation state. Schmeisser *et al.* [60] have discussed the stability of Ge oxides and compared it to that of oxides of other elements close to Ge. Prabhakaran *et al.* [10, 12] combined UV photoemission spectroscopy (UPS) with XPS to compare the formation and removal of oxides on Ge(100) and Ge(111) using wet chemical treatments and *in situ* oxidation (*i.e.* by introducing oxygen gas directly into the UHV chamber). Focusing on the Ge3d, Ge2p and O1s core levels, they showed that a cleaning procedure involving a sequential treatment in DIW, hydrofluoric acid (HF) and hydrogen peroxide ($H_2O_2$:$H_2O$) leads to the formation of both GeO (in a non-bridged configuration) and $GeO_2$ (Figure 12.9).

This comprehensive study shows that *in situ* oxidation in UHV results in mostly GeO and some related sub-oxides, wet chemical oxidation leads to the formation of a mixture of GeO/$GeO_2$ and sub-oxides, and native oxidation in room air produces primarily $GeO_2$. Most of the Ge sub-oxides are not water soluble and thermally more stable than $GeO_2$ requiring annealing temperatures above 450°C for removal. Zhang *et al.* [13] confirmed these findings by showing that water immersion of 1-2-nm-thick native oxide leaves behind only a 1-2 Å thick film of GeO. They showed that $GeO_2$ can be thermally removed in UHV leaving behind a clean, reconstructed Ge(100) 2×1 surface. They also showed that carbon contamination plays a crucial role because the Ge-C bond is very strong and difficult to break [13]. In fact, carbon contamination is present on the surface (observed through C1s core level in XPS) after any wet chemical treatment, and can only be removed after a 30 min UV/$O_3$ irradiation (Figure 12.10).

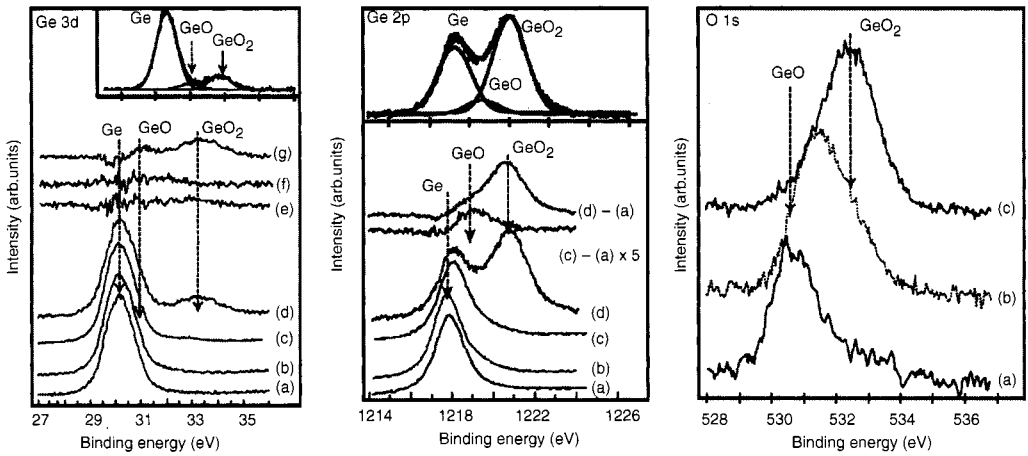


**Figure 12.9.** X-ray photoelectron spectroscopy of Ge3d (left panel), and Ge2p (middle panel) core level spectra of a) clean Ge(111), b) clean Ge(111) exposed to 100L $O_2$ at 250°C, c) *ex situ* oxide prepared by dipping the wafer in a mixture of $H_2O_2$ and $H_2O$ at room temperature, and d) clean Ge(111) exposed to clean room air for 6 hr. The difference spectra e) = (b–a), f) = (c–a), and g) = (d–a) are plotted for the Ge3d core level (left panel), and the fittings used for curves d) are shown as inset at the top of the left and middle panels. Data for O1s core level spectra (right panel) are for (a) clean Ge(111) exposed to 100L $O_2$ at 250°C, b) Ge(111) dipped in a mixture of $H_2O_2$ and $H_2O$ at room temperature, and c) Ge(111) exposed to clean air for 6h [10]. Reprinted from *Surface Science Letters*, Vol. 316(1), Prabhakarana, K., Ogino, T., Hull, R., Bean, J. C., and Peticolas, L. J., *"An efficient method for cleaning Ge(100) surface"*, page L1031. Copyright (1994) with permission from Elsevier.

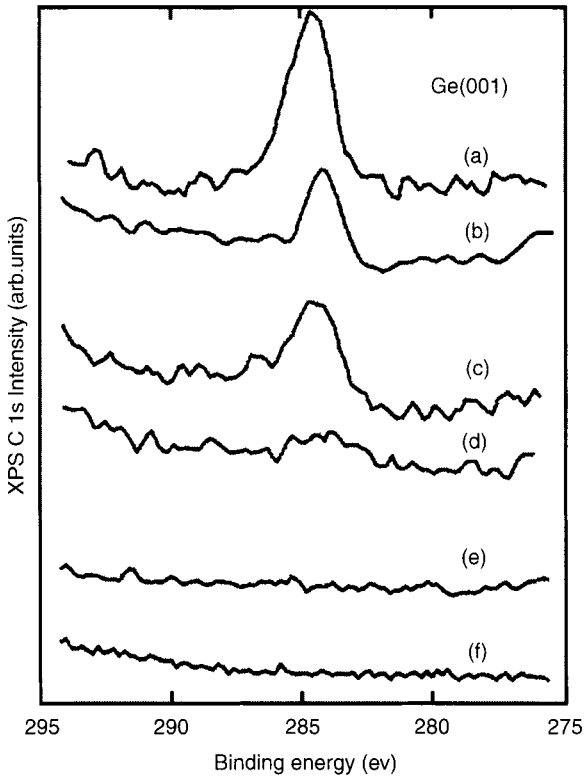


**Figure 12.10.** C1s core level XPS spectra from Ge(100) wafers after undergoing a) a degreasing step involving successive rinses of trichloroethylene, acetone, and methanol (process 1), b) process 1 followed by a thermal anneal to 620K, c) process 1 followed by an ultrasound rinse in DIW for 15 min (process 2), d) process 2 followed by a thermal anneal to 620K, e) process 2 followed by a 30 min $UV/O_3$ exposure (process 3) and f) process 3 followed by a thermal anneal to 620K [13]. Reprinted with permission from Zhang, X.-J., Xue, G., Agarwal, A., Tsu, R., Hasan, M.-A., Greene, J. E., and Rockett, A., *J. Vac. Sci. Technol.*, A11(5):2553 (1993). Copyright 1993, American Institute of Physics.

The ozone irradiation treatment leads to the formation of ~ 2 nm-thick $GeO_2$ including a 1.5 Å sub-oxide layer at the interface that is strongly dependent on the $UV/O_3$ exposure time [13]. This thickness is larger than after simple reoxidation of a clean Ge sample in air for 24 hr. Recent Fourier transfer infrared (FTIR) measurements show that a 30 minute $UV/O_3$ light produces an oxide similar to a 10-sec $H_2O_2$-grown oxide; $GeO_2$ is formed as evidenced by the appearance of $GeO_2$ longitudinal (LO, perpendicular) and transverse (TO, parallel) modes (Figure 12.11). Ultraviolet/ozone oxide tend to form more slowly than chemical oxides and does not show any Ge=O or $CH_x$ contamination [61]. In contrast, the oxide formed after 12 hr reoxidation in air is dominated by sub-oxides and $CH_x$ species with no dioxide (Figure 12.11a).

A recent FTIR and XPS study has examined the removal of oxides prepared by various chemical treatments on epi-ready Ge(100) [61]. The IR spectrum (Figure 12.12a) obtained after rinsing a native oxide (epi-ready and subsequent air exposure) in DIW shows the loss (negative absorption) of a broad absorbance feature in the 750–1050 $cm^{-1}$ range with a more intense negative component at

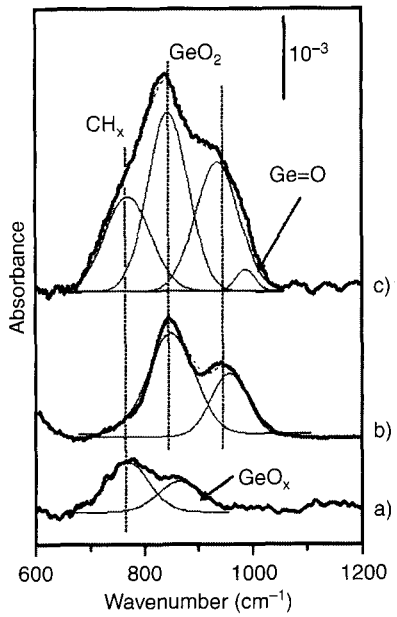


**Figure 12.11.** Transmission absorption IR spectra of germanium oxides formed a) after 90 min in air, b) after 30 min UV/$O_3$ exposure and c) after 10 sec in $H_2O_2$ (30 wt%). The reference spectrum is H/Ge(100) in all cases (see Section 12.3.4). Gaussian lines are used for the fitting. Unpublished results, used with permission from Chabal.

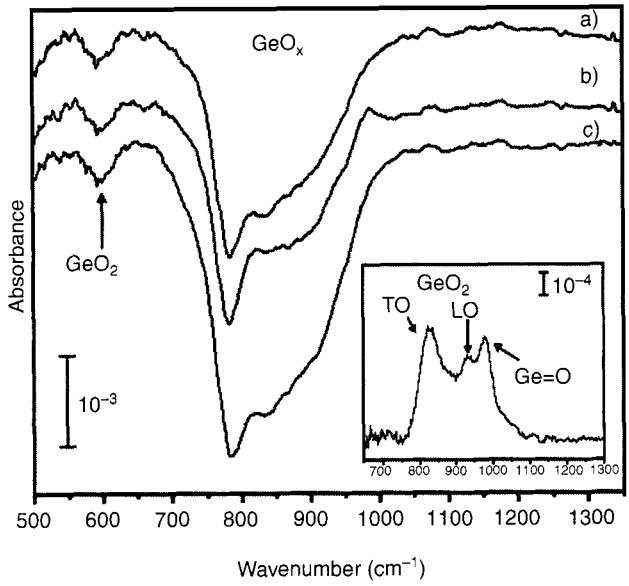


**Figure 12.12.** Transmission absorption IR spectra of Ge(100) after treatment in: a) DIW, b) DIW followed by 10 sec in $H_2O_2$. All the spectra are referenced to an as-received Ge(100) wafer. The insert shows the oxide region after $H_2O_2$ oxidation, using the $H_2O$-treated Ge(100) surface [61]. Reprinted with permission from Rivillon, S., Chabal, Y. J., Amy, F., and Kahn, A., *Appl. Phys. Lett.*, 87(25):3101 (2005). Copyright 2005, American Institute of Physics.

785 $cm^{-1}$. This region generally corresponds to germanium oxide, but the assignment is difficult because this band is wide and relatively featureless. The removal of this oxide in water suggests that it consists mostly of $GeO_2$ in either a hexagonal (solubility: 4.5 g/l) or amorphous (solubility: 5.2 g/l) phase (Figure 12.12) [61].

Further treatment in $H_2O_2$ leads to the growth of two components at 830 and 980 $cm^{-1}$ indicating the re-growth of an oxide (although the resulting oxide is thinner than the original native oxide since the overall integrated area is still negative). This new $H_2O_2$-grown oxide is also soluble in water suggesting that it is primarily composed of amorphous or polycrystalline $GeO_2$ [61]. By referencing this $H_2O_2$-grown oxide to the surface previously treated in water, as shown in the inset of Figure 12.12 corresponding to the difference of spectra b) and a), it is apparent that this newly formed oxide is characterized by three distinct components at 830, 940, and 980 $cm^{-1}$. Polarization studies have shown that the pair at 830 and 940 $cm^{-1}$ exhibits the proper dependence for the TO and LO optical phonon modes of $GeO_2$ (involving primarily the Ge-O-Ge asymmetric stretch mode) [56, 57]. The TO and LO modes associated with the Ge-O-Ge *symmetric* stretch are observable at 583 $cm^{-1}$ (weak shoulder) and 595 $cm^{-1}$ respectively. The third absorbance feature at 980 $cm^{-1}$ is assigned to germanium doubly-bonded to oxygen (Ge=O) [61].

Recent XPS data [61] confirm the presence of GeO and $GeO_2$ as previously established [12, 13]. Using a simple attenuation layer model and assuming a 15 Å mean free path for the photoelectrons, the total native oxide thickness is estimated to be ~ 15 ± 5 Å. The $GeO_2$ component completely disappears after DIW rinse and only GeO remains on the surface [61]. Longer rinse time in DIW does not remove GeO [62]. Hydrogen peroxide grows a mixture of GeO and $GeO_2$ oxides of thickness ~10 Å – very similar to the initial oxides present on the as-received substrates [62].

### *12.3.2.1 Gate Stacks on Oxidized Germanium*

The role of interfacial $GeO_2$ in high-κ/Ge gate stacks has been controversial. To rationalize the often poor electrical quality of gate stacks on Ge, it has frequently been claimed that $GeO_2$ is intrinsically of lower electrical quality than $SiO_2$. However, recent observations indicate that stoichiometric $GeO_2$ may be an acceptable interfacial layer as long as decomposition, the loss of oxygen or interfacial GeO formation and up-diffusion, is avoided [3, 63, 64].

For example, relatively low interfacial trap densities of ~$10^{11}$ $cm^{-2}$ $eV^{-1}$ can be achieved by forming stoichiometric $GeO_2$ *via* annealing the Ge surface in $O_2$ (1 atm, 350–450°C) prior to deposition of $Al_2O_3$ or $HfO_2$ [63]. Remaining concerns include significant charge trapping in the bulk of the gate dielectric, possibly due to high-κ/$GeO_2$ intermixing. Also, it is not clear whether such stacks can be scalable to the very low effective electrical thicknesses (<1 nm) required to be competitive with state-of-the-art silicon technology given that good interface passivation appears to require more than 1 nm, and preferably more than 2 nm, interfacial $GeO_2$ [63].

The importance of the choice of high-κ material and the thermal device process has recently been highlighted by Toriumi *et al.* [64]. They demonstrated that GeO formed at the $GeO_2$/Ge interface during thermal device processing at ~500°C tends to diffuse into and through the high-κ dielectric. While GeO diffuses easily in $HfO_2$, diffusion is reduced by $Y_2O_3$ and nearly prevented by $LaLuO_3$. In line with

this observation, electrical characteristics were found to be best with $LaLuO_3$ gate dielectrics.

In summary, $GeO_2$ may be an acceptable interfacial passivation layer for high-κ/Ge gate stacks, but scalability has yet to be demonstrated.

### 12.3.3 Nitridation and Oxynitridation

Nitridation of germanium surfaces has been investigated mostly because a thin nitride (or oxynitride) layer can effectively prevent Ge oxidation and Ge diffusion into high-κ dielectrics [65–72]. Nitride layers are grown primarily by exposure to ammonia gas, N-containing plasma, $NH_3$ or $N_2H_4$ exposure [68] and by N implantation.

Much of the early nitridation work was done in UHV initially at relatively low temperatures (exposure below room temperature) to investigate the chemisorption of $NH_3$ on clean Ge surfaces. At ~200K in UHV, there is evidence for molecular adsorption upon exposure of $NH_3$ on clean Ge(100) 2 × 1 as determined by XPS, UPS, as well as optical spectroscopy measurements. The modes related to $NH_3$ have been identified with high-resolution electron-energy-loss spectroscopy (HREELS) at 3270 (symmetric stretching mode), 1570 (asymmetric bending mode) and 1150 $cm^{-1}$ (symmetric bending mode) (Figure 12.13) [68].

Under these conditions, three adsorption regimes can be distinguished: monolayer, second layer and condensed multilayer [69]. Interestingly, as the temperature is increased to ~ 500K, ammonia is completely removed from the surface (Figure 12.14) [70]. Since there is no observable spectroscopic features related to $NH_2$ throughout the entire temperature range, it was concluded that $NH_3$ does not dissociate on Ge(100). This is in contrast to silicon where $NH_3$ does dissociate into $NH_2$ and H although it mostly recombines to desorb as $NH_3$ at higher temperatures. On Ge(100), $NH_3$ adsorbs initially on the electrophilic surface dimer atom (the atom lower in the dimer) and produces a (2 × 2) reconstruction because it adsorbs in a zig-zag fashion causing a flip of the dimer tilt direction of every second dimer row. In this HREELS study [70], germanium nitride could only be formed after electron irradiation at 110K as evidenced by the appearance of a component at ~800 $cm^{-1}$.

First-principles pseudo-potential calculations have confirmed that $NH_3$ dissociation into $NH_2$ and H on Ge(100) is not energetically stable [71]. Ammonia gas treatment performed at either room or high temperatures (up to 870K) does not form any nitride layer. Using relatively low pressures, XPS measurements confirm that less than $6.3 \times 10^{13}$ nitrogen atoms/$cm^2$ are observed on Ge(100) yielding an upper limit for the sticking (reaction) of $3 \times 10^{-6}$ [73]. This value is consistent with earlier studies [74] of $NH_3$ adsorption at 180K, which had derived a sticking coefficient < $10^{-4}$.

Nitridation requires higher pressures. Early work was performed on a thin evaporated (porous) germanium films. In the presence of low pressures of argon, ammonia was observed to dissociate on the Ge film even at room temperature [65]. Infrared experiments on Ge film show the presence of the Ge-$NH_2$ deformation mode in the 1550–1600 $cm^{-1}$ region and Ge-H stretch mode at 1920 $cm^{-1}$ consistent with dissociation into $NH_2$ and H. The weak Ge-H feature disappears after 17 hr

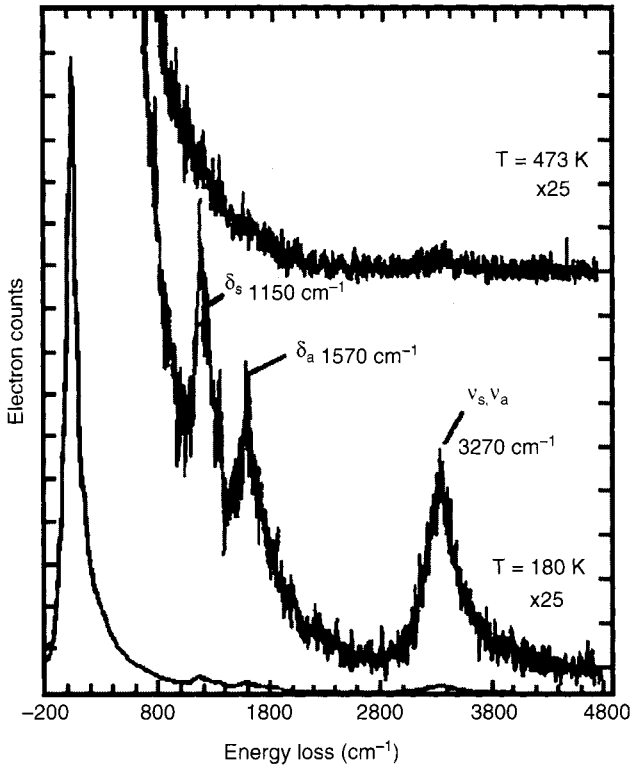


**Figure 12.13.** High-resolution electron-energy-loss spectra of $NH_3$ on Ge(100) 2 × 1. The lower curve shows Ge(100) exposed to 10L of $NH_3$ at T=180K. The upper curve was taken after annealing the sample at 473K for two minutes and then cooling the sample back down to 180K [68]. Reprinted from *Surface Science*, Vol. 330(1) and Tindall, C., and Hemminger J. C., *"HREELS studies of nitrogen hydrides on Ge (100): Formation of a surface nitride at low temperatures"*, page 67. Copyright (1995) with permission from Elsevier.

indicating that GeH is not as stable. The interpretation for the observation of $NH_2$, however, is different from simple $NH_3$ dissociation. The authors [65] suggest that at low exposure or in absence of $NH_3$ gas, the bonded hydrogen atoms recombine forming $H_2$ which is released. At higher exposures, $NH_3$ reacts with Ge-H forming Ge-$NH_2$ on the surface and releasing $H_2$(g) this explains why Ge-H stretching mode is weaker and observed only briefly. The mode observed at 1450 cm$^{-1}$ after many hours of $NH_3$ exposure is attributed to adsorbed $NH_4^+$. To explain the presence of this mode, Metcalfe [65] suggest either an ionic reaction between $NH_3$(g) and Ge-H forming so Ge-$NH_4^+$ (less probable due to the area of Ge-$NH_2$) or the possible reaction of $NH_3$ gas with water. Various studies have actually demonstrated that oxygen incorporation during the thermal nitridation is unavoidable and leads to the formation of an oxynitride on top of the germanium substrate [66, 75].

Using ellipsometry and optical micrography, Hua *et al.* [66] have shown that the growth of a smooth and uniform nitride film takes place at 870–930K in 2–4 hr on a hydrophobic germanium surface. They also observed an increase of the refractive index during the growth they attributed to the presence of oxide. The growth mechanism is dependent of the diffusion of the nitrogen and oxide

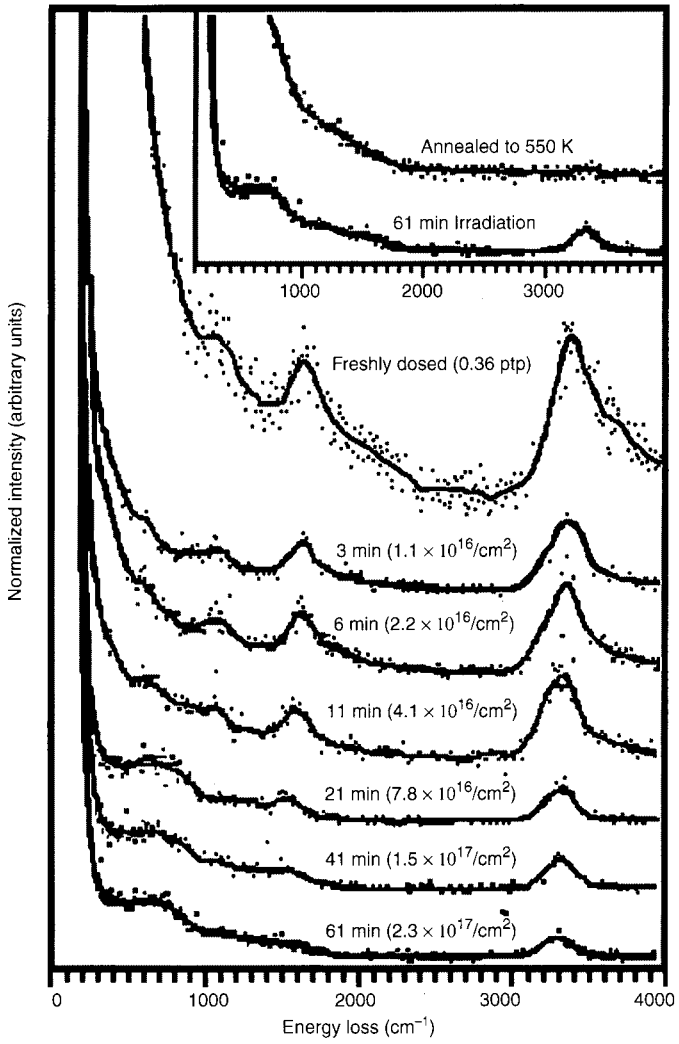


**Figure 12.14.** High-resolution electron-energy-loss spectroscopy spectra for ammonia adsorbed on Ge(100) 2 × 1 at 110 K after several exposure times [70]. Reprinted from *Applied Surface Science*, Vol. 171(3–4), Sanders, M. and Craig, Jr., J.H., *"HREELS study of electron irradiation effects on ammonia adsorbed on the Ge(100) surface"*, page 283. Copyright (2001) with permission from Elsevier.

into and through the film. However, when nitrogen gas is used instead of ammonia, there is no growth of a nitride layer indicating that $N_2$ does not dissociate. Finally, nitridation without oxygen incorporation or carbon contamination has been recently achieved using a plasma-enhanced nitridation technique [72]. Auger spectra show that a two-step cleaning procedure involving out-gassing at low temperature and thermal annealing at high temperature (870K) in UHV leads to the formation of a good quality nitride layer (1.6-nm thick) with a stoichiometry close to $Ge_3N_4$. Cross-sectional high-resolution transmission electron microscopy (HR-TEM) images show a sharp interface between the germanium substrate and the crystalline $Ge_3N_4$ film (Figure 12.15).

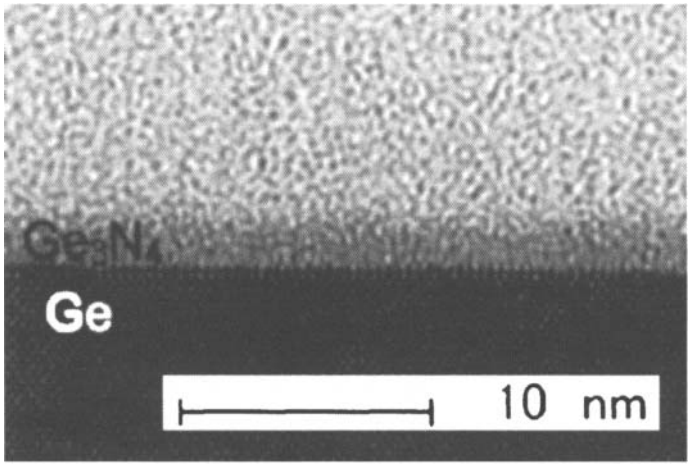


**Figure 12.15.** A cross sectional HR-TEM image of $Ge_3N_4$/Ge substrate [72]. Reprinted with permission from Maeda, T., Yasuda, T., Nishizawa, M., Miyata, N., Morita, Y., Takagi, S., *Appl. Phys. Lett.*, 85(15):3181 (2004). Copyright 2004, American Institute of Physics.

Oxynitridation has been investigated more recently as an alternative to $GeO_2$ to passivate Ge surfaces. Layers consisting of $Ge_2N_2O$ are insoluble in water and their interface with Ge appears to yield good electrical properties [76–78]. Oxynitride layers are obtained following a two-step oxidation/nitridation process after an *ex situ* chemical treatment, the hydrophobic Ge(100) surface is introduced in a furnace at 820K and maintained for 90 min in an atmosphere of $O_2/N_2$ (1:4), followed by $NH_3$ gas flow at 870K for 30–45 min. Transmission electron microscope pictures of such a films (~ 22 nm thick) display a sharp interface between the crystalline germanium and the amorphous oxynitride layer comparable to a $Si/SiO_2$ interface (Figure 12.16) [76]. However, Paine mentions that the electron beam stimulates

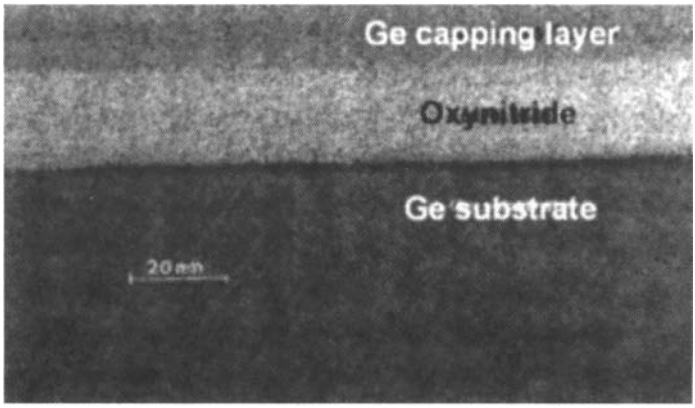


**Figure 12.16.** High resolution TEM image of an oxynitride film grown on a Ge(100) wafer obtained after a two stage-oxidation/nitridation process. The oxynitride layer is capped with amorphous Ge [76]. Reprinted with permission from Paine, D. C., Rosenberg, J. J., Martin, S.C., Luo, D., and Kawasaki, M., *Appl. Phys. Lett.*, 57(14):1443 (1990). Copyright 1990, American Institute of Physics.

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# 13

# Wafer Reclaim

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*Abstract*

Reclamation of wafers results in significant cost savings for integrated circuit manufacturers. To successfully reclaim wafers, particle, metallic, and organic contamination must be removed from the wafer surface after etch-back, grinding, lapping, and polishing. The cleaning and surface conditioning processes used during the reclaim process will be presented in this chapter. Specification for reclaiming wafers, especially removal of copper and other metal contamination and methods to obtain a pristine, particle-free surface are discussed. Comparison of different processes, including standard RCA cleaning compared to simplified cleaning, will be shown and their advantages and disadvantages discussed, and evidence will be provided for how the chemistry and process affects the yield and defect levels of the reclaimed wafers.

*Keywords:* wafer reclaim, wafer recycle, photoresist stripping, silicon life-cycle, metal induced pitting, contamination specifications

## 13.1 Introduction to Wafer Reclaim

Semiconductor manufacturing uses test wafers for particle, film thickness, etching rate, and tool marathon testing monitors, as well as for characterizing new and existing equipment and processes. Depending on the capacity of a fab, test wafer usage can be as high as tens of thousands of wafers per month. As a result of the ever-increasing demand for silicon and the high cost of wafers, integrated circuit (IC) manufacturers are increasing their efforts to reduce overall spending on silicon [1], which is currently the largest non-equipment related expenditure [2]. Current analysis of materials cost as a percent of device revenues indicate that the industry is spending slightly above the historical average of 14%, largely due to high silicon consumption [3]. Therefore, it is not surprising that cost saving due to the use of reclaimed wafers is more important than before the introduction of 300 mm wafers. In addition, the transition to larger wafer diameters such as 300 mm and 450 mm is inevitably accompanied by demanding process technologies resulting in the need for more test wafers during the ramp-up period and also at early stages of process development.

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One approach taken by many IC manufacturers is extending the life of test wafers by using them as many times as possible by processing them through a reclaim process to make them fit for reuse. Typically, the cycle involves sending used wafers to a reclaim vendor, processing them to meet fab specifications, and sending them back to the customer for use as test wafers. A wafer reclamation process involves three main steps:

1. Removing any unwanted materials from the wafer surface (referred to as stripping).
2. Mechanically polishing to remove any surface damage or impurities.
3. Cleaning to ensure that the ultra-low defect requirements of customers can be met.

Currently, the number of times a wafer may be reclaimed is limited as the combination of stripping and polishing steps reduce the thickness of the substrate. Eventually, the test wafers become too thin to be reclaimed and are then scrapped. Therefore, the need for a cost-effective method of efficiently reclaiming test wafers is highly desirable.

In this chapter the lifecycle of silicon in a fab and will be discuss, including the effect on the costs and performance of integrated circuits. A detailed description of the silicon manufacturing process for semiconductor applications, including silicon purification, crystal growth, the wafer slicing process, and energy requirements, will be given in addition to the flow and use of silicon test wafers through a wafer manufacturing fab. Comparison of different reclaim processes will be shown and their advantages and disadvantages discussed, and evidence will be provided for how the chemistry and process affects the yield and defect levels of the reclaimed wafers.

## 13.2 Introduction to Silicon Manufacturing for Semiconductor Applications

Silicon, the seventh most abundant element in the universe and the second most abundant element in the earth's crust, is used to make many electronic devices, such as transistors, integrated circuits, and solar cells because it is a good semiconductor. The process flow for wafer manufacturing is shown in Figure 13.1. Polycrystalline (polySi) and mono-crystalline silicon (mc-Si) wafers are manufactured using high purity, semiconductor-grade silicon as the raw material. They are grown by a technique known as the Czochralski (CZ) method, named after the Polish scientist Jan Czochralski, who discovered the method in 1916 while investigating the crystallization rates of metals [4]. The polySi raw material is first made by the reduction of silica ($SiO_2$), which is mined as quartz sand, with carbon in an electric furnace at temperatures between 1500–2000°C resulting in commercial brown metallurgical-grade silicon (MG-Si) with a purity of 95–98%. This powdered silicon must be further purified to bring impurities below the parts per billion (ppb) level before being used for semiconductor applications. This purification of MG-Si is done by means of a complex reduction and purification process, which starts by reaction of the MG-Si with HCl at 300°C in a fluidized-bed

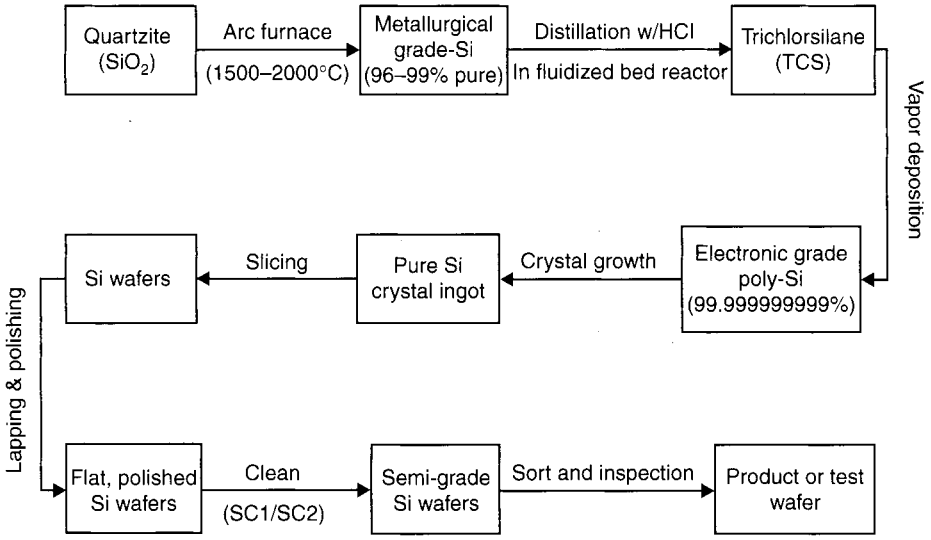


**Figure 13.1.** The process flow for silicon wafer manufacturing for semiconductor applications. Used with permission of the authors.

reactor to form the intermediate compound trichlorosilane (TCS) using the reaction shown in Equation 13.1.

$$Si + 3\,HCl \rightarrow SiHCl_3 + H_2(g) \tag{13.1}$$

In the course of converting MG-Si to TCS, impurities such as iron, aluminum, copper, and boron are removed. Next, the ultra-pure TCS is distilled to achieve a higher level of purity, diluted with hydrogen gas, and the flowed into a deposition reactor where it is retransformed into elemental silicon [5, 6]. The resulting polySi has typical contamination levels of less than 0.001 ppb and purity of 99.999999999%.

Once a high level of purity has been attained, a process known as crystal growing, shown in Figure 13.2, transforms polySi into ingots with a single crystal orientation. The polySi is mechanically broken into chunks, from 2.5–7.5 cm, which are then packed into quartz crucibles for meltdown (at 1410°C) in a CZ furnace in a high-purity argon environment. A monocrystalline silicon seed is placed into a seed shaft in the upper chamber of the furnace. Slowly, the seed is lowered so that it dips approximately 2 mm into the silicon melt. Next, the seed is slowly retracted from the surface allowing the melt to solidify at the boundary. The CZ process starts from a neck process with a reduced growing diameter of a few millimeters to ensure dislocation-free integrity. It is then followed by shoulder, or top, and body growth, and finally by the termination at the ingots tail section (Figure 13.3). As the seed pulls the silicon from the melt, both the crucible and the seed are rotated in opposite directions to allow a round crystal to form. Once the proper crystal diameter is achieved, the seed lift is increased. The silicon crystal ingot is grown with a slightly larger diameter than that of the wafer to account for fluctuations from the slight variation of process conditions during growth.

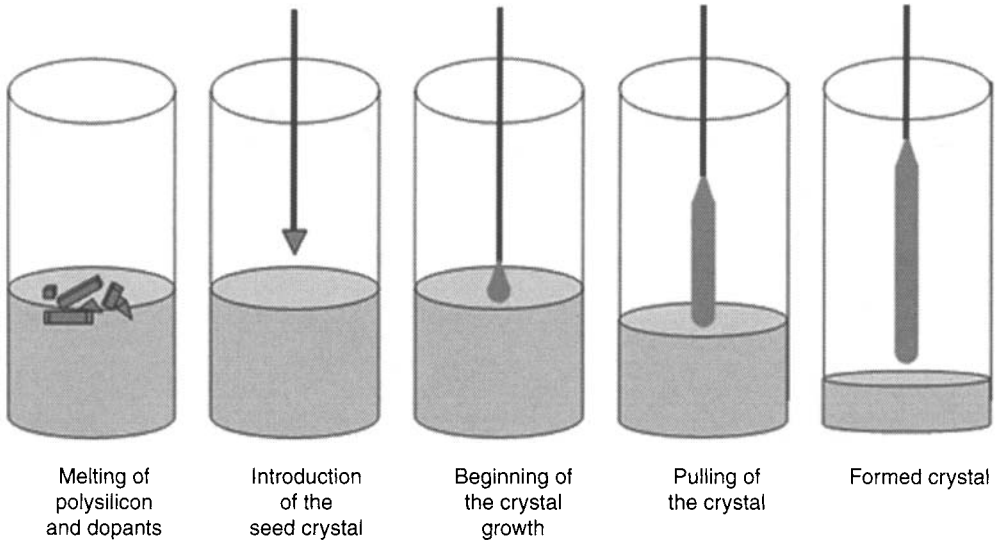
Melting of polysilicon and dopants
Introduction of the seed crystal
Beginning of the crystal growth
Pulling of the crystal
Formed crystal

**Figure 13.2.** A schematic showing the silicon crystal growing process for wafer production. Used with permission of the authors.

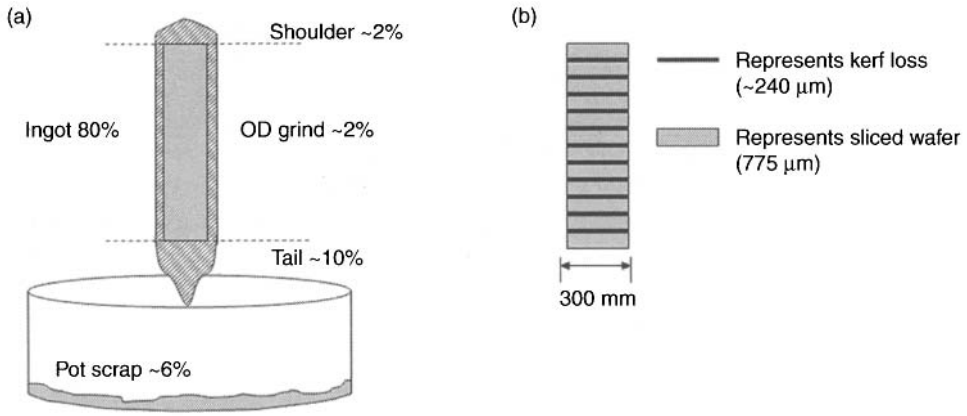


**Figure 13.3.** Graphical representation showing identity and distribution of scrap silicon waste during the wafer manufacturing process [10]. Used with permission of Sage Concepts.

During growth, the walls of the crucible dissolve into the melt; therefore, silicon made *via* the Czochralski method contains oxygen impurities with a typical concentration of 25 parts per million (ppm). The annealing process can be modified to allow the oxygen impurities to form precipitates, which provide the beneficial effects of trapping unwanted transition metal impurities. This is a well-known process called gettering [7, 8]. Additionally, the oxygen impurities can improve the mechanical strength of silicon wafers by immobilizing any dislocation, which may be introduced during device processing. The additions of dopants such as boron, phosphorus, or arsenic are used to modify the electrical characteristics of the silicon and control the resistivity distribution of the final crystal. Once the growth

process is complete, the crystal is cooled inside the furnace for up to 7 hours. This gradual cooling allows the crystal lattice to stabilize and makes handling easier before transport to the next operation. The CZ process typically results in some material loss from four sections, specifically the shoulder, the tail, the overgrowth diameter, and the residual silicon melt remaining in the crucible. This "clean" silicon scrap is cascaded down to the photovoltaic industry as solar cell silicon specifications are slightly less stringent than IC silicon [9].

Once the crystal growth process is complete, the ingot then undergoes a complex slicing and shaping process necessary to turn it into functional wafers. This process includes a series of mechanical and chemical process steps that are designed to bring the wafer into compliance with each customer's specification that will be described in detail in Section 13.5. The first step in transforming the silicon ingot into individual wafers is multi-wiring slicing (MWS) [11, 12]. A thin wire is arranged over cylindrical spools so that hundreds of parallel wire segments simultaneously travel through the ingot. The sawing effect is achieved by using abrasive agents such as silicon carbide particles (~10 μm diameter) carried by a thin iron wire (~140 μm diameter) in the presence of a cutting fluid, typically a glycol solution. This process creates large amounts of micron-size silicon powder called "kerf" which is currently discarded as waste. The amount of silicon waste powder created by sawing a silicon ingot primarily depends on the wire diameter. A reasonable estimate for the average kerf loss produced by wafering silicon ingots in the microelectronics industry currently is ~17%. As a result, many efforts are underway to reduce this material loss in both in the microelectronics and solar industries.

After the MWS process the wafers are cleaned to remove any residual abrasive and debris generated during the process. The rough cut silicon wafers possess saw marks and other defects such as wire-to-wire thickness variations, thus a lapping process is used to remove saw marks and surface defects from the front and backside of the wafers. Lapping is also designed to thin the wafer and relieve stress accumulated in the wafer from the sawing process. After lapping the wafers go through several cleaning and etching steps using sodium hydroxide or a hydrofluoric/nitric/acetic acid mixture ($HF/HNO_3$/Ac-H) to remove microscopic cracks and surface damage caused by the lapping process, followed by a deionized water (DIW) rinse. The edges of the wafer are then rounded *via* a grinding and polishing technique to render the wafers less susceptible to breakage in the remaining steps of the manufacturing process. Edge rounding is an important part of the wafer manufacturing process as it can reduce wafer breakage up to 400% [13, 14].

Polishing is the next step in the wafer manufacturing process. Most prime wafers go through 2–3 polishing steps using progressively finer slurry solutions. The polishing is normally done on the front side of the wafer, but sometimes it is done on both sides, especially for 300 mm wafer processing. After polishing the wafers are rinsed in DIW and scrubbed to remove any residual slurry residues from the wafer. For many applications an additional layer (epitaxial layer) of high purity silicon is deposited on the top of a polished wafer substrate if the quality of a polished wafer is not sufficient. These defects are typically generated during crystal growth. Defects within a few microns of the surface can deteriorate the performance of devices built on top of the silicon.

The final step in the wafer manufacturing process is a rather intense series of cleans and scrubs to remove trace metals, residues, and particles from the surfaces of the finished silicon wafers. Normally most wafer manufacturers use a final cleaning method developed by RCA in the 1970's [15]. A standard RCA clean consists of a combination of two classic chemistries known as standard clean 1 (SC-1) and standard clean 2 (SC-2), also known as RCA-1 and RCA-2. The functions of these chemistries, in the order which they are performed, remove particles and metal contamination and are designed to ensure that all foreign substances are removed from the surface, which enhance the even distribution of the dopant into the silicon lattice.

Standard clean-1 is comprised of ammonium hydroxide, hydrogen peroxide, and DIW. This mixture typically employed in a volume ratio of 5:1:1; respectively, $H_2O$:30 wt% $H_2O_2$:29 wt% as $NH_3$ ($NH_4OH$) and removes any remaining organics by oxidative dissolution. Further, many metal contaminants (Au, Ag, Cu, Ni, Cd, Co, and Cr) are dissolved, complexed, and removed from the surface. The ammonia serves as a mild oxide etchant, the hydrogen peroxide serves as a powerful silicon oxidizer. The peroxide continuously grows oxide on the silicon which results in a continual availability of oxide for the ammonia to remove. Wafers are usually processed for 5–10 min in this solution which is typically at ~70°C, followed by quench and rinse with cold ultra-filtered DIW. Higher temperatures leads to more aggressive particle removal due to higher oxide etch rates.

Standard clean-2 is used to remove any residual metal impurities on the wafer surface left behind from the preceding process step which can severely degrade the quality of the oxide layer. SC-2 is a mixture of $H_2O$:$H_2O_2$:37 wt% HCl, and generally mixed in a 6:1:1 ratio by volume. The wafers are immersed in the solution, which is at 70°C for 5–10 min, followed by quenching and rinsing in cold ultra-filtered DIW. This process removes alkali ions, $NH_4OH$-insoluble hydroxides such as $Al(OH)_3$, $Mg(OH)_3$, and $Zn(OH)_3$, and any residual trace metals such as gold and copper that were not completely desorbed by SC-1 are readily complexed by chlorine to form molecules that do not adhere to the wafer surface.

## 13.3 Energy Requirements for Silicon Wafer Manufacturing

Wafer manufacturing is a long and complex process and requires a substantial amount of energy to produce a single silicon wafer. The melting and purification during the production of the polySi starting material consumes the largest amount of energy (1000 kWh/kg for $1m^2$ of wafer surface) [14]. Production of the single crystal using the Czochralski method requires another 150 kWh/kg for $1m^2$ of wafer surface, thus roughly 1400 kWh/kg are used before the complex steps of device manufacturing is even started. With impurities in the parts per billion, a silicon wafer is the purest product manufactured on a commercial scale. The chain of processes yielding silicon wafers starting from raw quartz is technologically advanced and energy intensive. Table 13.1 displays the results from data search and analysis provided by Williams *et al.* [14] from which it is clear that purification and wafer preparation stages are very energy intensive. Also, significant silicon losses throughout the process chain, largely from the wafer slicing and shaping processes, suggest that 9.4 kg of raw silicon are needed per kg of final wafer [13, 16–19]. The main result

**Table 13.1.** Energy use in stages of production of silicon wafers [14]. Reprinted with permission from *J. Environ. Sci. Technol.*, 36(24):5504 (2002). Copyright 2002, The American Chemical Society.

| Production Stage | Electrical energy input/kg silicon out | Silicon yield (%) |
|---|---|---|
| quartz + carbon → silicon | 13 kWh | 90 |
| silicon → trichlorosilane | 50 kWh | 90 |
| trichlorosilane → polysilicon | 250 kWh | 42 |
| polysilicon → single crystal ingot | 250 kWh | 50 |
| single-crystal ingot → silicon wafer | 240 kWh | 56 |
| process chain to produce wafer | 2130 kWh | 9.5 |

is that 2130 kWh per kilogram is used in the production chain for silicon wafers, about 160 times the amount used to produce "raw" silicon. Energy consumption in purification is thus much more important than the preparation of starting crude material [14]. Electricity consumption to produce one square cm of wafer is nearly one-fourth that needed for device fabrication implying that wafer production is a significant factor in the life cycle assessment of a semiconductor device.

## 13.4 Test Wafer Usage and Wafer Reclaim

### 13.4.1 Silicon Material Flow in a Wafer Fab

In a semiconductor manufacturing facility both product and non-product wafers are consumed. The flow of wafers through a semiconductor fab is illustrated in Figure 13.4 [10]. Product wafers are subjected to hundreds of process steps, typified in the figure as steps ($N$–1), $N$, and ($N$+1), that include the formation of transistors, other basic circuit elements, and metal deposition onto the wafer, which are used to interconnect the basic circuit elements to produce hundreds of integrated circuit devices per product wafer. The yield of each step must be very high in order that the overall yield of the wafer is acceptable. Since the overall yield of a device is the product of all of the individual step yields multiplied together, then Y (overall) = Y (individual) × n, where n is the total number of steps. Thus if there are 100 steps in the process and the yield of each step is only 95%, the resultant overall yield is less than 1%; if the step yield is 99%, then the overall yield would be 36.6%; and if the individual step yield is 99.9%, then the overall yield would be 90%.

Since the individual step yields are important determinants of the overall device yield, it is necessary to assure the yield of each individual step is as high as possible. Therefore, non-product wafers are used to verify the individual step processes before the product wafers are processed. These non-product wafers are known as test and monitor wafers. They are used to assess the individual performance

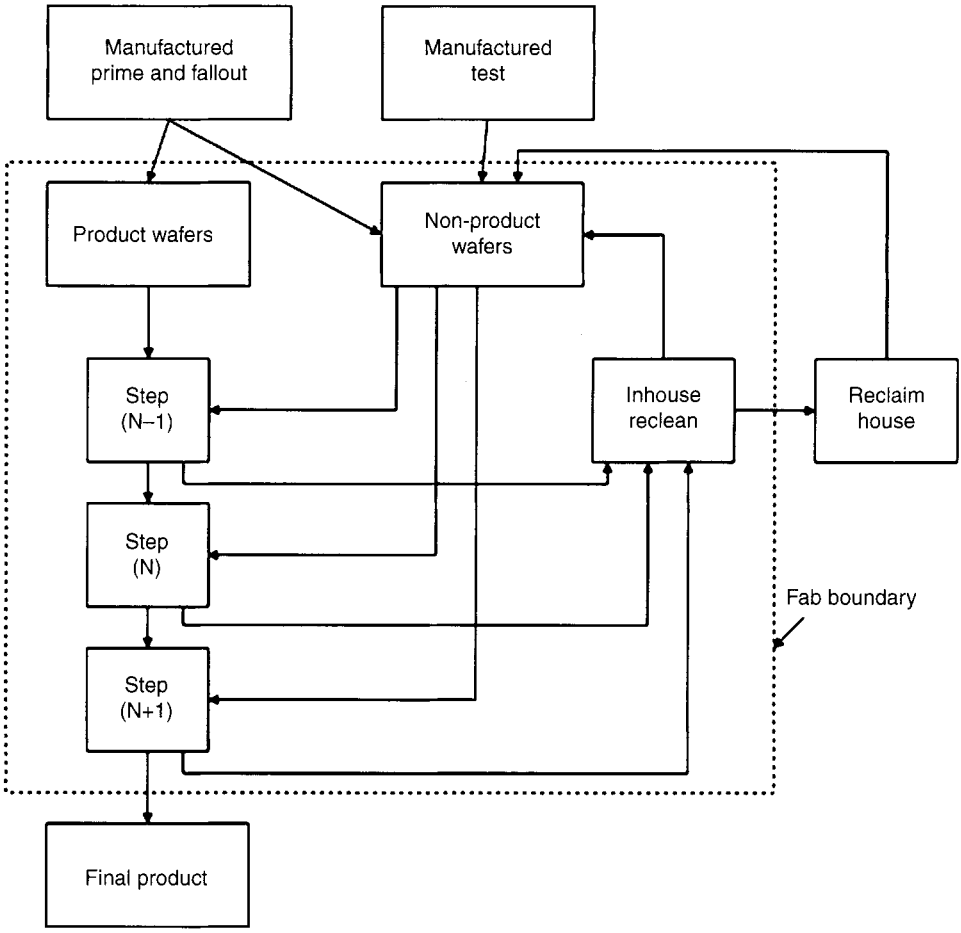


**Figure 13.4.** Schematic flow of wafers through a typical semiconductor fab. Adapted from [10]. Used with permission of Sage Concepts.

of each production tool and to monitor the repeatability of processing steps. The primary source of test and monitor wafers are virgin test wafers. The wafers are obtained from fallout of the manufacture of product wafers or they are manufactured specifically as test wafers.

## 13.4.2 Economics of Reclaiming Wafers

Cost is an important metric in semiconductor fabrication and this is particularly true for device manufacturing. As a result, cost control and cost reduction programs have become extremely critical at semiconductor foundries. Effective use of resources and stable processes are part of the key to enabling cost control and reduction. Fab materials currently make up about 50% of the value of the total worldwide semiconductor materials market, with the majority of revenues coming from silicon sales, shown in Figure 13.5 [3]. The fact that silicon is the

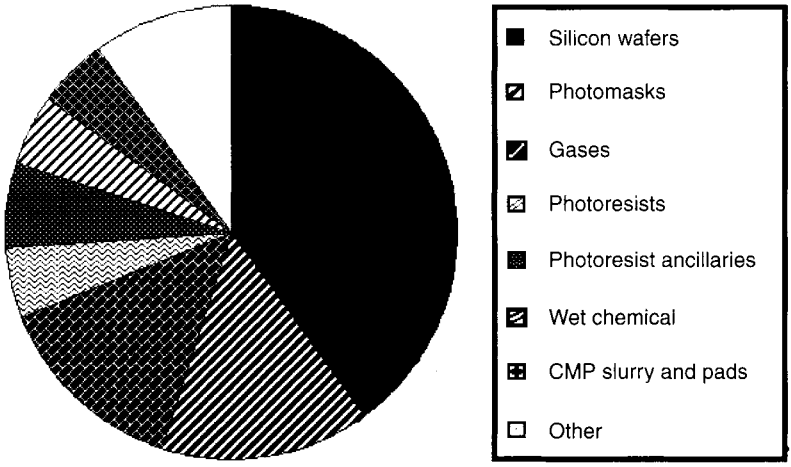


**Figure 13.5.** Graph showing the fabrication materials market by segment. Adapted from [3]. Used with permission of SEMI.

fundamental backbone of semiconductor processing is evident and accounts for 43% of the wafer fabrication materials market.

In the start-up phase of a new fab, product wafers may represent less than half of the wafers while the remainder are test and monitor wafers, which are less expensive for non-critical tests. For 200 mm fabs, the test wafer cost is about half the overall materials cost while for a manufacturer using 300 mm substrates test wafers account for about 64% of the total materials cost. This percentage will increase once the transition to 450 mm wafer begins since the early wafers will be approximately $15,000 to $20,000 when pilot production is underway [20].

Test and monitor wafers are wafers that are processed along with product wafers. Although they are substantially the same as prime polished wafers with respect to cleanliness and flatness, other specifications are generally less rigorous allowing for a more cost-effective solution for non-critical wafer applications. Test wafers are used for equipment qualification, regular monitoring for particles tests, and film thickness/uniformity, process development such as modifying an existing process step, as well as for short loop test wafers, such as to verify *via* chain resistance. In a sense, they represent a snapshot of process reliability for particular parts of the overall flow.

More than 22 million test wafers are used annually across the semiconductor industry [21], and as a result, a number of major semiconductor manufacturers have built in-house recycling programs or used third-party reclaim services, focused on extending the usable life of test wafers by attempting to reuse them as many times as possible. Internally recycling of test wafers can save companies millions of dollars (the calculation is shown in the next paragraph) compared to the cost of new or externally reclaimed wafers since reclaimed wafers are usually about half the cost of new wafers. In addition, reclaim wafers can typically be recycled an average of three times before they become too brittle and thin due to silicon loss during the reclaim process.

A high volume production fab may consume up to 1000 test wafers each day depending on their usage efficiency, and considering the cost of a new 300 mm test wafer, which is roughly $200 each, this can lead to a monthly test wafer spending of $4 million for 20,000 test wafers per month. This is a significant cost to the fab for a non-product related material; therefore, manufacturers try to reduce this cost by recycling wafers through external reclaim services since reclaimed wafers from these services are usually about half the cost of new wafers. Assuming a recycle rate of three, as stated above, the average cost per wafer use over the wafer lifetime still drops to $125 (=[$200 + $100 + $100 + $100]/4) which can create a positive impact on overall test wafer spending.

## 13.5 Requirements for Wafer Reclaim and Recycle

In order to maximize the lifetime of reclaimed wafers, it is essential to maintain wafer surface quality, both physical and chemical, throughout the reclaim process. Besides reducing silicon loss during mechanical polishing steps, trace metal contamination must be monitored and controlled and are subjected to the same specifications as new wafers. There are several important performance specifications that reclaimed wafers must meet before being inserted back into process lines and used as test wafers. The key metrics are:

1. Particle concentrations.
2. Minimal surface defects such as pits and scratches.
3. Trace metal contamination.
4. Surface roughness.
5. Flatness, or total thickness variations (TTV).
6. Final thickness.

Total thickness variation represents the difference between the minimum and maximum thickness measured on the wafer. Another requirement is overall wafer thickness. Many reclaim process use mechanical polishing to remove films and surface defects, thus, reducing surface silicon thickness by 10–20 μm per reclaim cycle. A typical prime 300 mm wafer with an initial thickness of approximately 775 μm becomes too brittle and prone to cracking once its thickness is reduced below 680 μm. Other important metrics are yield, cycle time, and wafer usable life.

### 13.5.1 Reclaim Wafer Metrics

The surface quality of reclaimed wafers is very important. This is used to assess the successfulness of the reclaim process. Table 13.2 shows the comparison of existing wafer reclaim specifications with the equivalent spec on a 300 mm wafer. For a 300 mm wafer, the metal, flatness, and particle specification is the same as for 200 mm, even though the area is more than twice the size of a 200 mm wafer. As the industry moves to each successful technology generation, new specifications will continue to be needed [21–23]. Therefore, effective analytical methods are critical to characterize and monitor the blanket Si surface. These methods will be briefly discussed.

**Table 13.2.** Comparison of existing wafer reclaim specifications. Compiled from data found in [22, 23].

| Specification | Existing high quality 200 mm wafer | Required 300 mm specification | 300 mm specification for sub-0.18 μm |
|---|---|---|---|
| Defect density | <0.16 def. $cm^{-2}$ | <0.07 def. $cm^{-2}$ | <0.028 def. $cm^{-2}$ |
| Light point defects (LPD) | <50 @ 0.16 μm | <50 @ 0.16 μm | <50 @ 0.12 μm |
| TTV | <15 μm | <15 μm | <5 μm |
| Surface roughness (RMS, Å) | 4 | 4 | 4 |
| Metals | $<5 \times 10^{10}$ $cm^{-2}$ | $<5 \times 10^{10}$ $cm^{-2}$ | $<1 \times 10^{10}$ $cm^{-2}$ |

### 13.5.2 Techniques for Measuring Wafer Reclaim Specs

Wafer defect and particle measurements use a light scattering system to detect the light point defects (LPD) on the surface [24]. Particles or defects on the wafer surface will have a stronger scattering signal than the wafer surface. The scattering signals with intensities higher than the threshold are reported as defects, and the signal below the threshold is recorded as haze. Surface roughness, damage, and organic film residues from unwanted contaminants will result in haze scattering, which must be distinguished from defects. When particle size becomes smaller (*i.e.* nanometers) and the scattering intensity for the small particles approach the level of stray light in the system, the detection will reach a limit which translates into the haze sensitivity. Current state-of-the-art commercially available technology has limitations for detecting particles at 30 nm.

Atomic force microscopy (AFM) is a technique that is capable of measuring three-dimensional surface roughness at a nanometer scale level [25]. These measurements are obtained by mechanically scanning a cantilever tip over the wafer surface. When the tip scans, it interacts with the attractive (non-contact mode) and repulsive (contact mode) forces between the tip and surface and moves up and down following the contours of the surface roughness. The size of the AFM tip has a significant impact on the measured roughness. Roughness is typically presented by a mathematical relationship known as root-mean-square (RMS), which describes the variation of the surface height about an average surface height. A limitation of AFM is that the analyzed area is quite small, which may not be representative of the entire wafer surface. For entire wafer surface roughness, light scattering measurements should be utilized.

Total thickness variation is the difference between the maximum and minimum values of the thickness of the wafer. The thickness variation of silicon wafers can significantly affect yield of semiconductor devices and is an important specification for reclaim wafers. The measurement of TTV uses capacitance gage technology. The thickness variation is recorded by serially scanning a pair of probes located on each side of the wafer over the spinning wafer surface [26]. Interferometry is

another approach to determine the wafer thickness variation and surface profile by using a laser beam and measuring the position of the beam reflected from the wafer surface [26].

Trace metal concentrations are a critical specification of reclaim wafer surfaces. An appropriate metrology method is vapor phase decomposition/inductively coupled plasma-mass spectroscopy (VPD/ICP-MS), which can quickly analyze the whole wafer surface with extremely low detection limits ($10^8$ atom/cm$^2$) for a wide range of elements. The limitation of this method is that it is destructive [25]. Another trace metal measurement metrology is total reflection x-ray fluorescence (TXRF) spectrometry, which is non-destructive, and possesses a detection limit of $10^8$ atom/cm$^2$. The limitation of this method is that it cannot analyze Na and Al and has a limited sample analysis area (10 mm resolution) [25].

Organics analysis is also an important metric for monitoring the surface contamination and cleanliness of a reclaimed wafer. Some of the common techniques used for organics analysis are time-of-flight secondary ion mass spectrometry (TOF-SIMS) , Fourier transform infrared spectrometry (FTIR), and thermal desorption gas chromatography mass spectrometry (TDMS) [25]. Time-of-flight secondary ion mass spectrometry provides a high lateral (1000 Å) and depth resolution (<10 Å) and can analyze low-level organic contamination deposited on a wafer's surface. Fourier transform infrared spectrometry can provide useful information on chemical bonding, but has relatively high detection limits compared to TOF-SIMS and TDMS. The method of TDMS involves heating the wafer in a sealed chamber collecting the resulting gas-phase organics desorbed from wafer surface, and then analyzing them. The detection limit is on the order of $5 \times 10^{11}$ C atom/cm$^2$. The advantage of TDMS over TOF-SIMS is that it can analyze an entire wafer surface and eliminate the potential loss of contaminants in the sample preparation. The disadvantage of this method is that it cannot provide information on the lateral distribution of the contaminants.

## 13.6 Wafer Reclaim Options

When considering reusing test wafers, a distinction should be made between the definitions of "reclaiming" versus "recycling" wafers. Recycling is the reuse of wafers with low particle defectivity and good surface characteristics. Once the wafers have deteriorated beyond the point that they can be successfully recycled, *i.e.* failure to meet the defectivity specification, they can be reclaimed. Since wafer recycling does not involve any removal of silicon, it is thus generally viewed as yielding higher value wafers since the lifetime of the wafer is significantly increased, which results in a reduced cost of the wafer throughout its lifecycle. In order to be recycled, the bulk silicon prior to film removal must be in near pristine condition, and the wet chemical process to remove the film must not damage the silicon surface.

In either case, there are two options when considering reclaiming or recycling of wafers: the wafer user can process the test wafers using their own internal process procedure or ship them out to manufacturers that specialized in reclaiming wafers. Although internal test wafer recycling programs are attractive due to

reduced cost and cycle time plus a low risk of contamination, the ability of fabs to implement reclamation is quite limited since most have limited real-estate and capital equipment to be dedicated to recycling. This has led to the establishment of the wafer reclamation industry by where the reclamation cycle forms a loop in which used wafers are sent to a reclaim vendor, processed to meet fab specifications, and sent back to the customer for use as test wafers. The advantages and disadvantages of both internal and external wafer reclaim will be discussed in detail in the following sections.

### 13.6.1 External Reclaim

Since the number of processes that require the use of test wafers is vast, many different types of wafers including: bare, patterned, metal, non-metal, and combinations thereof are produced, making it difficult for device manufacturers to handle all of them with an internal reclaim loop. As a result, many fabs send their wafers to an external reclaim house to be processed. Some of the reclaim industry leaders are Rasa, Kobe Precison, Mimasu, and Hamada (Japan), Rockwood (United Kingdom), Nestec (North America) and Kinik (Taiwan), and there exists approximately 26 more reclaim companies world-wide. Reclaim processes employed by these companies typically are extremely complex and include many cleaning steps followed by intense inspection steps that yield wafers of different grades that can be used for different applications.

The quality of the incoming wafers has significant influence on the yield and future application of the reclaimed wafers. The yield of wafers used for different applications by the IC manufacturer may vary between 0% and 100%. Typical reasons for a wafer reclaim provider to reject wafers at incoming inspection are wafer thickness, deep stress lines, edge chips, or extremely high warp [27]. Knowing a wafer's history allows choosing an optimized reclaim process and future application for the wafer or immediately to reject the wafer. Different quality levels are defined for the different applications in a wafer fab. For example, for some applications the number of particles on the wafer surface is of critical importance, whereas the wafer geometry, thickness, bow and warp are of minor importance.

The first step of the reclaim process, as shown in Figure 13.6, is inspection and sorting of the wafers. This is followed by film layer removal by means of chemical etching. The wafers are then presorted and subjected to visual inspection to determine the surface quality of the wafers. The next step is a strict regimen of polishing and lapping; consisting of both coarse and fine surface polishing to remove deep scratches and surface defects, followed by a final cleaning. The last step is final inspection where the particle level of the wafers is determined.

Although reclaim processes are similar to the manufacturing processes of virgin silicon wafers, there are additional challenges due to the wide range of conditions of the incoming wafers. The main objective of the reclaim process is to minimize the removal of silicon wafer by the etching and polishing processes. The number of reclaim cycles, which a wafer could possibly undergo before being too thin, has a significant impact on the cost savings of the IC manufacturer. The conventional approach, which treats every wafer in the same way, is to remove the films and silicon from the front and back surface of the wafer by mechanical grinding

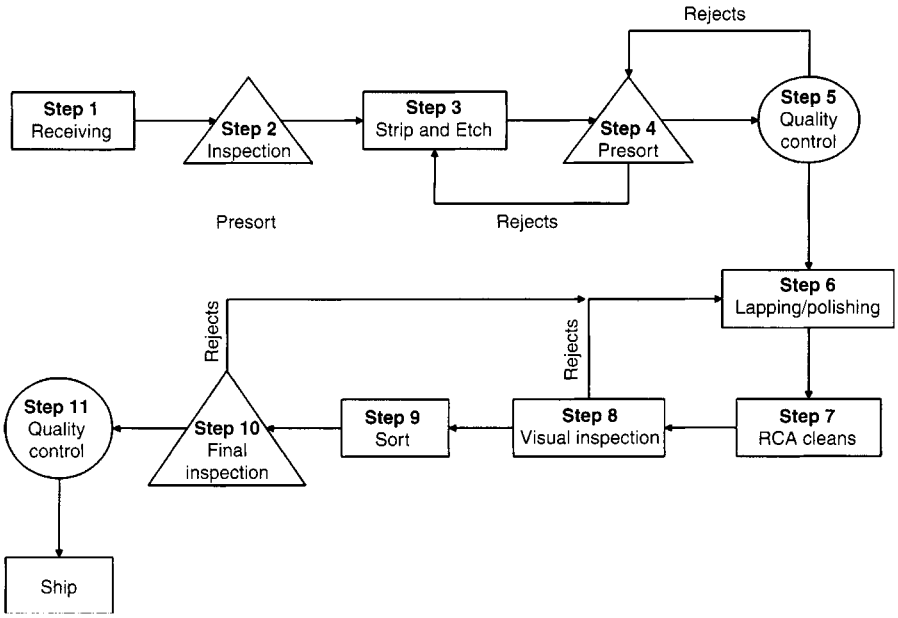


**Figure 13.6.** Schematic of the wafer process flow for wafer reclaim suppliers. Used with permission of the authors.

or lapping processes. Depending on the condition of the used wafer, 2–40 μm can be removed from the surface. For example, a wafer without any scratches and chuck marks will only lose a few microns, whereas a wafer with deep trenches requires more silicon removal, in some cases, up to 40 μm. In the latter case, it is only possible to reclaim each wafer 1 to 2 times before the minimal critical thickness of 680 μm is reached.

Semiconductor manufacturers who send wafers outside of their fab are taking a risk that the returned wafers will not contaminate their production line. For instance, in IC fabrication processes, copper will effect minority carrier lifetime [28], and thus presents a formidable challenge during reclaiming copper-containing wafers. Copper can diffuse into silicon at relatively low temperatures, thus posing the danger of device failures (discussed in detail in Section 13.7.3). As a result, many reclaim houses have been forced to develop stringent copper-specific protocols such as process line segregation to avoid cross-contamination during the reclamation process. Incoming copper wafers are physically segregated from non-copper wafers according to visual inspection. However, such segregation methods are prone to risk as a small number of copper wafers are misplaced into non-copper process baths and cause problems, thus reclamation processes are required that are robust enough to deal with copper wafers in non-copper chemical stripping baths and processes.

Overall, the downsides of external reclaim are longer cycle time as compared to internal reclaim loops, risk of contamination, and yield reduction due to loss of wafers from shipping, handling, processing, *etc.* These concerns must be weighed with respect to a customers' needs and grade of wafer desired for further reuse as a monitor or test wafers in the wafer manufacturing processes.

### 13.6.2 Internal Wafer Reclaim Programs

The driver for a fab to use wafer reclaim is the cost saving benefits. As a result of these benefits, many semiconductor manufacturers have implemented internal test wafer recycling programs which consist of process loops that range from simple cleaning and reuse steps to extremely complex strategies, with the former being more common. A simple process flow may be developed to recover wafers that are used for only one purpose. Complex process flows may involve the categorization of all wafers and their upgrading or downgrading according to test wafer specifications and then specialized processing. The level of complexity is highly dependent on resources such as equipment availability and fab space, the volume and types of wafers needed to be reclaimed or recycled, and thus is highly customized from fab to fab. An example reclaim process is depicted by the schematic shown in Figure 13.7. In the case of carbon-doped silicon oxide ULK films, the films are oxidized in a plasma process to collapse pores and deplete the carbon of organic groups such as methyl ligands [29, 30]. The oxidation also renders the film surface hydrophilic increasing its wettability in the second step; wet etching is performed in dilute HF (DHF) for removal of the Si-O network. Following the wet stripping step, the wafers undergo a series of ultra-pure cleaning steps such as SC-1 and SC-2 to ensure surface metal levels of less than $1 \times 10^{10}$ atoms/cm$^2$ and to meet defect specs which are $\leq 50$ LPD at $\geq 0.12$ μm for a reclaimed wafer. Once completed, the wafers are downgraded to monitor wafers.

In addition to cost savings, cycle time can be significantly reduced when the reclaim process is performed in the fab thus enabling the test wafers to be back in the production line quickly. When the test wafer supply is small, a short reclaim cycle can translate to higher throughput of production wafers. However,

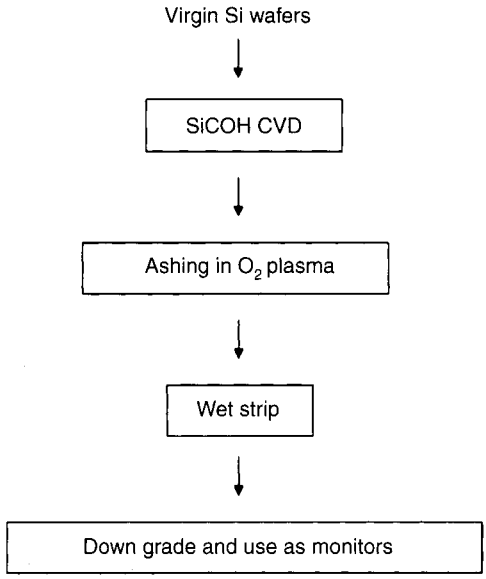


**Figure 13.7.** Example reclaim process flow for carbon-doped chemical vapor deposited (CVD) low-κ films [30]. Used with permission of the authors.

the benefits gained through cost and cycle time can sometimes be erased when problems such as cross-contamination with copper occur. Because of copper cross-contamination issues, many device manufacturers avoid processing copper wafers internally. However, those who do process such wafers rely on segregating them and by performing stringent incoming inspections.

## 13.7 Types of Wafer Reclaim Processes

### 13.7.1 Conventional Reclaim Processes

Until recently, most wafer reclaim techniques involved the immersion of wafers in a series of chemical baths using commodity chemicals such as sulfuric acid, nitric acid, hydrogen fluoride, hydrogen peroxide, and combinations thereof. Although these solutions are capable of stripping a variety of films, they are also very corrosive and cause damage to the underlying substrate, such as roughening, pitting, and thinning. As a result, a post-strip chemical mechanical polishing (CMP) step typically is needed during the reclaim process; however, polishing possesses a major disadvantage – it can remove up to 20 μm of silicon depending on the severity of surface damage such as scratches and pits. In many cases, the back surface of the wafer is also polished to remove potential metal contamination. Polishing is an expensive process and results in considerable silicon loss, which can result in a brittle wafer and as a result decreases the overall lifetime of that wafer. The post-strip polishing step is a key factor that distinguishes recycled from reclaimed wafers. Moreover, it is risky to employ traditional film-removal methods involving CMP when processing copper wafers as this technique does not remove contamination on the wafer edge, as depicted in Figure 13.8. Chemical mechanical polishing cannot round the edge of the wafer, thus if residual copper film is deposited on the edge or the edge is contaminated, copper may remain and endanger downstream processes. Furthermore, because of the mechanism of conventional lapping, a deeply damaged layer is created on the wafer requiring significant silicon removal in subsequent processing steps to recover the original wafer finish.

### 13.7.2 Non-metal Reclaim Processes

The increasing demand for smaller, faster, and more powerful integrated devices has led to many new materials being introduced to achieve these goals [31], which has resulted in a wide variety of materials being deposited on test wafers that must be removed during the reclaim process. These materials include:

1. Dielectric materials consisting of organosilicate glass (OSG), carbon-doped oxide (CDO) glass, fluorinated silicate glass (FSG), tetraethylorthosilicate (TEOS), and silicon nitride.
2. High-κ dielectric materials such as the oxides of hafnium ($HfO_2$), zirconium ($ZrO_2$) tantalum ($Ta_2O_5$) and aluminum ($Al_2O_3$), and silicates ($HfSiO_x$) and nitrides ($SiN_x$).

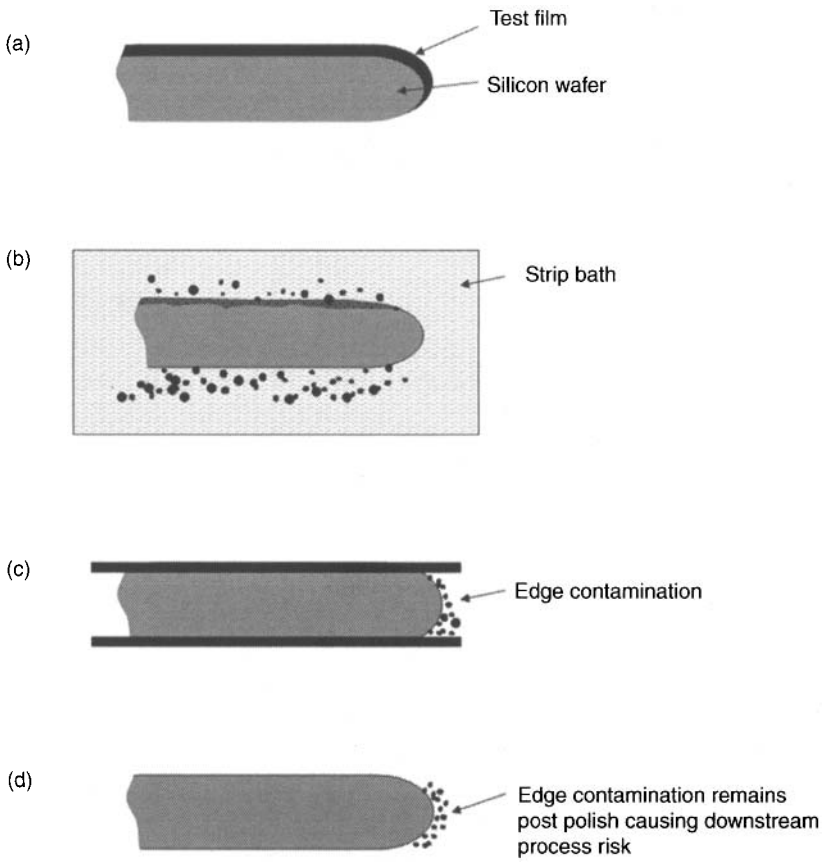


**Figure 13.8.** Depiction of edge contamination: (a) test wafer prior to the reclaim process, (b) the immersion in a chemical stripping bath to remove the material on the wafer surface, (c) double-side polishing of the wafer to remove surface damage, and (d) the wafer post-reclaim with edge contamination. Used with permission of the authors.

3. Etch stop materials such as silicon carbide (SiC), silicon carbon nitride (SiCN), silicon carbon oxide (SiCO), silicon oxynitride (SiON).
4. Barrier layer materials including silicon-rich nitrides, silicon-rich oxynitrides, tantalum, titanium, ruthenium, hafnium, tungsten, and other refractory metals and their nitrides and silicides.
5. Organic polymer films such as photoresist and bottom anti-reflective coatings.

Test wafers containing inorganic dielectric films such as barrier, etch stop and CDO films mentioned typically are stripped using dilute DHF solutions. It is well known that $HF_2^-$ is the active agent for etching silicon nitride and oxide-based films according to the following equation, discussed in Chapter 3:

$$SiO_2(s) + 6\,HF(aq) \rightarrow H_2SiF_6(aq) + 2\,H_2O \qquad (13.2)$$

An effective reclaim process should be able to strip films *via* a dissolution mechanism versus a delamination mechanism. In general, delamination and/or

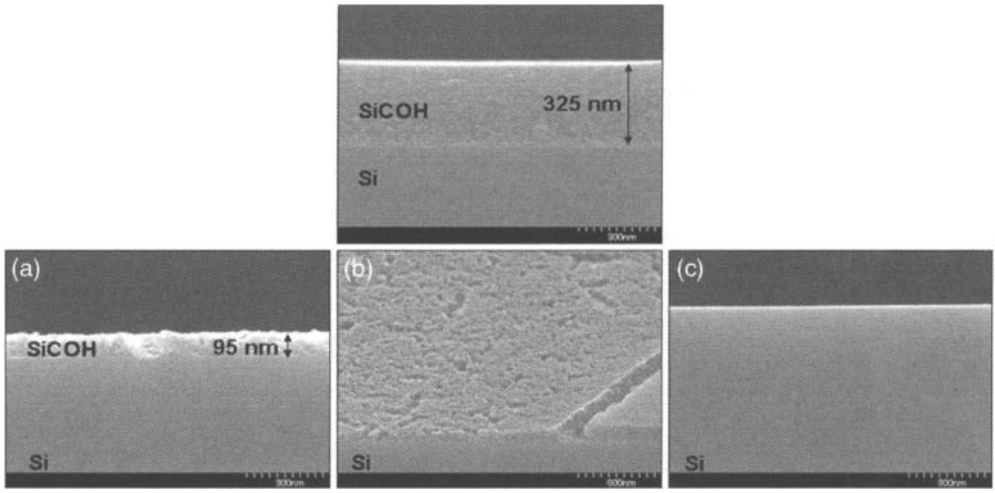


**Figure 13.9.** Cross section (90°) scanning electron micrograph image of CDO film $\kappa = 2.2$ (top view); (a) 90° view of film processed in HF, (b) 60° view of same film processed in HF, (c) 90° view of wafer processed using a dry and wet reclaim process [30]. Used with permission of the authors.

cracking of films results in the generation of particles that can lead to high defect counts, which requires the wafer be subjected to a polish step to lower defects to within customer specifications (*i.e.* <50 at 0.12 μm). Delamination and partial etching becomes more of an issue when the Si-based films contain high levels of carbon as in the case of CDO and SiC. To avoid the defect issue related to delamination of films and to remove films that are difficult or impossible to remove *via* chemical dissolution, some fabs use a combination of dry and wet processing [30]. Due to the inability of HF to remove CDO films (Figure 13.9a and 9b); they are oxidized in a plasma process to collapse the pores and deplete the carbon. The oxidation also renders the film surface hydrophilic. The clean-up steps are similar to those discussed in Section 13.6.2.

Low-κ film surfaces are known to have low surface energies [32] and are therefore difficult to wet, especially using water-based cleaning solutions with high surface tension. Thus, to achieve efficient etching or dissolution of a non-polar low-κ film in an aqueous HF-based solution, good wetting behaviour of the liquid is essential. To lower the surface tension of water-based etching solutions, the addition of surfactants [33, 34] and/or solvents [35] are some approaches. Commercially available formulations incorporate the use of biodegradable surfactants in very low concentrations to achieve effective wetting of ultra low-κ dielectrics. Low-κ materials with dielectric constant values below 2.2, which are poorly wetted, can make use of the hydrophobicity of the surfactant tails and ionicity of the surfactant heads, as depicted in Figure 13.10. The low-κ films are wetted and subsequently dissolved in the solution, while simultaneously passivating the underlying silicon surface from damage during the process.

Using surfactant addition in a formulated CDO stripping composition ATMI's RegenSi®, a comparison of surface contamination levels between it and an HF solution using x-ray photoelectron spectroscopy (XPS) is shown in Figure 13.11.

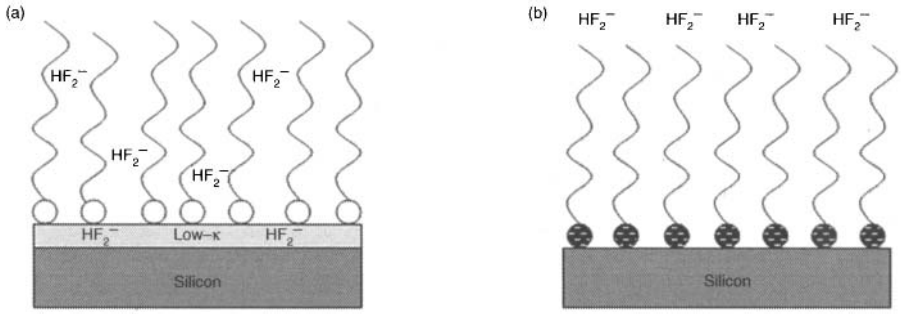


**Figure 13.10.** The wetting behaviour of the (a) surfactant A allowing the penetration of the active low-κ etching species, $HF_2^-$, to the film surface to perform dissolution and the passivating behavior of (b) surfactant B on the silicon surface blocking the active etching species from damaging the underlying substrate surface. Used with permission of the authors.

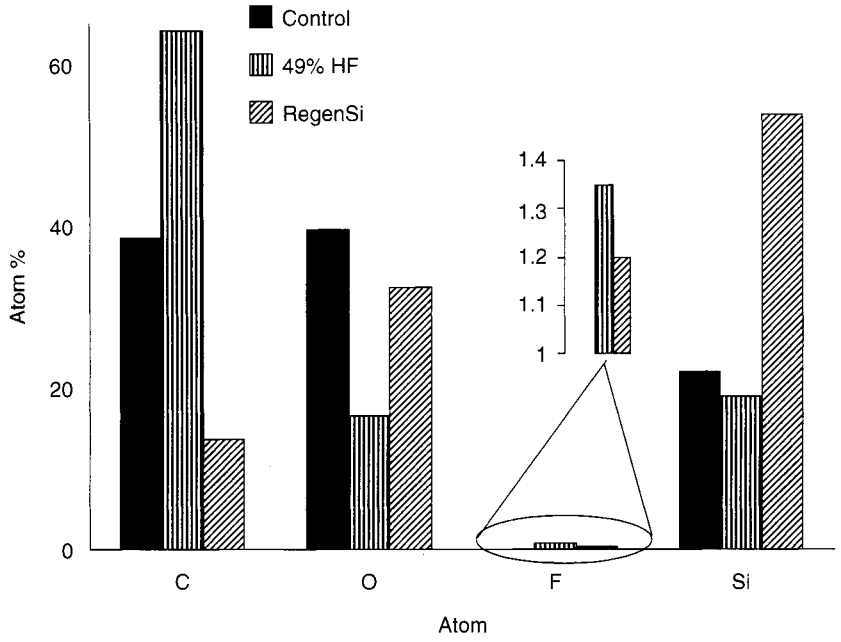


**Figure 13.11.** X-ray photoelectron spectroscopy analysis of κ = 2.2 CDO film processed using HF and RegenSi® which is a HF-based solution with surfactant as an additive, compared to unprocessed film [30]. Used with permission of the authors.

The XPS analysis indicates the carbon content of the wafer processed in 49 wt% HF is higher than the control, perhaps due to a densification of the low-κ material during the plasma processing. Conversely, the low-κ film stripped using the addition of surfactant into the HF shows a reduction in carbon and a concomitant increase in silicon and oxygen indicating the removal of the low-κ film. The slight carbon detected on the surfactant/HF processed sample is likely due to ubiquitous atmospheric contamination.

### 13.7.3 Metal Reclaim Processes

Normally metal wafers are received with a variety of films, including wafers with combination films, such as Al, W, Ti, and Ta, barrier layers such as SiN, TiN, TaN, and non-metallic layers, such as plasma enhanced chemical vapor deposition (PECVD) tetraethyl orthosiloxane (TEOS). A common back end of line (BEOL) metal film stack is listed in Table 13.3. Figure 13.12 shows a typical stack layer of films that must be chemically removed from a silicon wafer surface in order to reclaim it.

A metal wafer reclamation process involves three main steps: removing films on the surface, polishing to give a mirror finish to the wafer, and cleaning the polished wafer [36–38]. The process flow is shown in Figure 13.13. Reclaimed silicon wafers have a unique film removal process that is needed to reduce the concentration of metals on the silicon surface, such as Al, Ti, and W. After this film removal process, the silicon wafers are subjected to a process similar to that used for the manufacturing of virgin wafers.

The traditional film removal methods include chemical and mechanical techniques. Chemical techniques involved the immersion of wafers in a series of chemical baths, such as SPM (sulfuric acid hydrogen peroxide mixture), SC-2, DHF and/or a mixture of nitric and HF, to strip the film materials and etch the silicon. Mechanical techniques, also called lapping process, physically remove films and silicon by placing the wafer between two counter rotating metal plates and grinding away material with the assistance of slurries. Although this technique effectively removes films from the front and back surfaces of wafers, it does not remove

**Table 13.3.** Typical BEOL copper stack for recycling or reclaiming.

| Film Material | Thickness (Å) |
|---|---|
| Electroplated Copper | 10,000–15,000 |
| Copper seed | 1,000 |
| Barrier (Ta TaN) | 100–250 |
| PECVD-TEOS | 4,000–5,000 |

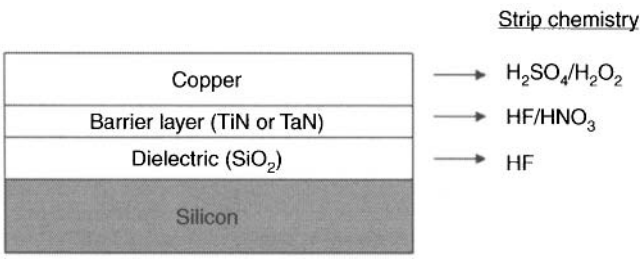


**Figure 13.12.** Typical stack of films to be removed from silicon wafer surface. Used with permission of the authors.

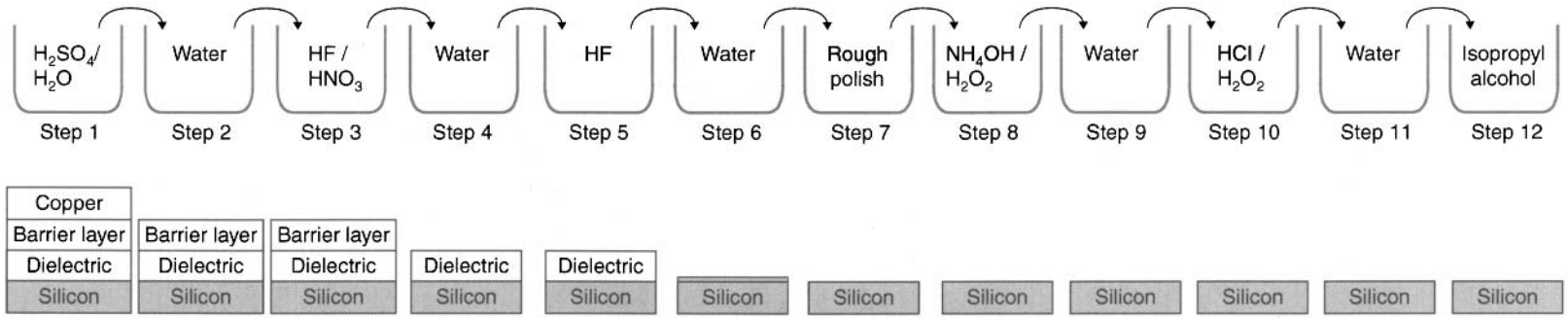


**Figure 13.13.** A typical reclaim process flow for copper and barrier film-containing wafers. Used with permission of the authors.

contamination on the wafer edge. Furthermore, because of the mechanical nature of conventional lapping, a deeply damaged layer is created on the wafer requiring significant silicon removal in subsequent processing steps.

### 13.7.4 Metal Contamination

As device feature sizes shrink, aluminum wiring which had been used for decades is being replaced by copper wiring which has significantly better electrical conductivity and higher electromigration resistance. However, the presence of copper films in BEOL processes poses new problems to the wafer reclaim industry. Copper has a larger diffusion factor in silicon compared with other transition metals, which induces not only deposition of copper on the silicon wafer surface, but penetration within the silicon lattice during traditional reclamation processes [39–42]. Moreover, contamination spreads during the reclamation processes; copper can penetrate deep inside the silicon lattice which is difficult to remove by traditional methods. To date, there is industry-wide reluctance to reclaim copper wafers for fear of cross-contamination. Reclaim vendors typically separate wafers with copper-containing films during the initial visual inspection. However, these segregation methods are inadequate when weighing the risks of contamination since "stealth" copper wafers may slip into non-copper process baths and cause problems. On the other hand, residual copper containing wafers are inevitably mixed with non-copper containing wafers due to human error associated with the subjectivity of a visual inspection. The integrity of an entire reclaim wafer lot can be compromised by one misidentified copper-containing wafer. Therefore, it is very important to prevent this from occurring during the reclamation process.

In the wafer reclamation loop, the process step most prone to the copper contamination is chemical etching. In this step, the chemical solutions used to remove films from a wafer are typically hydrofluoric acid-based. While HF-based solutions effectively remove most types of materials from the wafer surface, they tend to promote surface pitting on bare silicon when copper is present in the solution. Moreover, it was reported that the slurries used during the polishing step containing copper impurities on the order of only ppm can cause copper penetration into the wafers [40].

The deposition of copper on a silicon surface in HF-containing solutions has been extensively studied [43–47]. Although the exact mechanism in which this deposition occurs is still under investigation, it is generally agreed that an electrochemical reaction occurs where the copper ions are reduced at the cathodic side of the silicon surface following electron transfer, as shown in Eq. 13.3 while the silicon atoms are oxidized and release electrons at the anodic side and are simultaneously dissolved in the HF solution, Equations 13.4 and 13.5.

$$2\,Cu_{(aq)}^{2+} + 4e^-_{(Si)} \rightarrow 2\,Cu_{(s)} \tag{13.3}$$

$$Si + HF \rightarrow SiF_6^{2-} + 6\,H^+ + 4e^-_{(Si)} \tag{13.4}$$

$$Si + 2\,Cu^{2+} + 6\,HF \rightarrow H_2SiF_6 + 2\,Cu + 4\,H^+ \tag{13.5}$$

Because a copper stripping bath contains a significant amount of copper, redeposition will occur even if the copper is initially removed. Furthermore, hydrofluoric acid solutions etch the oxidized silicon resulting in surface roughening and pitting, as depicted in Figure 13.14. Figure 13.15 shows typical SEM images of Si surface (p-doped Si and undoped Si) after copper contamination in a 0.5 wt% HF solution spiked with 1 ppm of copper ions [48]. The SEM images reveal that the samples of undoped silicon show severe corrosion, otherwise known as metal induced pitting (MIP), while the p-doped silicon surface shows a surface roughness and redeposition of copper particles.

One method to prevent Cu contamination in the chemical etching step is to develop a more effective cleaning solution having the capability to prevent copper reduction by separating contaminants from the wafer surface and to preventing adhesion of contaminants. One approach is to use a chemical etching solution with a high oxidation-reduction potential (ORP) value. Figure 13.16 shows

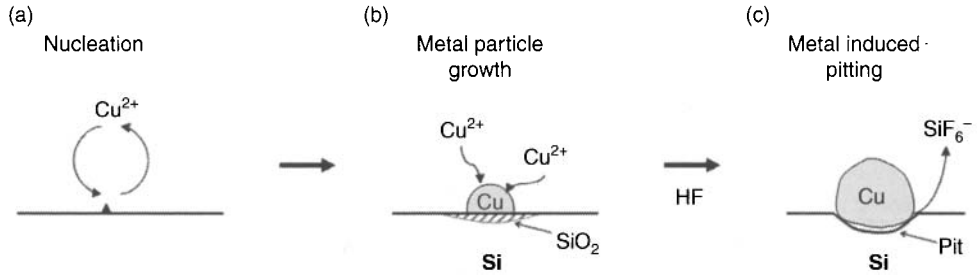


**Figure 13.14.** The mechanism of MIP in Cu/HF systems [43]. Reproduced with permission of ECS – The Electrochemical Society from Morinaga, H., Suyama, M., and Ohmi, T., *Journal of The Electrochemical Society.*

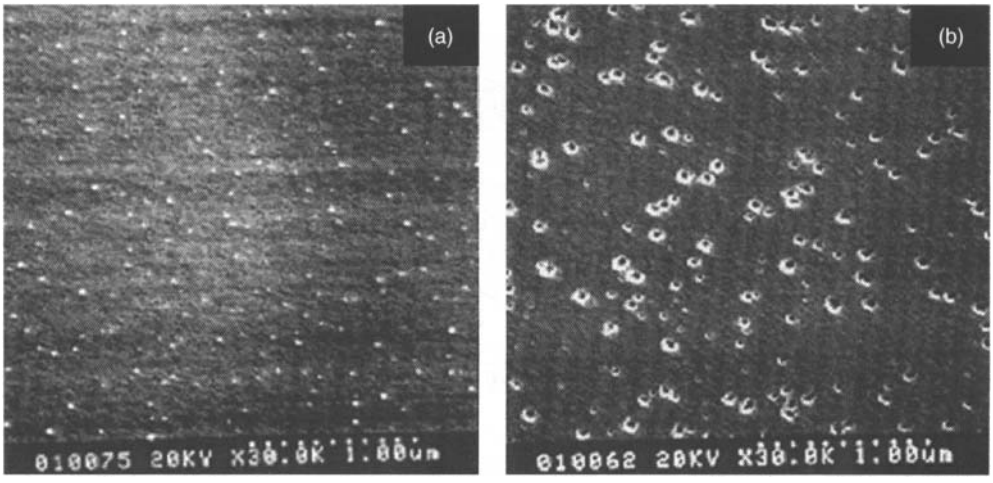


**Figure 13.15.** Scanning electron micrographs of (a) *in situ* p-doped Si and (b) on undoped Si surfaces after Cu contamination in a 0.5 wt% HF spiked with 1 ppm Cu using $CuCl_2$ for 3 min [48]. Reproduced with permission of ECS – The Electrochemical Society from Choi G.-M. and Ohmi, T., *Journal of the Electrochemical Society.*

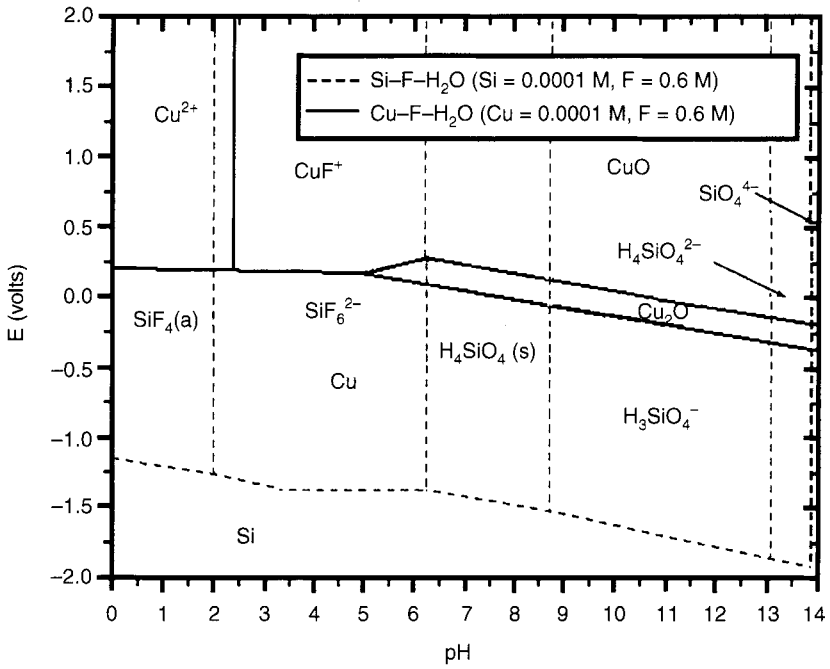


**Figure 13.16.** Pourbaix diagram of Cu-F-$H_2O$ system superimposed on that of Si-F-$H_2O$ system [49]. The shaded area emphasizes the redox potential lower than 0.2 V and in acidic $F^-$ conditions (pH < 6), where Cu metal formation is thermodynamically favorable. Used with permission of Srini Raghavan.

the oxidation-reduction potential of copper and silicon as function of pH in a fluoride-based solution [49].

When a silicon wafer is immersed in a copper-contaminated HF solution with pH < 6, the potential of the silicon wafer is above −1 V and the potential for metallic copper in this solution is usually below 0 V. At this point, the silicon fluoride and metallic copper are thermodynamically stable species, and as a result, the copper ion will reduce to copper metal and deposit or plate-out onto the silicon surface and the silicon will dissolve into solution. Using this approach, HF/oxidizer chemistries, such as $HF/H_2O_2$, $HF/HNO_3$, and $HF/HNO_3/H_2O_2$ are used to effectively remove copper and other noble metals from the silicon wafer surface [50, 51]. These cleaners, however, can significantly increase the micro-roughness of the surface during treatment. The addition of HCl in a HF-based solution to inhibit silicon roughening and pitting has been studied by several researches [52–54]. It was found that small amounts of HCl can suppress silicon pitting due to changing the passive surface state, speculated as Cl passivation due to large ionic size and decreasing the fluoride ion concentration [54]. The addition of surfactants/solvents to HF-based chemistries has also been proposed in order to modify the electric charges of both the wafer surface and particles to decrease metal deposition, to passivate the surface from attack, thus minimizing the surface roughness [55–57]. However, surfactants are only effective at low levels of metal contamination, and some surfactants may increase other contamination levels due to physical adsorption onto the bare silicon surface. The complete removal of the surfactant from the

wafer surface is also a challenge and if not done effectively can create detrimental problems downstream.

Another approach to deter contaminants from the wafer surface is to add metal complexing agents to the chemical etching solution and/or rinsing solution. The requirements are that they must be capable of complexing metals in solution and also be stable against oxidative breakdown from $H_2O_2$. Carboxylic acid-type chelating agents have been widely used to chelate metal ions of Cu, Ca, Fe, Co, Ni, and Zn [58–60]. Solutions of citric acid are used, similar to those for post-CMP copper cleaning [61]. Phosphonic acid chelating agent can also inhibit metal adsorption onto a wafer surface in SC-1 solutions [62]. The combination of oxidizer, chelating agent, and/or surfactant in HF-based etching solutions were reported by several researchers [63, 64]. These formulated solutions can effectively remove Cu contamination from the wafer surface lowering silicon surface roughness and minimizing surface pitting.

There has not been much published on formulated reclaim solutions for metal stack containing tests wafers with the exception of work by Beaudry *et al.* [63]. The authors studied the effects of various chemical additives to evaluate their ability to prevent copper redeposition in hydrofluoric acid solutions contaminated with copper ions.

Tests were performed that combined both an oxidant and metal sequestering agents to oxidize the metal films and subsequently suppress the electrochemical reaction that causes metal plating onto the silicon wafer in the presence of hydrofluoric acid contaminated solutions. The metal sequestering agent, referred to as a chelator, binds to the metal ions in solution eliminating their ability to interact with the exposed silicon surface. For example, after a clean wafer was immersed for 10 minutes in an optimized non-copper stripping solution that had been contaminated with copper, the concentration of copper on the wafer surface was on the order of $10^{13}$ atoms/cm$^2$ – an improvement of at least 200% over wafers that had been stripped by non-protected chemistry methods. Their investigations showed that it is possible to improve chemical stripping technologies that can withstand a large spike of copper contamination protecting all wafers within the wafer reclaim loop to reduce inadvertent copper cross-contamination of non-copper wafers with the introduction of appropriate additives; however, this study did not examine the loading capabilities of such a chemical stripping bath used as a reclaim solution. In addition, today's metal specs for reclaim are $< 5 \times 10^{10}$ atoms/cm$^2$ – far lower than the results attained by Beaudry *et al.* Thus, a reclaim solution that allows for the processing of hundreds, potentially thousands of copper stack wafers yielding surface metal levels of $< 5 \times 10^{10}$ atoms/cm$^2$, low defects and damage-free surface is necessary for high throughput wafer reclaim applications.

Besides improving the efficiency of the chemical etching process, other methods have also been investigated to prevent copper contamination. One method is to identify the composition of a film on the wafer surface using analytical techniques such as x-ray fluorescence (XRF) before and after the chemical etching steps, correlate the results of the measurement with a wafer type, and then sort [65]. This method can effectively isolate copper wafers preventing copper-containing wafers from mixing with non-copper containing wafer. Another method is to add a thermal processing step between the film removal process and the polishing process,

in which a silicon wafer is heated at 150–500°C for 15 min to 5 hrs depending on the type of silicon wafer (p-type or p-type) [30, 66]. This method utilizes a phenomenon in which heating a semiconductor substrate drives the copper toward the surface of the substrate, which can then be removed.

## 13.8 Formulated Reclaim Solutions

One of the driving forces for next generation formulated reclaim solutions is the capability of recycling wafers with no degradation of surface quality. Other drivers are cost reduction by decreasing wafer recycling times and increasing reclaim life, plus addressing environmental concerns.

Since a single commodity chemical cannot remove all layers in a single step, three separate chemicals (Figure 13.11) were traditionally needed to remove the stack of films individually. Formulated chemicals, as discussed in Section 13.7 can not only improve the effectiveness of traditional cleaning chemicals such as HF, but also reduce the number of baths required for optimal removal of films, residues, and contamination. One such approach is RegenSi® 74, formulated to provide a single-step process for removal of metal stack layers for copper BEOL integration that can replace the traditional three-step metals reclaim process for copper, barrier, and dielectric removal.

The formulation first removes the copper by an oxidizer (Ox), in Equation 13.6, and then additional copper metal is oxidized by one cupric ion to produce two cuprous ions, Equation 13.7. The $Cu^{+}$ is made water soluble with the help of coordination ions which are present in the formulation. The cupric etchant can be regenerated to its original state by oxidizing the $Cu^{+}$ ions back to $Cu^{2+}$ by the hydrogen peroxide and dissolved oxygen, Equation 13.8.

$$Cu_{(s)} + Ox_{(aq)} \rightarrow Cu^{2+} + H_2O_{(aq)} + O_{(aq)} \tag{13.6}$$

$$Cu_{(s)} + Cu^{2+}{}_{(aq)} \rightarrow 2Cu^{+} \tag{13.7}$$

$$2\,H^{+} + Cu^{+}{}_{(aq)} + O_{(aq)} \rightarrow Cu^{2+} + H_2O \tag{13.8}$$

The barrier and dielectric layers, comprising metal nitride and silicon oxide, respectively, are dissolved by the HF in the formulated solution. The $H_2SiF_6$ byproduct is also a very good at attacking Si-O-Si ether linkages found in the $SiO_2$ framework, and in turn continues the dissolution of the dielectric films.

The trace metal level on stripped wafer surfaces is less than $5 \times 10^{10}$ atom/cm$^2$ for most metals. Additionally the number of wet bench tanks that are required is reduced, and the effective throughput of the reclaim module is increased [67, 68].

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14

# Direct Wafer Bonding Surface Conditioning

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*Abstract*

The aim of this chapter is to describe the diverse surface conditioning processes that, alone or combined, allow direct bonding. For more than 20 years, direct bonding of Si and $SiO_2$ have been evaluated and applied for microelectronics, micro-technologies, and optoelectronic applications. More recently, direct bonding has been successfully performed on materials as diverse as Ge, SiGe, III-V, SiC, glass, quartz, diamond, sapphire, perovskite, and metals. The surface conditioning processes must take into account the nature of each material, the state of its surface (*i.e.* surface bonds, micro-roughness, topography) and its structure (*i.e.* amorphous, single crystalline, polycrystalline). Cleaning processes and surface preparation must be customized for each single or composite material to insure high quality direct bonding. For most applications, direct bonding involves hydrophilic surfaces which are well suited to spontaneous adhesion at room temperature. Surface preparations that result in hydrophilic surfaces will be discussed, and a short overview will also be given on direct bonding of hydrophobic surfaces. The importance of customizing surface conditioning processes will be illustrated for diverse direct bonding structures.

***Keywords:*** direct bonding, surface conditioning, surface cleaning, planarization, smoothing, wet conditioning, dry conditioning, brush scrubbing, surface plasma activation, UV-ozone cleaning, annealing

## 14.1 Introduction and Overview of Bonding

Direct wafer bonding consists of contacting two wafer surfaces without any adhesive or additional materials between the two surfaces to promote the adhesion (Figure 14.1). Direct bonding has been developed as an alternative route to many other bonding processes such as anodic bonding [1], thermo-compression bonding [2], eutectic bonding [3], glass fritting [4], and polymer adhesive bonding [5].

Direct bonding of surfaces has been used since the early 1960's and has strongly influenced the engineering of many innovative substrates and structures. Direct bonding allows different materials to be stacked together without concern for the crystalline relationship to one another. It is also well suited for layer transfer

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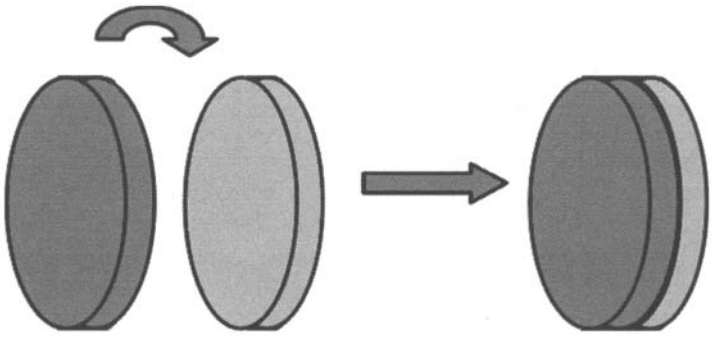

**Figure 14.1.** Direct wafer bonding at room temperature. Reproduced with permission of CEA-LETI.

techniques. Philips Labs developed one of the first applications: direct bonding of mirrors for flat mirror gas laser structures [6, 7]. Direct bonding of hydrophilic or hydrophobic surfaces is commonly performed in a clean room after physical and chemical surface conditioning. Smooth surfaces and suited surface bonds are needed to enable direct bonding. There also is a need to properly address key issues such as low particulate and metallic contamination levels with aggressive surface preparation requirements to achieve high-yielding, strong-bonding, and defect-free structures. Typically, bonding is performed at room temperature. The interaction between the two solid surfaces is a subject of considerable interest that has been extensively studied.

The main advantages of wafer bonding over other technologies are:

1. There is no need for a specific material (*i.e.* anodic bonding) or for an additional material (*i.e.* eutectic bonding, glass frit soldering, adhesive).
2. Stacked structures formed by direct bonding enable subsequent high temperature processes that would not be possible with polymer adhesive bonding or soldering (*i.e.* filler metal that has a low melting point).
3. Most direct bonded structures can be subsequently processed using standard micro-technologies and microelectronics manufacturing tools which is a key point for developing new stacked structures.

Processes have been developed and customized to enable stacking and the transfer of diverse layers. Varieties of materials as different as SiGe, Ge, III-V, SiC, nitride, garnet, sapphire, diamond, glass, quartz, perovskite, and metal, – bare or processed, can be direct bonded [8–11]. This approach opens a window enabling many types of innovative engineered substrates, device structures, and three dimensional (3D) integration applications.

The aim of this chapter is to describe various surface conditioning processes that, alone or combined, allow direct bonding. The importance of customizing surface conditioning processes is illustrated for diverse direct bonded structures in the first part of this chapter. The second part is devoted to planarization and smoothing processes required prior to direct bonding. In the third part, several wet conditioning

processes such as surface cleaning, brush scrubbing, and drying will be described for both silicon and silica. Then, two types of dry pre-bonding conditioning processes are presented: surface plasma activation and ultraviolet excited ozone (UV/$O_3$) cleaning. Afterwards annealing and thermal treatment prior to or subsequent to direct bonding in combination with other surface preparation processes are discussed, and specific conductive bonding processes are briefly presented.

## 14.1.1 Wafer Bonding for Semiconductor Applications

### *14.1.1.1 Silicon and Silica Direct Bonding*

For semiconductor applications, early reports on silicon or silicon dioxide surface direct bonding were first published in the 1980's [12–14]. Researchers showed that direct bonding is feasible thanks to van der Waals attraction, further strengthened by capillary forces, electrostatic Coulomb forces, and hydrogen bonding in the case of hydrophilic surfaces. These adhesion forces allow two mirror-polished wafers to bond at room temperature without application of an external force or glue.

The surface micro-roughness plays a key role in the bonding phenomenon. Statistical models of rough surfaces and the adhesive asperity contact are used to understand bonding mechanisms at nanometer scales [15, 16]. The research has shown that immediately after bonding, only a few asperities of the wafer surfaces are intimately in contact with one other in accordance with the Hertz model. These models have been shown to be well suited for most bonded structures.

After bonding at room temperature, bonding energies are still weak, typically 0.1–0.2 J/m$^2$ for hydrophilic silicon wafers, and the bonding is reversible. To increase the strength, high temperature thermal anneals typically are used to enhance the adhesion by creating covalent siloxane or silicon-silicon bonds [17–19]. During thermal annealing, the interface disappears and any reaction species that formed are evacuated from the structure. Figure 14.2 shows the variation of surface energy which is half the bonding energy as a function of annealing temperature

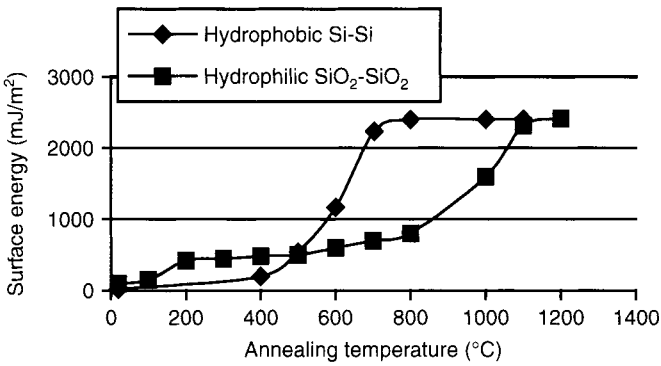


**Figure 14.2.** Variation of surface energies versus thermal annealing temperature for a) Si-Si hydrophobic bonded structures and b) $SiO_2$-$SiO_2$ hydrophilic bonded structures [19]. Reproduced with permission of Solid State Phenomena,Trans Tech Publications, from Moriceau, H., Rieutord, F., Morales, C., Charvet, A.M., Rayssac, O., Bataillou, B., Fournel, F., Eymery, J., Pascale, A., Gentile, P., Bavard, A., Mézière, J., Maleville, C., and Aspar, B. *Solid State Phenomena, Trans Tech Publications.*

for the bonding of a) two hydrophobic silicon wafers and b) two hydrophilic thermally oxidized Si wafers [19].

### *14.1.1.2 Silicon-on-insulator Structures*

In the 1980's, several direct bonding processes for wafers prepared with hydrophilic surfaces were developed for creating silicon-on-insulator (SOI) structures [9, 18, 20]. High temperature annealing processes were tuned to strengthen adhesion after bonding. Silicon-on-insulator structures can be considered as the most well known bonded structures thanks to their numerous applications in microelectronics, micro-technologies, micro-electromechanical structures (MEMS), biotechnologies, and optronics. Figure 14.3 shows a typical schematic for a SOI fabrication process consisting of silicon surface preparation before direct bonding of the two silicon wafers.

The process starts with a clean surface on which oxide is either thermally grown or deposited forming the buried oxide layer. Smoothing and additional cleaning are performed to prepare the surface for bonding. The bonding process then is performed including a thermal annealing step. Finally, the thinning can be done by mechanical techniques, such as grinding [20–22] or by chemical processes, wet or dry etching, or a lift-off technique [23]. Specialized processes, such as the SOITEC Smart-Cut™ technology [24–27] or the Canon Eltran® process [28] were developed primarily for thinning one of the two wafers in order to obtain a thin silicon layer to form a buried insulating oxide layers (Box). Within a few years after the initial introduction of these techniques, the quality of SOI layers could be compared to single crystal bulk silicon wafers. Now SOI wafers formed by direct bonding are produced for high volume manufacturing processes.

### *14.1.1.3 3D Integration Wafer Level Packaging*

Wafer bonding using mechanical or chemical thinning is well suited to transfer layers with circuit features already in place because it does not affect the integrity of the transferred layers nor the device and preserves the functionality of the device. Additionally, it offers a solution to stack devices with different functions

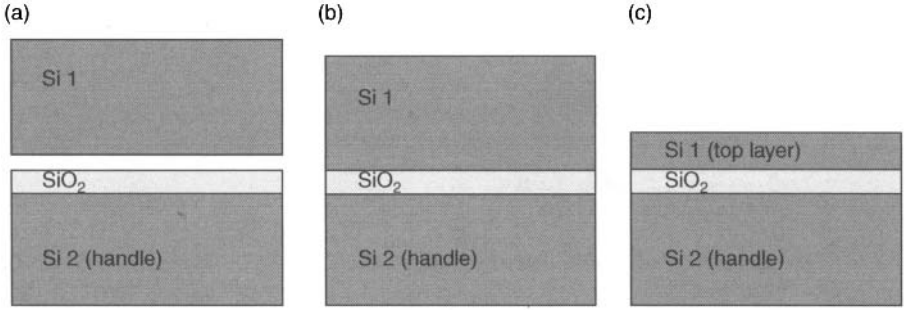


**Figure 14.3.** Schematic of a typical process for SOI fabrication; a) surface preparation that can include oxide formation, smoothing, and cleaning, b) direct bonding of the two Si wafers with an oxide layer between them, and c) thinning down of one wafer to obtain a top silicon layer. Reproduced with permission of CEA-LETI.

including 3D integration or wafer level packaging. Moreover, direct bonded structures remain compatible with most of the subsequent microelectronics processes.

Direct bonding of processed wafers, especially when they include several layers of metallic interconnections such as bond pads, requires control of the surface states to allow high yields and efficient bonding. Usually, only low temperature bonding treatments <400°C are used because of the low melting point of aluminum, if present, and other material limitations, such as low dielectric constant insulators. However, the maximum bonding temperature chosen is determined by the materials present on the wafers.

Usually, processed wafers exhibit diverse surface topographies. It is necessary to perform a surface treatment to fulfill direct bonding specifications – hydrophilicity, smoothness, and particle contamination. Silicon oxide layers can be deposited on top of processed wafers, and planarization can be performed to smooth the surface to meet the smoothness requirement. Bonding energies obtained from planarized deposited $SiO_2$ layers are strong enough to allow subsequent mechanical and chemical thinning of at least one wafer. Thus, device layers may be bonded onto new holder substrates either by a "single transfer" or by a "double transfer" [29]. Single transfer is defined as when the initial top surface of the device layer is buried at the bonding interface. Double transfer is defined as the initial top surface of the device layer is the top surface of the final bonded structure as depicted in Figure 14.4. Bonding various layers (*e.g.* CMOS – complementary metal oxide semiconductor – processed SOI wafers) onto diverse supports (handle wafers) such as silicon, fused silica, sapphire, and other processed wafers was demonstrated both by single and by double transfer [29] illustrating a wide variety of applications for 3D integration.

### *14.1.1.4 Diverse Material Stacking*

Direct bonding technologies also enable the formation of stacked structures using diverse materials. For example, direct wafer bonding enables stacking a single-crystal film on a substrate when it is not possible to grow it by epitaxial processing. This is the case if the substrate surface is an amorphous layer, or if the lattice mismatch between film and substrate lattice parameters is too high to allow epitaxial

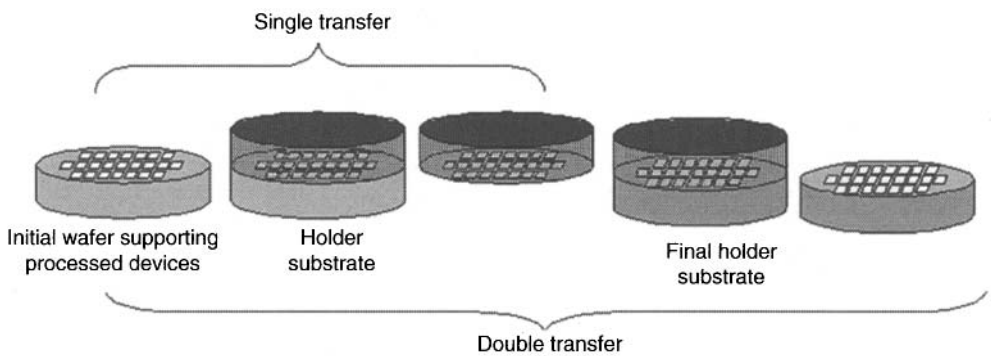


**Figure 14.4.** Transfer of an integrated circuit thin film pattern onto a substrate [29]. Reproduced with permission of ECS – The Electrochemical Society from Aspar, B., Lagahe-Blanchard,C., and Moriceau, H., *Semiconductor Wafer Bonding: Science, Technology, and Applications VIII.*

growth. Bonding of two hydrophobic silicon wafer surfaces that have very different doping concentrations and possibly a lattice mismatch and then thinning one of the two wafers enables the fabrication of a thick single crystalline Si film [30]. A single crystalline layer can be transferred onto a low cost substrate, or onto a substrate with a matched coefficient of thermal expansion, or onto a substrate with a matched or a different lattice parameter enabling the fabrication of new substrates for epitaxy.

Diverse active top layers such as <100>/<110>hybrid oriented Si, strained-Si, and SiGe with thicknesses between 5 nm and 100 μm on 300-mm Si wafers can be fabricated with these techniques. Bonded structures can be manufactured with a variety of buried intermediate layers (*i.e.* dielectric, conductive) combined with a diversity of substrates (*i.e.* Si, glass, sapphire) [26, 27].

### *14.1.1.5 Patterned Silicon-on-insulator Wafers*

Fabrication of bonded patterned SOI structures (PSOI) is required for specific applications where $SiO_2$ mesas are surrounded by either Si or $SiO_2$ areas. This approach permits the transfer of patterned or unpatterned layers [29, 31, 32]. Specialized chemical mechanical planarization (CMP) and cleaning processes are needed in order to achieve flat, smooth, and contamination-free surfaces for the various materials to be bonded (Figure 14.5) [33]. For instance, dishing induced by selective polishing or etching can be the cause of poor bonding.

### *14.1.1.6 Germanium-on-insulator Wafers*

Germanium-on-insulator (GeOI) substrates are fabricated for high frequency microelectronic or optoelectronic applications. In order to obtain good quality GeOI substrates, the germanium surfaces for direct bonding must be properly prepared by controlling the germanium oxidation. Germanium is not passivated when cleaned with a standard SC-1 (standard clean-1) wet chemical process because a thick oxide is grown as compared to silicon that forms a chemical oxide. Chapter 12 outlines methods for passivating the Ge surface and

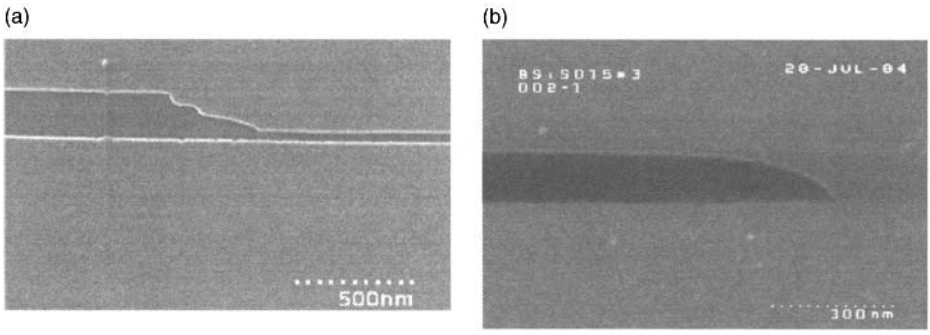


**Figure 14.5.** Scanning electron microscope images of a) a PSOI structure containing both ~35-nm thin and 200-nm thick Box areas and b) a PSOI structure with a 150-nm thick Box area and direct Si-Si bonded area [33]. Reproduced with permission of IEEE from Moriceau, H., Yalicheff, C., Gorla, C., Charvet, A. M., Morales, C., Zussy, M., Dechamp, J., Kernevez, N., Letertre, F., Ghyselen, B., *Proceedings IEEE SOI Conference.* © 2004 IEEE.

the physics and chemistry of the reactions. Specific passivation of Ge surfaces for bonding applications are discussed in Section 14.3-4.

### 14.1.2 Wafer Bonding Surface Conditioning

For more than 20 years, direct bonding of silicon and $SiO_2$ has been used. Many techniques and surface conditioning processes have been developed for Si or $SiO_2$ surfaces (both film and bulk). The nature of each material, the state of its surface (*i.e.* surface bonds, micro-roughness, topography) and its structure (*i.e.* amorphous, single crystalline, polycrystalline) must be taken into account to develop new surface conditioning processes. Surface cleaning and surface preparation have to be customized for every single or composite material to insure high quality direct bonding. For most materials, conditioning processes result in hydrophilic surfaces that are well suited to spontaneous direct adhesion at room temperature. Even if less commonly used, hydrophobic surfaces are also well suited for direct bonding. Both surface states are discussed hereafter.

Large non-uniformities of surface flatness (bowing, warpage, and micro-roughness) can cause areas to fail to bond properly [34–36]. In the case of commercially available silicon wafers, bowing and warpage values of approximately a few microns and root mean square (RMS) surface roughness of less than 0.5 nm must be achieved for high quality direct bonding. Bonding strength is shown to be strongly correlated to such parameters [16, 35, 37, 38].

Direct bonded structures often need to be strengthened through post-bonding thermal treatments. However, at the same time, a number of issues such as degassing species, trapped particles, and insufficient interfacial bonding can cause bonding defects. Avoiding these potential problems requires that conditioning processes must be specifically tuned to obtain high-yielding bonded structures.

## 14.2 Planarization and Smoothing Prior to Bonding

### 14.2.1 Chemical Mechanical Planarization

Wafer bonding requires smooth, flat, and clean wafer surfaces. To insure effective bonding, patterned wafers must be planarized to create flat, smooth, non-hazy, and defect-free surfaces. Minimizing wafer deformation, such as bowing, is needed to create a flat surface for a high-quality bond. Any topographical asperity, such as a step from a device feature, can prevent intimate local bonding and even a small pit or particle can result in an area that does not bond. Since bonding occurs at the atomic level and is induced by van der Waals attraction forces between the Si-OH groups or in between water molecules adsorbed on the surface Si-OH groups, roughness can interfere with the formation of a strong bond. In some cases, very rough surfaces can prevent bonding.

To address these roughness and nano-topographical issues that occur when transferring circuits onto a handle wafer or for 3D stacking, encapsulation by an oxide layer such as tetraethyl orthosilicate (TEOS) deposited by chemical vapor deposition (CVD) or reflowed boron phosphorous silicate glass (BPSG) layer is

commonly used to allow subsequent planarization and smoothing [39]. Chemical mechanical polishing is typically used to planarize the wafer yielding a sufficiently flat and smooth surface [40].

For wafer bonding, planarization requires specific metrology methods capable of monitoring global wafer deformation, step height, and nanometer scale topography. Typical tools are mechanical profilers, optical interferometers [41], and atomic force microscopes. These methods can characterize the wafer surface before and after a CMP process and help optimize thickness removal. Flatness measurements, such as non-contact capacitive measurements, are useful to evaluate local and global non-uniformities such as bowing or warpage. To monitor thickness, ellipsometry or reflectometry are useful and can even be implemented *in situ* on the CMP tools allowing endpoint detection that helps prevent variations during the process.

Some key criteria indicate the performance of the CMP process:

1. Removal Rate. Removal rate must be well controlled to prevent wafer-to-wafer thickness variations when there is no *in situ* thickness monitoring. Choice of removal rate is a trade-off between process performance and throughput.
2. Selectivity. Planarization selectivity for different materials on patterned wafers can lead to local variations in removal rate. Choice of selectivity affects process performance and planarity.

For oxide layers, planarization efficiency, $P$, is expressed as:

$$P = \frac{S}{T_{tot} - T_{\text{cov}}} \times 100\% \tag{14.1}$$

where $S$ is the step height, $T_{\text{tot}}$ is the total oxide thickness over the step (prior to CMP), and $T_{\text{cov}}$ is the oxide thickness that will remain over the step after CMP. Planarization efficiency evaluates the ideal encapsulated oxide thickness required to obtain a full planarization. Typical values are around 80%.

Degree of planarization (DOP) is expressed as:

$$DOP = 1 - \frac{T_{post}}{T_{pre}} \tag{14.2}$$

where $T_{\text{pre}}$ is the distance between the peaks and valleys on an oxide surface before CMP, and $T_{\text{post}}$ is the distance between peaks and valleys on an oxide surface after CMP. It represents how flat the surface is after the planarization process. Typical values are >95%.

Within wafer non-uniformity (WIWNU) and wafer-to-wafer non-uniformity (WTWNU) are expressed as:

$$WIWNU = \frac{s\left(\{T_i\}\right)}{x} \tag{14.3}$$

$$WTWNU = \frac{s(\{T_n\})}{X} \tag{14.4}$$

where $x$ is the average of thickness measurements within a wafer and $s(\{T_i\})$ is the standard deviation of thickness measurements within a wafer. Within wafer non-uniformity represents global uniformity across the wafer. Wafer-to-wafer non-uniformity shows the dispersion from wafer-to-wafer where $X$ is the average of thickness measurements from wafer-to-water and $s(\{T_n\})$ is the standard deviation of thickness measurements from wafer-to-water. Uniformity of a few percent (~3%) is common for both values in CMP [42].

### 14.2.2 Surface Smoothing

Another purpose of CMP in wafer bonding application is smoothing. Deposited materials, such as TEOS or polycrystalline silicon (polySi) need to be smoothed because of their high surface roughness. After deposition, roughness measured by high frequency atomic force microscopy (AFM) on (1 × 1) μm² or (2 × 2) μm² area scans can reach RMS values from a few angstroms (in case of PECVD – plasma enhanced CVD TEOS) to hundreds of angstroms (for some polySi depositions). Researchers have determined that ~0.6 nm RMS is a threshold for micro-roughness above which wafers covered with TEOS oxide layers do not bond [17, 36, 43]. Therefore, decreasing surface micro-roughness as low as possible improves bonding quality. Short time CMP (referred to as touch-chemical mechanical polishing) is one method to reduce surface roughness. This solution can be included in the planarization step of patterned wafers to obtain smooth and flat surfaces. Touch-CMP is used with the same materials as planarization, but smoothing requires smaller amounts of material be removed. Removing only a few nanometers is usually enough to decrease roughness whereas planarization usually removes hundreds of nanometers. Figure 14.6 shows optical interferometer measurements of micro-roughness

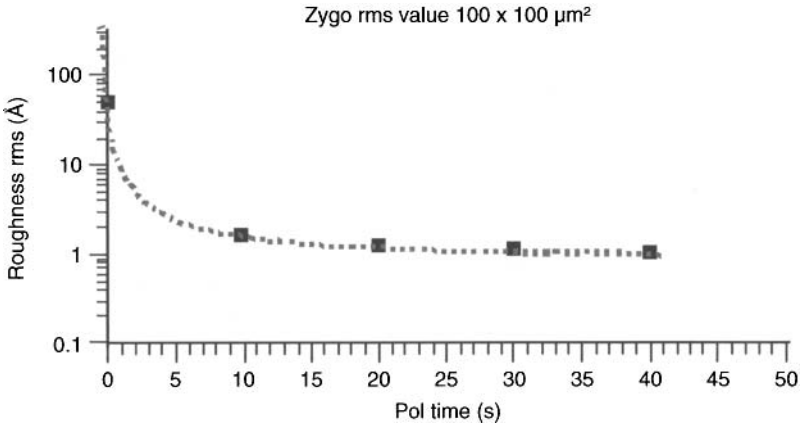


**Figure 14.6.** Micro-roughness RMS value *versus* polishing time on polySi, as measured by a Zygo Corp. optical interferometer profiler. Reproduced with permission of SOITEC.

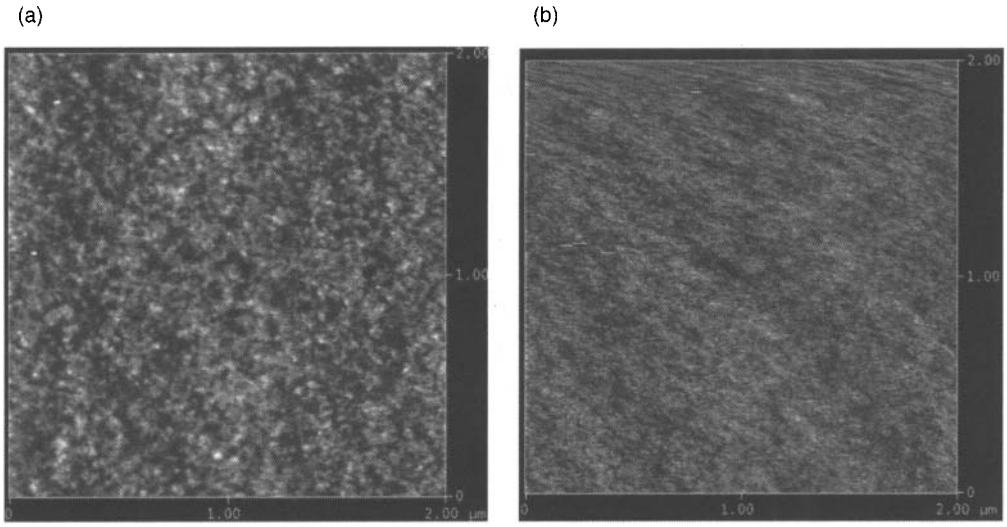


**Figure 14.7.** Atomic force microscopy scans of (2 × 2) $\mu m^2$ samples a) before and b) after 4 nm touch-CMP removal of CVD oxide films. The roughness significantly decreases after touch-CMP. Reproduced with permission of SOITEC.

(Å RMS) *versus* polishing time on polySi layers. Optical interferometer surface profiler (Zygo Corp.) measurements are performed on (100 × 100) $\mu m^2$ area. Typically, the use of touch-polishing is enough to obtain the low micro-roughness values required. A 10-15 sec polishing time corresponds to approximately 10–20 nm removal resulting in roughness values of approximately 0.1 nm RMS.

The touch process can also address the high density of defects obtaining a particle-free, scratch-free, and non-hazy surface. In Figure 14.7, 2 × 2 $\mu m^2$ AFM scans show a CVD oxide surface a) after deposition and b) after 4-nm touch-CMP removal. The roughness decreased from 0.5 nm to 0.26 nm RMS. Soft pads were used to obtain this result. Their high compressibility allows the removal process to follow the global shape of the wafer. Typically, polishing pads used in this operation are highly porous (class II), such as Rohm & Haas Polytex™ [44].

The slurries are usually basic solutions with colloidal silica particles (*e.g.* Klebosol™ 1501 from Rohm & Haas, for silicon dioxide), and typically, the diameter of the particles is a few tens of nanometers. Similar to planarization, the slurry is a key contributor to the process. Dilution or temperature will have a large influence on touch-CMP behavior. Other key parameters are the same as those found in planarization: down force, platen and carrier speed. Backside pressure must be adjusted to obtain the best results.

Metrology to monitor the touch-CMP surface is significantly different from planarization. The main purpose is to smooth and create a defect-free surface. The defects introduced by CMP include scratches resulting from dried slurry residue or embedded particles in the pad. For that reason, CMP-induced defectivity must be controlled. Defect measurement techniques such as light scattering (*e.g.* using SP2 tool from KLA-Tencor) combined with scanning electron microscopy (SEM) are used. Figure 14.8a shows a SP2 light point defect map of a 300-mm polySi

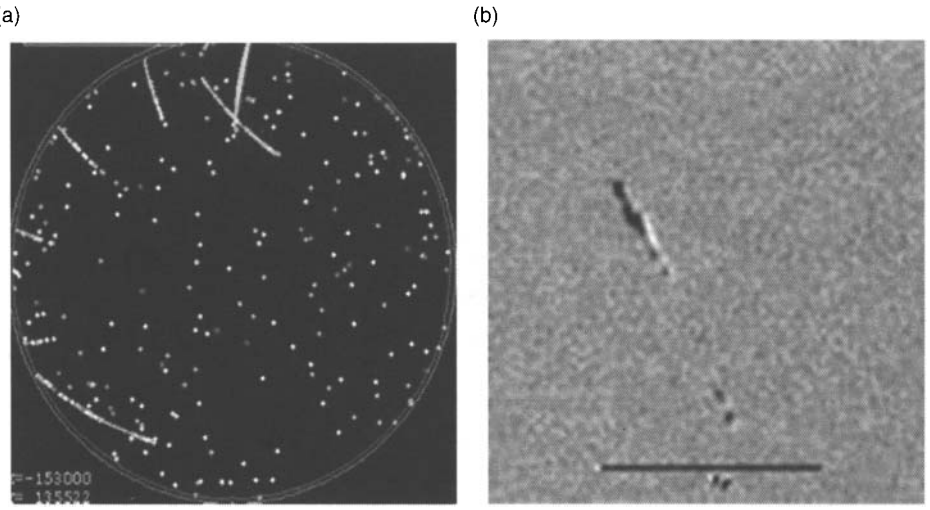


**Figure 14.8.** a) KLA Tencor SP2 map of light point defects (LPD) and scratches characterized on a polySi surface. b) SEM image of a scratch. Reproduced with permission of SOITEC.

coated wafer with scratches detected after touch-CMP. Figure 14.8b shows a SEM image of a scratch detected by the light scattering tool. In some instances, such as strained SOI or strained SiGeOI processes, CMP is a solution to remove crosshatch roughness before bonding [45].

Another important parameter in the touch-CMP process is surface micro-roughness measurement; atomic force microscopy is an efficient means of monitoring roughness because it can measure surface morphologies and power spectral densities on a large range of sample areas $(0.1 \times 0.1)\ \mu m^2$ to more than $(100 \times 100)\ \mu m^2$.

Considering the purpose of CMP is to remove material, uniformity and removal rate are important metrics that necessitate optimization. For touch-CMP, the amount removed is very small; therefore, uniformity becomes less of a concern. While it still should to be taken into account, within wafer uniformity is not as critical as in planarization. Removal rate remains important because it corresponds to process repeatability – an out of spec value could reveal process issues. Roughness and defectivity are the main output parameters that must be monitored in touch-CMP to insure a high-quality wafer bond without any defective areas.

## 14.3 Wet Cleaning and Surface Conditioning Processing

Wet cleaning and surface conditioning for wafer bonding is used for:

1. Surface state creation – either a hydrophilic or a hydrophobic surface is created.
2. Surface cleaning – removing particles, organic, and metallic contamination from the surface.

To create the proper surface state for bonding, the wafers must be prepared adequately. For hydrophilic bonding, hydrogen bonds are formed between polarized molecules. In silicon oxide-silicon oxide bonding or silicon-silicon oxide bonding, silicon oxide can be a thin native oxide or a chemically generated oxide or a chemically modified oxide. In these instances, hydrogen bonds form between Si-OH groups generated on the silicon oxide surface or in between water molecules adsorbed on the same Si-OH groups [10, 18, 46–48].

For the opposite case of hydrophobic bonding when no oxide is present or when a high temperature oxide is grown, interfacial bonding occurs due to pure van der Waals forces. To obtain a hydrophobic surface, the silicon wafer is treated with hydrofluoric acid (HF) which leads to a hydrogen terminated (Si-H) surface. Reference [49] thoroughly discusses the hydrogen passivation of silicon surfaces. Another example is silicon oxide in which the surface is saturated by siloxane bonds such as found in high temperature thermal oxide. Due to the high temperature, the lack of Si-OH surface groups renders the surface hydrophobic and allows only bonding via van der Waals forces [50].

In addition to having the proper surface, the wafer must also be adequately cleaned to remove surface contamination that may disturb the establishment of close wafer contact. Contamination such as particles, organic moieties [51], and metallic species all affect bonding quality. Particles will locally disturb chemical bond formation. Organic compounds from the ambient environment or from storage boxes can inhibit the establishment of chemical bonds. Metallic contaminants primarily come from the process tool or from consumables, such as chemicals, and can affect the electrical properties of the joined materials [52].

For instance, Maleville *et al.* reported the importance of surface preparation to create void-free bonded structures for the Smart Cut™ technology [17]. They showed a strong relationship between particle sizes and the presence and size of voids at the SOI bonding interfaces. The researchers accurately located particles on the wafer surfaces prior to direct bonding showing ~0.3-μm sized particles induced bonded defects several millimeters in diameter.

The chemical formulations used for wafer conditioning must preserve the surface micro-roughness to insure bonding strength and quality. The following section details the different chemistries commonly used for wafer bonding preparation to obtain optimal hydrophilic properties, surface roughness control, and particle and contamination removal.

### 14.3.1 Process Flow

It is preferable to start the critical pre-bonding wet cleaning with formulations able to remove organic contaminants. Two approaches are commonly used based either on sulfuric acid ($H_2SO_4$) and hydrogen peroxide ($H_2O_2$) mixture (SPM) or ozone diluted in deionized water (DIW). To remove particles after the organic removal step, surfaces are usually cleaned by ammonium hydroxide ($NH_4OH$) hydrogen peroxide mixture (SC-1) which, furthermore, renders surfaces highly hydrophilic. After a DIW rinse, the metallic contamination possibly due to the previous SC-1 step or metallic contamination already on the surface can be easily removed by a

hydrochloric acid (HCl) hydrogen peroxide mixture (SC-2). An optional scrubbing step and a drying step are then performed immediately prior to bonding.

### 14.3.2 Sulfuric Acid-Hydrogen Peroxide Mixture

Sulfuric acid-hydrogen peroxide mixture (SPM) is a strong oxidizing agent that effectively removes hydrocarbon contamination. The chemical properties and cleaning mechanisms of SPM are thoroughly discussed in Chapter 2.

Additionally, SPM can react with the Si-$CH_x$ groups replacing the organic groups and form Si-OH groups [53]. The elevated reaction temperature enhances surface oxidation producing an approximately 1.5-nm thick chemical oxide. The contact angle of a DIW droplet on the surface can be used to evaluate the wettability of a Si surface. With poor surface activation, (*i.e.* low Si-OH surface density) the contact angle is >10° while highly hydrophilic surfaces have contact angles of <3° [36]. After SPM treatments, the contact angle is on the order of 10–15° which is similar with what can be obtained with a long time water rinse. Sulfuric acid hydrogen peroxide mixture can effectively remove surface contaminants; however, the very low levels of $OH^-$ in the bath do not allow metallic contaminant precipitation and are not likely to be able to remove metals.

Sulfuric acid hydrogen peroxide etching of $SiO_2$ is very low (about 0.01 nm/min for a 3:1 $H_2SO_4$:$H_2O_2$ mixture at 140°C); consequently, this solution does not affect surface micro-roughness. On a Si wafer, the surface potential of SPM is positive because of its very low pH. Negative particles from the bath are attracted to the wafer resulting in surface contamination. Similar particulate contamination occurs on oxide layers but to a lesser degree than on Si due to screening of the surface potential by the oxide layer.

### 14.3.3 Deionized Water/Ozone Cleaning

Ozone dissolved in DIW ($DIO_3$) is a strong oxidizing agent and easily able to decompose organic impurities. However, its low solubility limits the number of available reactive species, and thus, limits the oxidation capability of the solution and its oxidation kinetics. The oxide thickness cannot exceed 0.75 nm, and oxide growth will stop at this maximum value regardless of the ozone concentration in the DIW [54]. Dissolved ozone can effectively remove a large variety of organic compounds – even compounds that cannot be decomposed by other chemistries, such as cyclic organic or carbon-carbon double bonds. However, due to its limited concentration, it is not possible to remove a large quantity of organic residue; therefore, it is more adapted to the removal of airborne contaminants. It has been shown that 6 ppm ozone dissolved in DIW at 20°C is comparable to SPM at 120°C with an exposure time of 10 min [55] to clean these contaminants. Ozone cleaning has the advantage of lower temperature, simplicity, reduced consumption, and reduced chemical waste.

However, $DIO_3$ cleaning does not remove metals or particles. Indeed, ozone does not react with any metal. Ozone does not etch Si or $SiO_2$, and thus, particle detachment caused by lift off does not occur when using this chemistry. Ozone can

be employed with other chemistries to passivate the surface by the creation of a thin oxide layer or to remove organic compounds.

### 14.3.4 Standard Clean-1 Surface Conditioning

For the purpose of wafer surface preparation, SC-1 cleaning (or ammonium hydroxide hydrogen peroxide mixture – APM) is mainly used to remove particulate contamination and to render a surface hydrophilic [56]. A thorough discussion of this process is found in Chapter 2. At the same time, the etching of Si or $SiO_2$ by SC-1 will lead to surface roughening. It will then be necessary to properly define cleaning conditions – the mixture ratio and concentration and temperature, and to optimize particle removal – hydrophilic surface properties and surface roughening.

This basic solution effectively removes particles from silicon surfaces. Simultaneously, it oxidizes and slightly etches undercutting and removing particles from the surface. At the same time, the elevated pH of the solution (approximately 9) induces a zeta potential of the same sign for both the particles and the oxidized surface. The resulting electrical repulsion forces particulate contaminants into the solutions. Therefore, SC-1 silicon surface cleaning is very efficient, but SC-1 is less efficient on thermal oxide because of a lower etching rate. Megasonic energy can also be employed to enhance particle removal efficiency [57–59].

While the soft chemical etching of SC-1 efficiently removes particles by undercutting, this isotropic etching increases surface micro-roughness [60]. Surface roughening limits the formation of hydrogen bonds; therefore, SC-1 conditions must be optimized. Because $OH^-$ ions are responsible for oxide etching by the formation of $HSiO_3^-$ ions, etching rates or surface roughening are affected by parameters that change the hydroxyl interaction with the oxide, such as bath temperature, cleaning duration, and ammonium hydroxide concentration. A thorough discussion of the reaction is presented in Chapter 2.

The equilibrium between surface oxidation and oxide etching leads to the creation of a chemical oxide with a thickness of about 0.8–1.2 nm depending on the mixture concentration and temperature. This chemical oxide renders the surface hydrophilic. At the same time, the oxide etching generates dangling bonds through the departure of $HSiO_3^-$ ions that are replaced by $OH^-$ ions from the basic solution [57]. The resulting surface is covered by Si-OH groups on which water molecules can adsorb. After SC-1 cleaning, the wafer surface is very hydrophilic. The wettability test using the static contact angle of a water droplet becomes irrelevant in case of SC-1 cleaning since the droplet spreads out quickly, and the contact angle stabilizes at around 3°. Preparation of Si hydrophilic surfaces requires the formation of surfaces terminated by silanol groups and adsorbed water. When initiating direct bonding, a few monolayers of water are trapped at the bonding interface enabling hydrogen bonding between the two wafers at room temperature [48, 61–65].

When processing germanium substrates, SC-1 can result in issues because the germanium is not passivated by this formulation. This cleaning process produces an uncontrollable germanium oxide growth and also etches the surface. To address this issue, specific HF-based cleaning processes have been developed that result in passivated germanium surfaces [66] that are outlined in detail in Chapter 12. Such

cleaning processes enable low Ge consumption, low metallic contamination levels, high particle removal efficiency, and minimal degradation of the surface smoothness. Their efficiency for particle removal from Ge surfaces had been tested [67]. Deguet *et al.* intentionally contaminated Ge test wafers with 0.5-μm $SiO_2$ spheres and after cleaning, particle removal efficiency (PRE) was measured ~98%.

Standard Clean-1 can induce metallic contamination of surfaces that is exacerbated by elevated pH. Iron physisorbs while aluminum, copper, and calcium deposit by chemisorption [68]. Ultrapure chemistries are needed to limit precipitation of these metallic contaminants. For high volume manufacturing, SC-1 bath aging should be optimized to limit metallic contamination caused by the processing of large numbers of wafers even though these wafers have low inherent contamination levels. For this reason, SC-1 cleaning is not used alone and is generally followed by an acid solution cleaning such as SC-2 or HF.

### 14.3.5 Standard Clean-2 Cleaning

Standard Clean-2 or HPM (hydrochloric acid hydrogen peroxide mixture) is used after an SC-1 bath to remove metallic contamination (the RCA cleaning sequence) [69]. Chapter 2 thoroughly reviews this chemistry formulation and RCA cleaning. A 0.6-nm chemical oxide is left after an SC-2 cleaning on an initially bare silicon surface while no silicon oxide etching occurs during SC-2 [18, 47, 54].

The very low pH of SC-2 leads to the degradation of the hydrophilic surface property. After SC-2, the DIW contact angle is approximately 7–15°. The positive zeta potential induces attraction of negatively charged particles that can lead to contamination of the Si or oxide surfaces.

In the case of hydrophilic bonding, SC-2 concentration and temperature must be adjusted to optimize metal removal efficiency with limited degradation of wafer surface hydrophilicity and to minimize surface particle contamination.

### 14.3.6 Wafer Brush Scrubbing

Because wafer bonding is strongly affected by particles, polyvinyl alcohol (PVA) brush scrubbing is an effective means of surface preparation before bonding. Propelled into the mainstream of semiconductor wafer cleaning in the 1990's, brush scrubbing is considered one of the most effective methods for removing particles, especially slurry residues after CMP [70].

Early brush scrubbers were constructed of nylon and caused damage to the wafer surface. However, using brushes made of PVA, a highly compressible sponge-like material (~90% porosity), shown in Figure 14.9, permits particle removal without any damage to the surface. Brush scrubbing can remove particles on the order of a micrometer as well as nanoparticles, of sizes ~0.1μm [47, 71].

The mechanism of particle removal by brush scrubbing is:

1. Particles are mechanically dislodged from the wafer surface by the PVA brush.
2. Particles are carried away from the wafer surface by a liquid (usually DIW) that is continuously dispensed on the wafer and the brush.

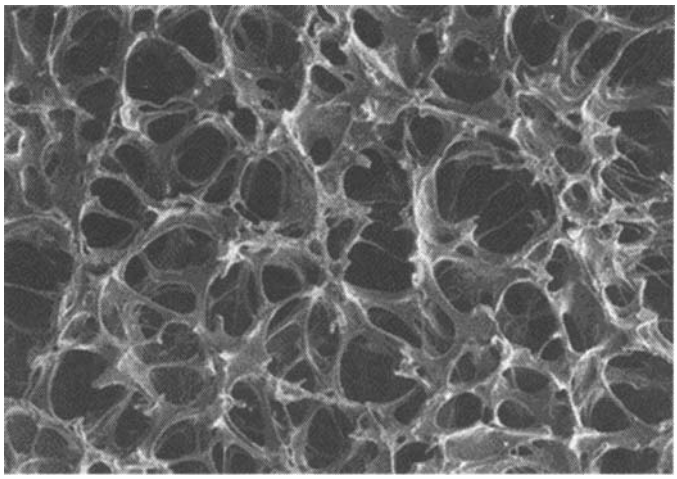

**Figure 14.9.** Scanning electron micrograph illustrating the porous structure of PVA material [72]. Reproduced with permission of Rippey.

To avoid reattachment of the particles to the wafer surface and brush loading (attachment of the particles into the porous brush structure), electrostatic interactions, and in particular, Zeta potential must be controlled with appropriate media. This is commonly obtained with high-pH solutions, such as dilute ammonium hydroxide in a concentration range of 0.1–2 wt%.

In addition to the nature of the chemical solution dispensed and its flow rate, particle removal efficiency is driven by the mechanical properties of the PVA brush, the pressure applied by the brush on the wafer surface, the overall kinematics of the brush and the wafer, and the cleaning time [73, 74].

In the case where surface preparation before bonding includes a CMP step to reduce surface nanotopography and micro-roughness, double sided brush scrubbing is recommended to remove slurry residues on the wafer front and back surfaces. The brush scrubber can be integrated into the CMP tool or be a stand-alone tool. To further increase the void-free bonding yield, single-side brush scrubbing can also be performed immediately before wafer mating. Typically, automatic bonding tools include a single side brush scrubbing station, as illustrated for an EVG tool in Figure 14.10 [75].

## 14.3.7 Wafer Drying

### *14.3.7.1 Equipment*

Wafer drying is usually the last step in the chemical cleaning sequence required for wafer bonding. Drying techniques have been widely investigated and many types exist: from the basic centrifugal dry under a $N_2$ atmosphere, to the single-wafer spin dry (that may be assisted by light heating), to the more advanced drying techniques using the surface tension gradient effect with isopropyl alcohol (IPA), also called Marangoni drying [76–78]. The Rotagoni™ system, a single wafer centrifuge operating at low speed utilizing the surface tension gradient effect,

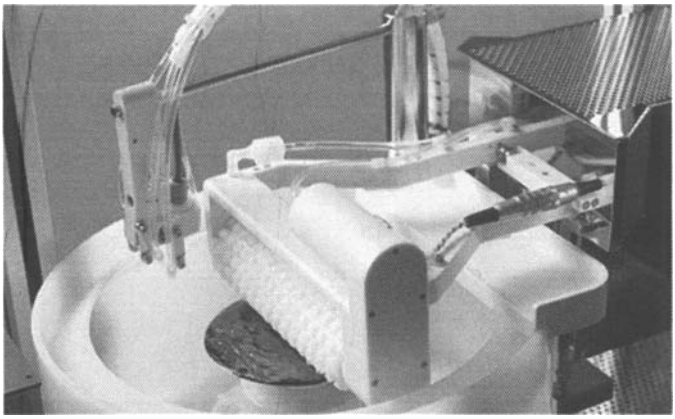

**Figure 14.10.** Single side brush scrubbing module integrated onto an automatic bonding tool [75]. Reproduced with permission of EV Group (EVG).

combines spin-rinsing and IPA drying [79]. Drying methods are discussed in detail in [80].

More recently, new solvents that offer very low surface tension referred to as low gamma solvents (LGS) [81] have been introduced for drying specially targeting wafer bonding applications. Already well known chemical compounds have been evaluated again for this purpose, such as chlorofluorocarbons (CFC), perfluorocarbons (PFC), and hydrofluoroethers (HFE).

Wafer dryers have progressed from batch systems with 25 wafers/run using a spin technique to larger batch systems processing up to 200 wafers/run to a single wafer platform with multiple single wafer modules in a single platform.

Cleaning and drying of silicon surfaces by lamp illumination has been also reported [82]. Cleaning can also be performed using a mix between lamp illumination and the new low surface tension application as well as using temperature modifications to optimize drying in the shortest time period to increase throughput.

### *14.3.7.2 Analysis*

For hydrophilic wafer bonding applications, the density of Si-OH groups generated by the chemical cleaning sequence is impacted by the drying step. In the case of hydrophobic bonding, the native oxide is removed from the surface by HF-based solutions, and the drying step must maintain the Si-H termination as long as possible. For an optimum process, the process time between the cleaning/drying step and the direct bonding step must be as short as possible. Solvent purity and its $H_2O$ content as well as the level of dissolved oxygen in the DIW rinse must be controlled to avoid watermarks [83]. In addition, drying methods should also consider cost and environmental issues.

Preventing metallic contamination during drying is a key point because any metallic residues on the surface would be encapsulated at the bonding interface and may lead to electrical reliability issues. This is strongly dependent upon construction materials used in the wafer cleaning system, and also on the DIW

rinse and the grade of the chemicals used. Organic contamination is another concern since it affects wafer bonding by significantly decreasing the Si-OH group density that may be introduced from the liquid or vapor solvent used for drying [81].

Fourier transform infrared-multiple internal reflection (FTIR-MIR) spectroscopy [17] and high-energy X-ray reflectometry (HEXRR) [84] are sensitive techniques to characterize the bonded interface. Figure 14.11 shows the results of FTIR-MIR characterization performed after low gamma solvent (as a liquid) exposure of wafers. Ratios of LGS to IPA absorbance have been performed to highlight the difference between drying of native oxide and thermal oxide surfaces. The isopropyl alcohol peaks are used as the baseline in Figure 14.11. In the case of thermal oxide, the LGS solvent slightly reduces the Si-OH signal (~3500 $cm^{-1}$) that can be associated with fewer Si-OH groups on the surface before bonding. At the same time, a significant $CH_x$ signal is observed around 2900 $cm^{-1}$ suggesting residual organic contamination. For the native oxide, the Si-OH absorbance appears unaffected by LGS exposure while peaks near 3200 $cm^{-1}$ indicate little water adsorption on the wafer.

In Figure 14.12, FTIR-MIR characterization has been performed after LGS drying. At t = 0, the LGS liquid was dispensed *in situ* on the sample surface with an apparatus internal to the FTIR-MIR [81]. Le Tiec and coworkers showed that the native and thermal oxides are affected by liquid LGS differently. It is worth noting that the $CH_x$ absorbance (between 2850 and 2900 $cm^{-1}$) disappears after about

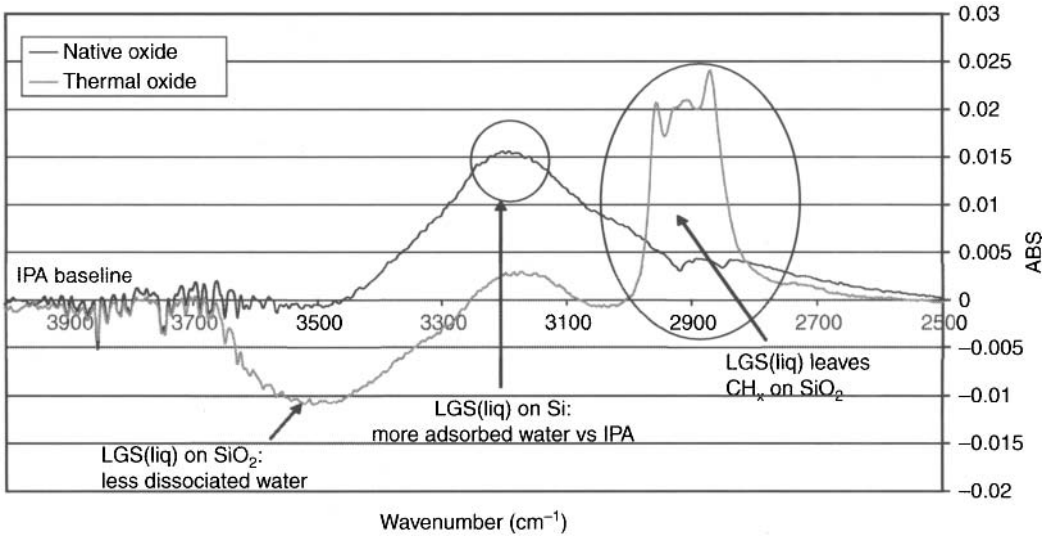


**Figure 14.11.** Fourier transform infrared-multiple internal reflection characterization after low gamma solvent exposure of native oxide and thermal oxide surfaces, as compared to IPA [81]. Reproduced with permission of ECS – The Electrochemical Society from Le Tiec, Y., Fournel, F., Rochat, N., Barnes, J.-P., Veillerot, M., Morales, C., Moriceau, H., Clavelier, L., Rieutord, F., Morote, C., Vandenbossche, M., Butterbaugh, J., and Radu, I., *The Electrochemical Society Transactions*.

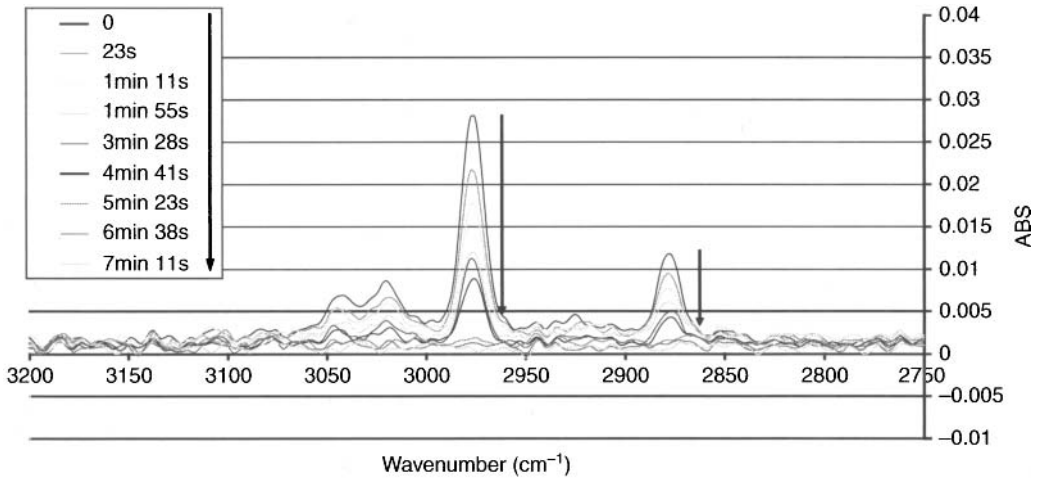


**Figure 14.12.** Fourier transform infrared-multiple internal reflection characterization after a low gamma solvent dry, the solvent is used in its liquid phase. The $CH_x$ chemical signature decreases gradually in air and disappears at ~5 min [81]. Reproduced with permission of ECS – The Electrochemical Society from Le Tiec, Y., Fournel, F., Rochat, N., Barnes, J.-P., Veillerot, M., Morales, C., Moriceau, H., Clavelier, L., Rieutord, F., Morote, C., Vandenbossche, M., Butterbaugh, J., and Radu, I., *The Electrochemical Society Transactions*.

5 min in air. The conclusion is that direct bonding should be performed a few minutes after drying to allow removal of residual $CH_x$ organic contamination from the surface.

## 14.4 Dry Surface Conditioning Processing

Dry surface cleaning and conditioning processes have been studied as alternatives to wet cleaning. Plasma activations and $UV/O_3$ process are shown to be very effective for organic contamination removal and for inducing modifications of the surface and near subsurface that result in high-quality bonding. Also, thermal treatments that allow high bonding energies and defect-free bonding after low temperature annealing have been widely studied. This section will discuss these surface conditioning techniques.

### 14.4.1 Process Flow

Dry surface conditioning can be considered as an additional treatment to help optimize surface preparation. In that sense, plasma-activation or $UV/O_3$ cleaning can be integrated into the wafer bonding process flow for several applications. A typical sequence would consist of:

1. Wet cleaning (typically RCA).
2. Plasma or $UV/O_3$ treatment for one or both wafers to be bonded.
3. Optional rinse in deionized water or a short or modified RCA cleaning.
4. Direct wafer bonding in air at room temperature.
5. Thermal annealing.

Next Page



## 14.4.2 Plasma Activation

### *14.4.2.1 Background of Plasma Processing*

Plasma-assisted wafer bonding employs a surface activation step in which one or both wafers to be bonded are submitted to plasma processes without intending to etch or deposit a film. In order to bond wafers containing temperature sensitive devices or to obtain heterostructures corresponding to the assembly of wafers made of two different materials (*e.g.* wafers whose the coefficients of thermal expansion are very different), a bonding process operating at moderate temperature (<500°C) is needed that yields high bond strengths. For instance, such a process flow has been used to generate silicon on glass (SOG) taking into account that silicon and glass exhibit very different coefficients of thermal expansion [85], strained SOI and SiGeOI structures [45], and accelerometers [86]. Wafers with special dopant profiles, metal patterns, or heterostructures requiring bonding of wafers with significantly different coefficients of thermal expansion are typical applications that have promoted the investigation of alternative bonding techniques based on surface plasma activations. Even if plasma activated wafer bonding is still in the development phase, it may become a standard technology providing it is compatible with complementary metal oxide semiconductor (CMOS) technology and may be integrated into semiconductor manufacturing process flows likely starting with MEMS fabrication.

Since the pioneering works of Sun *et al.* [87] and Kissinger and Kissinger [88], many studies have reported that strong hydrophilic bonding can be achieved at low temperatures (<500°C) [89–92] or even at room temperature [93] by exposing the wafers to plasma prior to bonding. Such treatments can last for a few seconds [93, 94], 20–60 seconds [90, 92, 95], or several minutes [89, 96]. It is worth noting that excessively long exposures can lead to surface degradation, in particular, roughening [92, 97].

Oxygen plasma is by far the most extensively described in the literature [90, 92, 98, 99]; however, other gases are also used such as Ar [92, 98], $N_2$ [92, 98], $H_2$ [100], $SF_6$ [101], and $NH_3$ [102] that have been shown to induce high bonding energies after limited thermal annealing, as illustrated in Figure 14.13. These wafers were activated by plasma for 30 seconds, subsequently cleaned in DIW for 5 minutes, bonded at room temperature, and finally annealed at various temperatures for 2 hours [92]. Surface energies were measured by inserting a blade between the two bonded wafers [103, 104]. The crack length, L, induced by the blade insertion is linked to the bonding energy which is proportional to $L^{-4}$. When bonded wafers are silicon wafers, the crack length can be measured by observation under infrared illumination [103, 104].

Wide varieties of plasma processes are suitable to perform surface activation before bonding. Studies report the use of barrel reactors and strippers, but most developments are done with radio frequency (RF) or microwave (MW) powered reactive ion etching (RIE) systems with either capacitively or inductively coupled plasmas [89–93, 95, 99–101, 105]. Traditional stand-alone vacuum plasma systems usually dedicated to etching or stripping can be converted for use as plasma surface activation systems without any hardware modification. Downstream plasma

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# PART 3
# NEW DIRECTIONS

# 15

# Novel Analytical Methods for Cleaning Evaluation

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*Abstract*

A review of recent trends in analytical characterization of wafer cleaning methodologies is covered in this chapter. For the wafer fab, there have been several improvements in the capabilities of total refection X-ray fluorescence spectroscopy. These would include difference X-ray sources for improved selectivity of analysis and more complete coverage of the entire wafer's surface. Methodologies also have been developed for monitoring trace metal contamination on the bevel and edge of the wafer. Non-visual defects and wafer charging mechanisms have been characterized with Kelvin probe type technologies. While some new methodologies are still highly specialized, lab based techniques that require a synchrotron X-ray source, others are *in situ* monitoring at the wafer processing level, such as electrochemical sensors.

*Keywords:* wafer contamination, contamination monitoring, analysis, TXRF, vapor phase analysis – VPD, vapor phase treatments – VPT, Kelvin probe

## 15.1 Introduction

The fundamentals of wafer contamination [1] and trace contamination analysis on wafers [2] are well covered in these and other references. The purpose of this chapter is to report on recent advances in analytical methodology associated with cleaning and surface conditioning processing. It is useful to consider the various methods of contamination monitoring in terms of different applications:

1. Device and wafer fabrication for high volume manufacturing and research.
2. Pilot line development activities.

Device and wafer manufacturers require detailed analysis when monitoring contamination and surface condition. However, monitoring typically is done only

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for a selected set of wafers in volume manufacturing. This information is provided to the fabrication facility engineers and includes surface roughness, particle counts, surface and bulk metallic contamination [3]. These metrics are used to track the cleanliness of tool, the process stability, and other important items required for manufacturing high yielding devices and high-quality wafers.

The research and pilot line facilities often evaluate a variety of new materials and processes, some of which are selected for volume manufacturing. Research and pilot line facilities, where tools can be shared using different types of materials and processes, must prevent these materials from contaminating the entire process line. For example, hafnium oxide and metal gate (*i.e.* titanium, tungsten, and tantalum-based metals) are now used in volume manufacturing; however, next generation transistors require the introduction of new elements to the gate stack [4]. Elements such as lanthanum or aluminum are candidate materials, while other elements are under consideration. A variety of low dielectric constant (low-κ) and barrier metal materials are also under consideration [5]. These must be monitored to determine if any detrimental effects are contributed due to their introduction.

The Front End Processes Roadmap in the International Technology Roadmap for Semiconductors (ITRS) provides important information about the measurement requirements for contamination. The Surface Preparation Technology Requirements Table [6] lists the maximum allowable amount of metallic contamination for elements that are known to cause problems to the integrity of silicon dioxide and oxynitride gate dielectric layers; the gate oxide integrity (GOI). The Si wafers should have less than $5 \times 10^9$ atoms/cm$^2$ of these critical GOI metals such as Ca, Ba, and Sr. Other metals are known to dissolve in Si and form silicides including Ni, Cu, Cr, Co, Hf, and Pt. Of these, less than $1 \times 10^{10}$ atoms/cm$^2$ should be present on wafer surfaces. Finally, less than $2 \times 10^{10}$ atoms/cm$^2$ of mobile ions such as Na and K should be present on wafer surfaces. The ITRS targets for mobile ions are based on allowable shift in threshold voltage for a transistor. As stated in the ITRS, some metals may remain in the active Si layer while others diffuse through the buried oxide layer interface out of the device layer.

The introduction of high-κ gate dielectrics and silicon on insulator (SOI) wafers may change these targets; however, the necessary data is not available at this time. The ITRS roadmap takes a conservative approach by specifying contamination levels based on experience with bulk silicon wafers and traditional gate dielectrics.

## 15.2 Novel Analytical Methods

Because of the processing challenges of new materials introduced, as discussed in Chapter 16, it is necessary to measure new types of contamination and at a lower concentration level on Si surfaces. The continuous introduction of new materials, especially, high-κ and low-κ dielectrics, metals for gate conductors, along with new patterning processes challenge analytical methods, such as total reflection X-ray fluorescence spectroscopy (TXRF), to increase their capabilities – detection sensitivity and ease of analysis. New methods are being introduced for monitoring surface contamination with the ultimate goal of measurements on patterned wafer surfaces that correlate to product yield.

## 15.3 Recent Advances in Total Reflection X-ray Fluorescence Spectroscopy Analysis

For many years the TXRF instrument used to monitor contamination in the fab has not fundamentally changed. There have been incremental improvements in detection limits with advances in optics, sources, and detectors, but the basic procedure has included the measurement of transition metals at a few locations on silicon wafers. See [2] for an overview of TXRF basics. Monitoring *via* TXRF is often done by running a test wafer upside down through a chamber, such as etching or deposition, and then measuring the contamination transferred to the wafer surface during processing [7]. With the switch to high-κ gate dielectrics and metal gate electrodes, the film must have the added contamination monitored and as well as the contamination from these new layers. Fairly recent innovations in TXRF capabilities have allowed the technique to remain relevant in modern semiconductor fabs. For a comprehensive review please refer to reference [8]. Described below are some of the significant advances.

### 15.3.1 Alternative X-ray Sources for TXRF

Early candidates for high-κ gate dielectrics included Hf and Zr based materials, Chapter 7 presents an in depth discussion of the metal gates and high-κ dielectric gate electrode. As research and development laboratories went through the initial learning process for successful manufacturing using these materials, there was a need to control cross contamination. Monitoring for Zr at $10^{10}$ atoms/cm$^2$ levels with a standard W-Lβ TXRF source was not possible because there is significant background noise from the Si-Kα peak at the Zr-Lα energy region causing poor detection limits. The other option was to have a high energy X-ray source that was greater than Zr's K absorption edge of 18.000 keV. Commercial TXRF instruments have taken two main routes to achieve this; one is to select a portion of the Bremsstrahlung radiation (for example, 24 keV) for an excitation source, and the other is to use characteristic radiation from a tube anode. The Ag tube anode with a Kα line of 22.1 keV has become a popular choice for a characteristic radiation source [9]. Monitoring for Hf contamination on bare silicon wafers is more straightforward. A different source is not needed to observe the Hf-Lα line, but there can be overlaps between the Hf-Lα line (7.899 keV) and Cu-Kα contamination (8.042 keV) if either is present in significant amounts.

As large manufacturers in the semiconductor industry have settled on Hf-based gate dielectrics as a replacement for $SiO_2$-based gate dielectrics, the challenge is measuring trace contamination on the surface of the Hf films with the background in the 6–8 keV region introduced from the multiple Hf lines. Hellin, *et al.* proposed a TXRF method using the W-Lα radiation [10] which at 8.398 keV is below the Hf absorption edge of 9.56 keV resulting in a low background for most of the transition elements. Unfortunately, the W-Lα incident radiation is below the absorption edge for Cu (8.979 keV), limiting the usefulness of monitoring for this important element. Commercial instruments have now been introduced that utilize either an Ir or Pt anode with fluorescence lines at 9.175 keV and 9.443 keV respectively [11, 12]. These

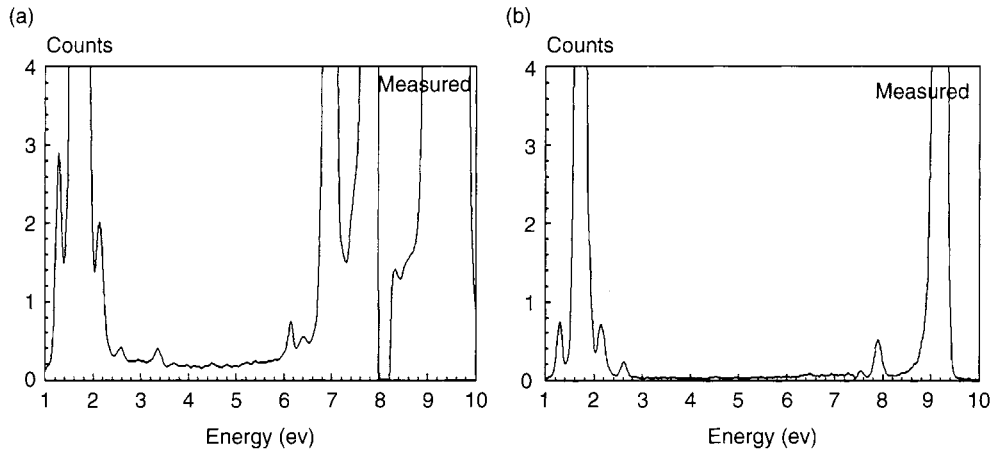


**Figure 15.1.** Total reflection X-ray fluorescence spectra of a 2-nm HfSiO film measured with (a) a W anode and (b) an Ir anode, showing that the Ir anode spectrum has less background noise. Used with permission from the authors.

sources minimize the background from the Hf substrate while allowing for trace level measurements of the transition metals. For example, Figure 15.1 compares the background spectra of a 2-nm HfSiO film collected by both a TXRF equipped with a) a standard W-Lβ source and b) an Ir-Lα source. There is a small peak at the Hf-Lα in the Ir collected spectra as well background from Raman scatter and the Ir escape peak [12], but otherwise the spectra is much cleaner for quantifying low levels of trace metal contamination. Recently work has been published describing methods for measuring trace metal contamination on a high-κ gate dielectric surface for evaluating wet etching of CMOS duel metal gates [11].

Monitoring contamination from light (low Z – atomic number) elements like Na, Mg, and Al are difficult with TXRF with a standard W-Lβ source. Reasons for this include low fluorescent yield of the elements due to a preferred relaxation mechanism that emits an Auger electron instead of a photon, re-absorption of the low energy photons, and a higher background from the Si matrix. Research into the measurement of low Z elements by Streli *et al.* [13–15] thoroughly investigated different sources for more efficient coupling of the photoelectric mass absorption coefficient and has led to improvements in detection limits. For example, using a windowless Si X-ray source Streli was able to achieve detection limits of $9 \times 10^{11}$ atoms/cm$^2$ for Na using only TXRF analysis extrapolating to a VPD-TXRF (vapor phase decomposition-TXRF) detection limit of $3 \times 10^9$ atoms/cm$^2$ on a 200-mm wafer [15]. Commercial TXRF systems have now implemented sources for more efficient excitation of the low Z elements. These systems have multiple X-ray sources that can converge at the same location on a wafer for more complete characterization. The system designed by Rigaku uses a monochromator to select the W-Mα line (1.776 keV) from the rotating W anode [16] while the system Technos International builds uses a multi-tube system (see Figure 15.2) that incorporates a Cr tube (Kα of 5.412 keV). Both manufacturers indicate they can reach detection limits in the low $10^{11}$ atoms/cm$^2$ range for Al with these sources.

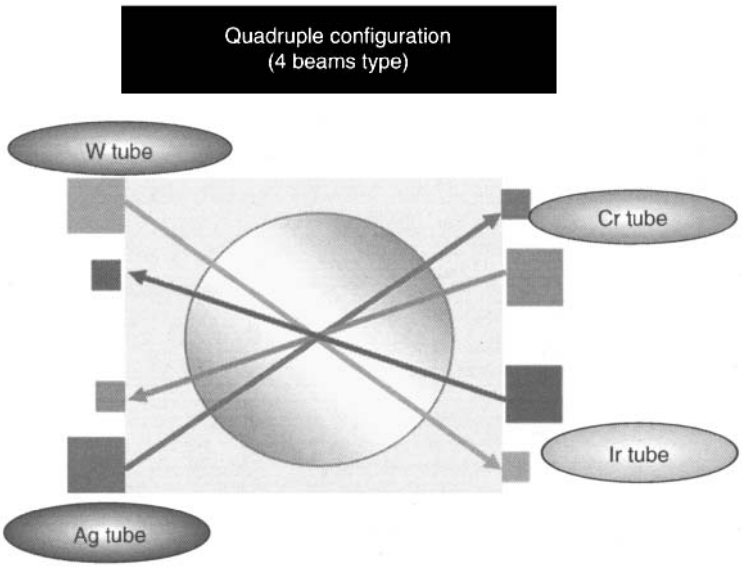


**Figure 15.2.** Example of a 4 beam TXRF system available from Technos International [17]. Used with permission from Technos International.

### 15.3.2 Surface Coverage of the Wafer

One of the advantages of TXRF is its ability to map contamination across the wafer. A standard recipe for a 300-mm wafer may be five points scattered across the surface which takes approximately one hour for the data acquisition. Assuming a quantitative spot size of 1 cm in that hour's time data is collected from about 0.6% of the surface area. To increase surface coverage, the data acquisition time will increase, and thus the throughput will decrease. In contrast, one of the reasons for the widespread use of VPD-based analysis is that contamination from the entire wafer surface is collected and analyzed. This along with the pre-concentration effect discussed by Hues and Lovejoy [2] are the primary advantages of VPD. Some disadvantages to using VPD are the loss of spatial resolution of the contamination, the dilution effect of averaging the contamination such that localized contamination may be lost, and the dependence of the efficiency of the metal collection on the scanning chemistry. To achieve complete surface analysis by TXRF in a reasonable amount of time, Mori recently developed sweeping TXRF [18, 19]. He showed by analyzing hundreds of points across a wafer for a very short integration time (10 sec or less) data could be collected from the entire wafer in approximately the same amount of time as a standard analysis. The accuracy error obtained by not rigidly controlling the incident angle was shown to be negligible if all the spectra are accumulated and summarized into a single spectrum. Additionally, a wafer map showing hot spots of localized contamination can be obtained whereas the detection limits only are about one order of magnitude worse than standard TXRF. The accumulated spectra can achieve good signal to noise averaging achieving approximately $10^9$ atoms/cm$^2$ detection limits for uniform contamination. Figure 15.3 shows an example of the sweeping TXRF – a localized hot spot of Fe

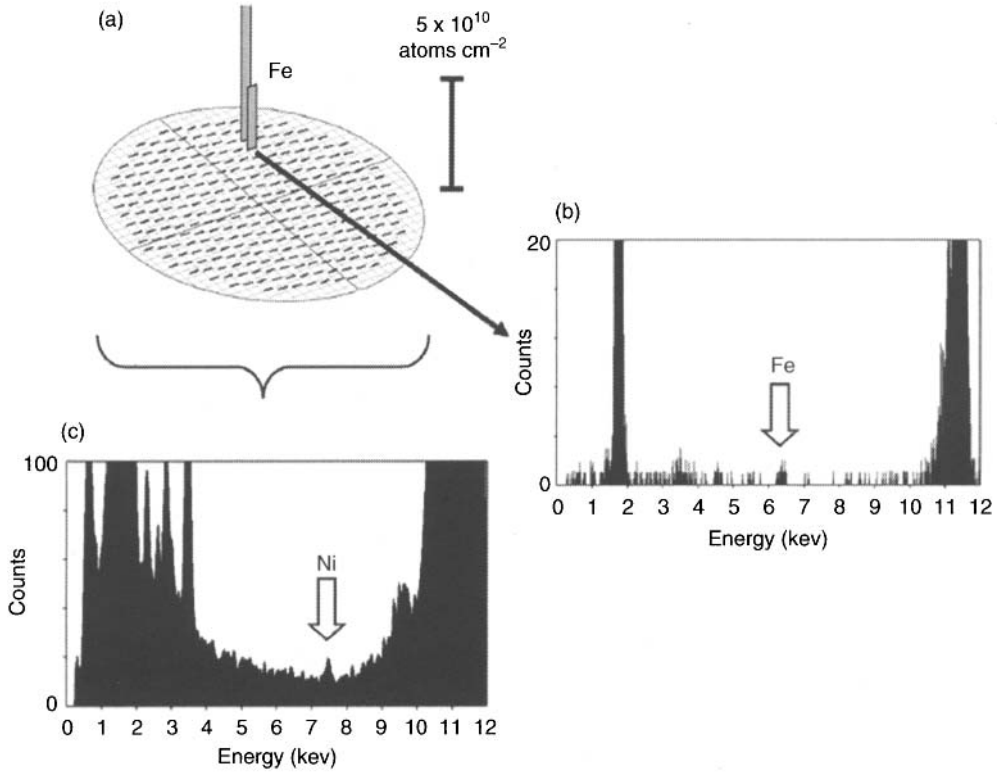


**Figure 15.3.** Result of the test of sweeping-TXRF for a 300-mm wafer, with uniform Ni and localized Fe contamination; (a) Fe is detected at a spot, (b) Fe-Kα peak can be seen at the spot, and (c) the accumulated spectra showed the presence of relatively uniform Ni at ca. $3 \times 10^9$ atoms $cm^{-2}$ [18]. Reprinted from *Spectrochimica Acta Part B*, Volume 59, Mori, Y., Uemura, K., Kohno, H., Yamagami, M., Yamada, T., Shimizu, K., Onizuka, Y., and Iizuka, Y., "Detection of unknown localized contamination on silicon wafer surface by sweeping total reflection X-ray fluorescence analysis", page 1277. Copyright (2004) with permission from Elsevier.

is detected in one area of the wafer while the accumulated spectra shows uniform contamination from Ni.

The major suppliers of TXRF tools designed for device fabrication analysis were quick to incorporate this method of mapping the surface of the wafer as an option on their instruments, and it was embraced by the analytical community. Investigations into contamination control [20], precision and accuracy [11], optimization [21, 22], and a holistic comparison of TXRF based analytical methods [23] soon followed. Figure 15.4 is an example of a 200-mm wafer that had been processed through a wet cleaning step that highlights the value of mapping TXRF. The data was collected from 109 points across the wafer surface; shown is a two dimensional map of the Cu contamination where the dark locations indicate Cu hot spots of about $2.5 \times 10^{10}$ atoms/$cm^2$. The x's represent where a standard TXRF measurement would have taken place and no Cu was detected at those locations. An analysis of this wafer by VPD-ICP-MS (VPD-inductively coupled plasma mass spectrometry) measured $1.3 \times 10^{10}$ atoms/$cm^2$ of copper

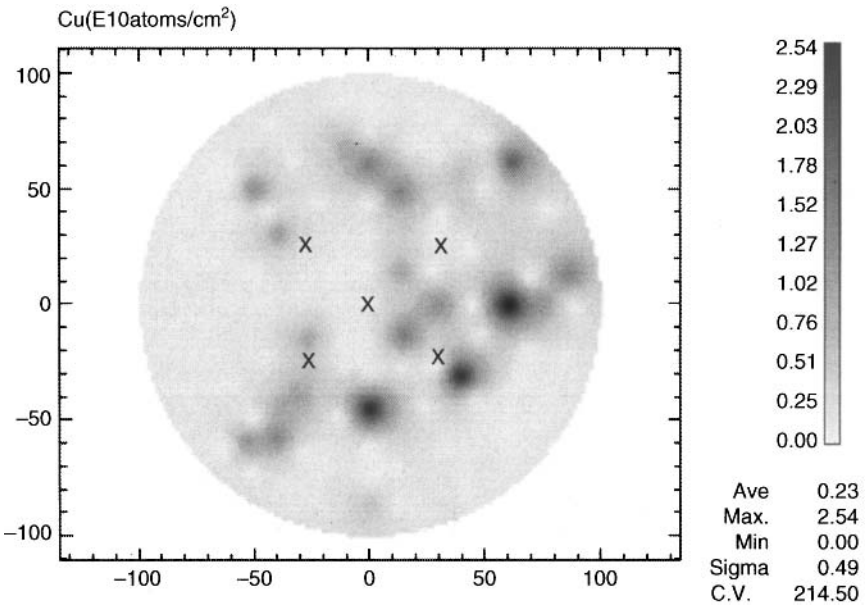


**Figure 15.4.** Two dimensional map of copper contamination, the X's represent coordinates for a standard 5-point map where no copper was measured [11]. Used with permission from the author.

contamination. This example shows the value of increasing the TXRF data density on a wet clean monitor even though the typical contamination from a wet cleaning tool is uniform coverage.

### 15.3.3 Edge Contamination Monitoring of the Wafer

Most TXRF systems have a built-in edge exclusion of ~10 mm to ensure that the incident radiation striking the edge and bevel of the wafer does not scatter into the detector. The edge region significantly contributes to contamination due to transfer of abraded material from edge grip handlers and cassette rails, for example. A recent innovation allowed for rotating the wafer 180° in the analysis chamber so the incident radiation approaches the edge of the wafer from the center [24], having a much lower background than the conventional geometry. As the incident X-ray beam travels nearly parallel to the surface of the wafer, if measurements near the edge of the wafer are attempted by conventional analysis, there will be scatter of the incident beam from the edge and the bevel region of the wafer into the detector. Figure 15.5 shows a schematic of the approach for a conventional incident beam and the approach of a beam that allows for measurement with no edge exclusion. Figure 15.6 shows the intensity dependence on the radius measured for Si and for Fe background counts. There is a drop in Si intensity past the 90-mm radius because the detector has a 10-mm diameter acceptance spot size, so a portion of the detector is over the edge of the wafer and not collecting signal from the wafer.

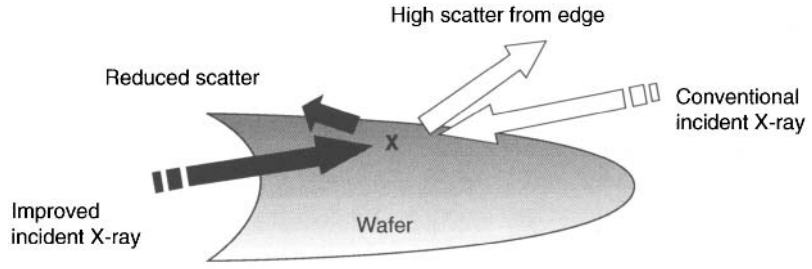


**Figure 15.5.** Example of edge contamination detection by TXRF [24]. Used with permission from H. Takahara.

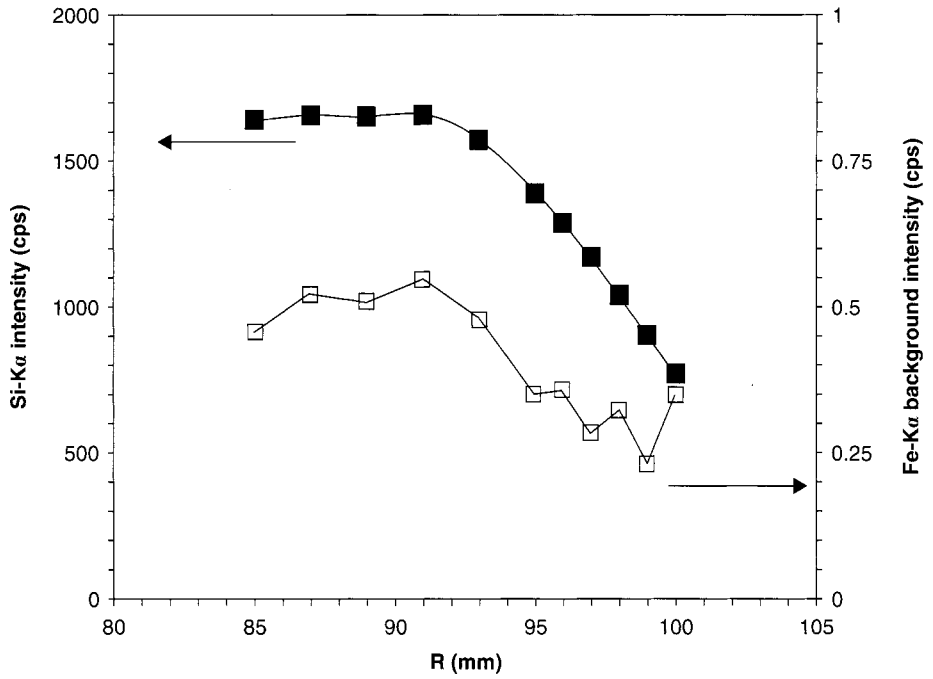


**Figure 15.6.** Intensity dependence on radius, *R*, in measurement coordinates for Si-Kα and Fe-Kα backgrounds for a 200-mm silicon wafer [24]. Used with permission from H. Takahara.

### 15.3.4 Front and Back Surface Monitoring of the Wafer

Measurement of contamination on the backside of a wafer due to the handling components of the tool typically has been accomplished on single-side polished 200-mm wafers by reversing the wafer in the wafer carrier, cycling the wafer upside down through the tool, and then reversing the wafer in the carrier to the polished side face-up for analysis. For 200 and 300-mm DSP (double sided polished) wafers, the contamination monitor wafer can be cycled through the tool and then flipped for standard TXRF analysis. In the interest of conserving monitor wafers, a TXRF tool has recently been developed that allows monitoring of contamination on both the front and back surface of the same wafer provided the wafer is DSP [25]. There

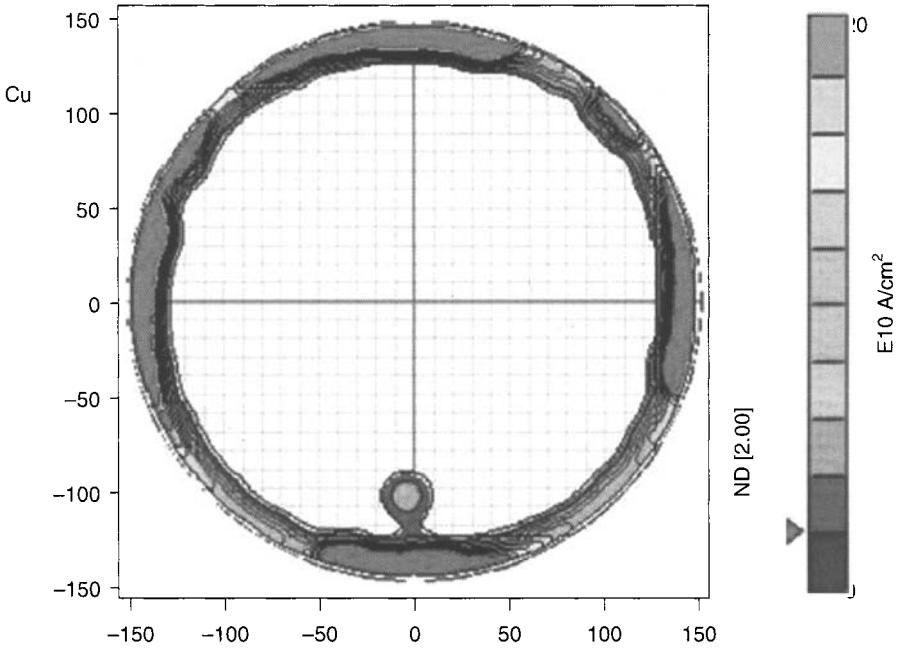


**Figure 15.7.** Copper contamination detected on the back surface of a 300-mm wafer, near the edge [24]. Reprinted with permission from Kohno, H., Yamagami, M., Formica, J., and Shen, L., *Abstracts of Frontiers of Characterization and Metrology for Nanoelectronics*. Copyright 2009, American Institute of Physics.

is a possibility for observing some cross contamination from the TXRF's handling robots and stage, but this tool was primarily developed to monitor contamination on the backside near the edge of the wafer. Figure 15.7 shows a Cu contamination map of the backside of a 300-mm wafer after a sputtering process where the contamination is concentrated close to the edge of the wafer.

### 15.3.5 Contamination Analysis on New Materials

The primary application of TXRF analysis is trace metal monitoring on silicon surfaces. With the rise of new materials, TXRF is also being used to characterize them as well. Earlier in Section 15.3.1, measuring Hf-based films for high-κ gate dielectrics was discussed. Other surfaces such as Ge [26–28], $Al_2O_3$ [29–31], Ru [30, 31], and CoWP [28] have also been characterized by TXRF.

## 15.4 Advances in Vapor Phase Analysis

There have been several reviews of the VPD TXRF technique [8, 32, 33] in recent years. The instrumentation has become automated to the point of "push-button analysis." Recent studies have investigated saturation effects that limit the linearity of the VPD TXRF signal and remediation of these effects [34–36]. Novel ways of depositing nanoliter and picoliter droplets and drying the VPD-residues have recently been studied [31, 37–41]. Some of the benefits found with the nanoliter and

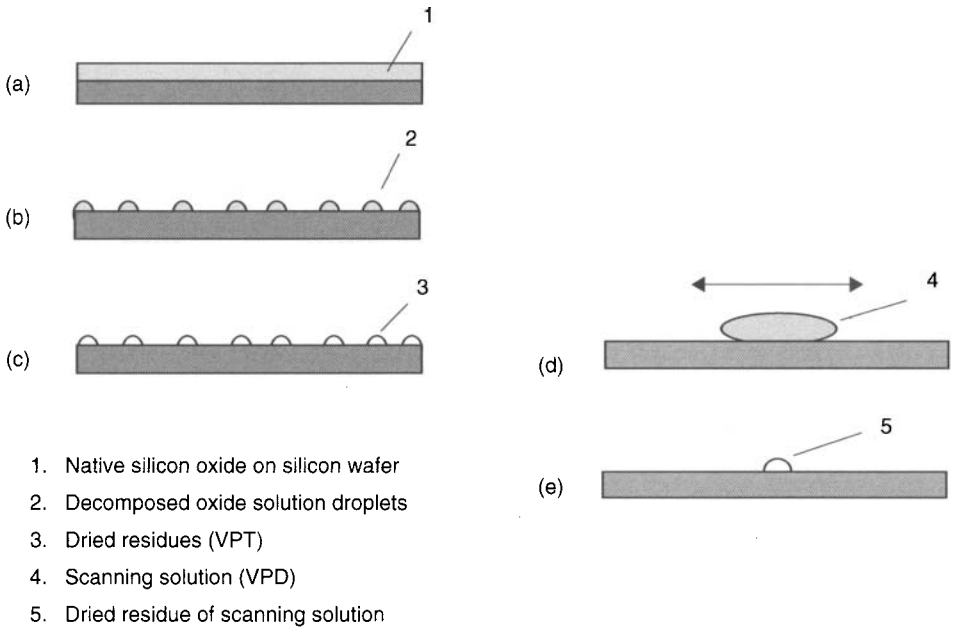


**Figure 15.8.** Flow schematic diagram of VPT-TXRF method compared with conventional VPD-TXRF method [44]:

- VPT-TXRF: (a) → (b) HF vapor decomposition of native silicon oxide → (c) natural drying of decomposed solution droplets → TXRF.
- VPD-TXRF: (a) → (b) HF vapor decomposition of native silicon oxide → (d) collection of decomposed solution droplets → (e) drying of collected scanning solution →TXRF.

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picoliter deposition are improved linearity of the TXRF signal and less signal suppression from additional matrices. An alternative method for decomposing thick (for example, 500-nm) $SiO_2$ films for VPD analysis use purging of the VPD chamber with nitrogen gas [42]. This reduces the water accumulation on the wafer surface from the byproduct of the reaction of HF with $SiO_2$ to an amount that is manageable for automated scanning. An interesting benefit of this process is that the Si concentration, measured by ICP-MS, of the sample from the oxide wafer is only a factor of two greater than the Si concentration from a wafer with a native oxide. This has potential benefits in the ability to quantitatively measure samples by ICP-MS and TXRF that would normally have matrix induced suppression [43]. This suppression is a reduction of the true analyte signal due to energy that would ideally go into creating the signal being absorbed by the matrix (for example, Si or $SiO_2$).

An interesting new sub-set of the VPD process called vapor phase treatment (VPT) TXRF has been recently introduced [44]. In this case, the wafer is exposed to HF vapor similar to the VPD process, but the collection solution from the wafer is not scanned. The condensate is allowed to dry in place allowing the spatial information of the contamination to remain (schematic in Figure 15.8). The premise is that low levels of contamination present on the wafer in plated contamination are converted to residue contamination (see Figure 15.9). This reportedly enhances

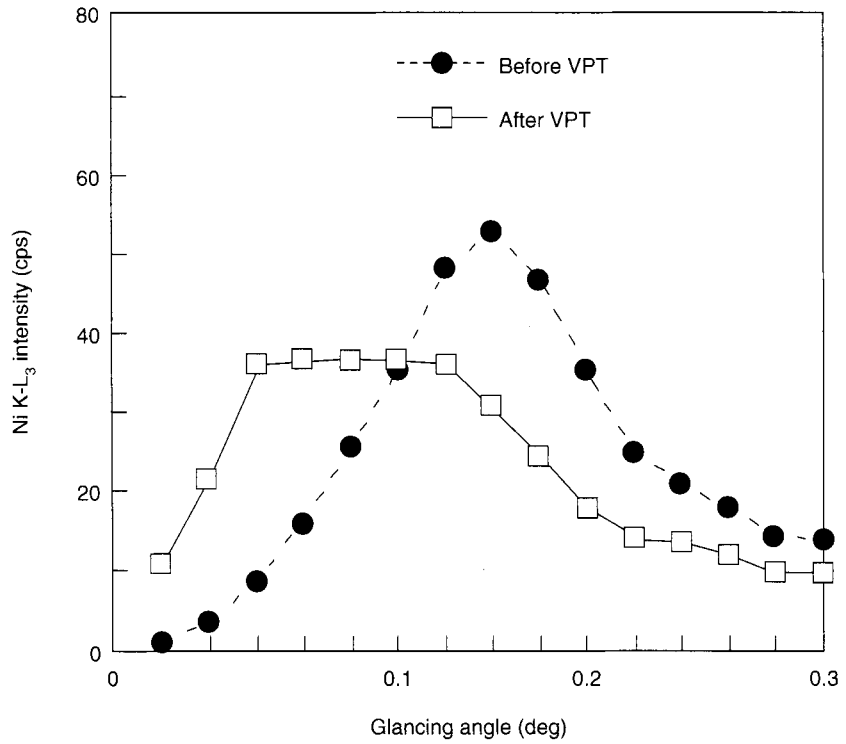


**Figure 15.9.** Angular dependence of fluorescent X-rays before and after VPT for $2 \times 10^{13}$ atoms/cm$^2$–Ni-contaminated standard wafer [44]. Reprinted with permission from the *Japanese Journal of Applied Physics*, Shimazaki, A., Miyazaki, K., Matsumura, T., and Ito, S., Volume 45(12), Page 9037 (2006).

the signal from the contamination at low incident angles of radiation by factors of 4–7 times, depending on the element, enabling quantification down in the low $10^9$ atoms/cm$^2$ range [44]. The VPT procedure combined with the mapping capabilities of TXRF has the potential to be a powerful technique for monitoring low level metallic contamination with spatial information. The Japanese ISO (international standards organization) working group ISO/TC201/WG2 implemented a round robin study of the VPT TXRF technique which resulted in a wide and inconclusive range of VPT signal enhancement factors; hence, work is being continued on this question [45].

## 15.5 Trace Metal Contamination on the Edge and Bevel of a Wafer

In section 15.3.2 the importance of measuring contamination on the whole wafer is discussed with respect to recent modifications to the TXRF system's ability to measure wafers with no edge exclusion. However, cross contamination of metallic contamination from the edge and bevel of the wafer can also occur and must be considered [46, 47]. Due to scattering of the incident radiation, TXRF cannot be used to measure the bevel or the edge of a wafer. One analytical technique that can be used to measure

on the bevel is time-of-flight secondary ion mass spectroscopy (TOF-SIMS); however, the angle on the bevel makes consistent analysis difficult, and the small analytical spot size would require many analyses for a representative sample set.

There have been methods of chemical extraction of the metallic contamination from the edge of the wafer that have been developed [24, 46, 48] where the extraction solution is subsequently analyzed by ICP-MS or TXRF. The extraction solution is usually similar to a VPD scanning solution being made up of HF, $H_2O_2$, and $H_2O$. In this case though, the concentration of HF is higher because the wafer may not have gone through a VPD-type step and there would be an oxide (native, chemical, or thermal) on the Si wafer. The higher concentration of HF allows for the surface to be converted from hydrophilic to hydrophobic as the wafer slowly rotates through the extraction solution. This prevents streaking or running of the extraction solution and allows for control over the area of the bevel and edge that is analyzed.

Figures 15.10a and 15.10b show a wafer vertically supported with the extraction solution in the sample boat [46]. The sample collection and wafer loading are manual procedures in this case. Another manual version of this type of analysis has the wafer horizontally supported, rotating through a sample cup, where the extraction solution is held in place by surface tension as shown in Figures 15.11a and 15.11b [48]. A fully automated version of the bevel and edge analysis has been incorporated into an automated VPD system where the standard VPD scanning nozzle has been be replaced with a nozzle designed to scan the bevel and edge of the wafer as shown in Figure 15.12 [24]. In this case the scanning droplet can be programmed to be dried on a wafer support for TXRF measurement or deposited into a vial for measurement by ICP-MS.

## 15.6 Kelvin Probe Technologies

There has been an influx of recent publications on non-contact measurements where the surface of a wafer is scanned by a metal probe and variations in the difference between the work function of the probe and the wafer surface are measured [49]. This can be used as an in-line monitoring step to capture defects that are not detected by current optical defect inspection equipment. A data map of the wafer is shown in Figure 15.13 from a Qcept Technologies instrument. Analysis of these variations in contamination levels allows process monitoring. Figure 15.13 shows processed-induced charging that is caused from single wafer cleaning [50]. Statistical process control can be applied to the data; when the measured charge surpasses the upper control limit the wafer is flagged.

Characterizing wafer charging associated with cleaning process and the efforts to mitigate the charging have been reported in [51, 52]. Kelvin probe based measurements have also been applied to other non-visual defects including trace metallic contamination, ionic contamination, and organic contamination on the front side, backside, and edges of wafers on both patterned and un-patterned wafers [53–57]. Identification of the various types of contamination and the concentration are under investigation, but this technique has been shown to allow rapid screening that can supply coordinate information for more efficient supplemental analysis by other techniques (*i.e.* TXRF, Auger, XPS, or SIMS).

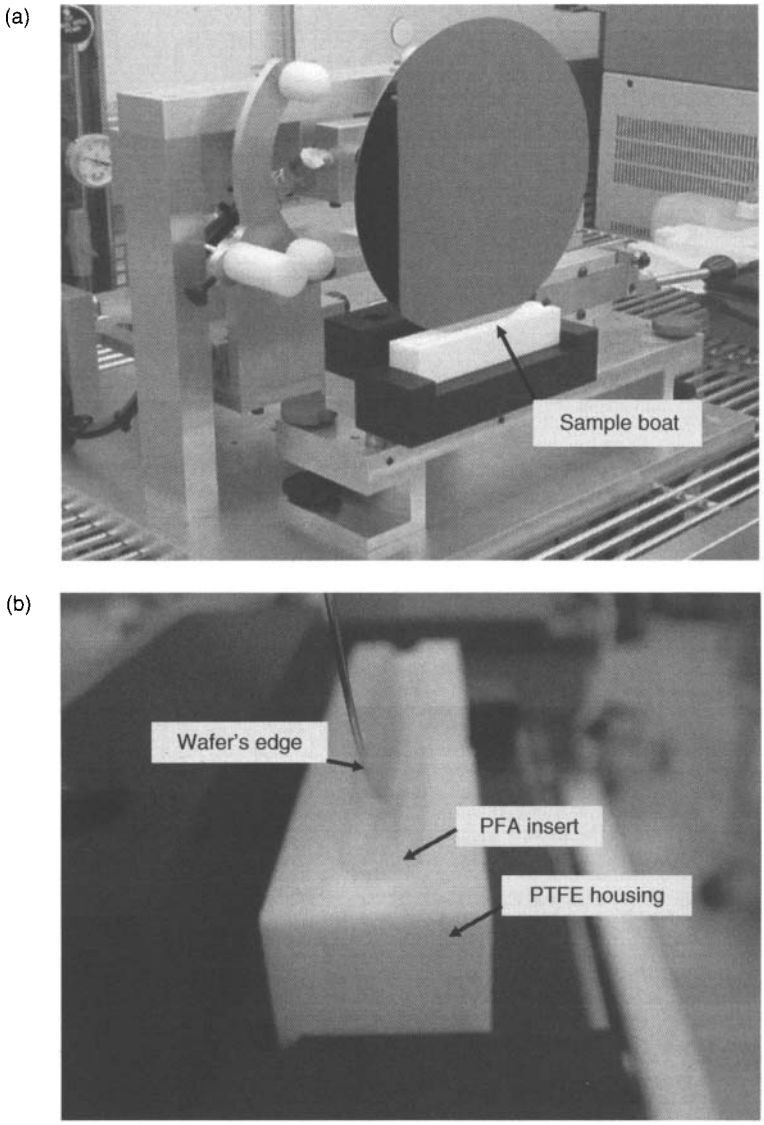


**Figure 15.10.** (a) Wafer vertically supported for analysis of the bevel and edge, and (b) side view of the wafer edge making contact with the extraction solution in the Teflon® perfluoroalkoxy (PFA) insert of the sample boat [46]. Used with permission from SPIE; Sparks, C., Gondran, C., Lysaght, P., and Donahue, J., "Novel Technique for Contamination Analysis Around the Bevel and Edge Exclusion Areas of 200 and 300 mm Silicon Wafers," *Process and Materials Characterization and Diagnostics in IC Manufacturing*, Volume 5041 (2003).

Other applications of Kelvin probe type technologies from KLA-Tencor Quantox™ have been used to extract electrical measurements; for example, current voltage and conductive voltage data, to evaluate pre-gate cleans [58]. The Quantox™ methodology can also be used to monitor surface charge, carrier, and generational lifetimes [59–62].

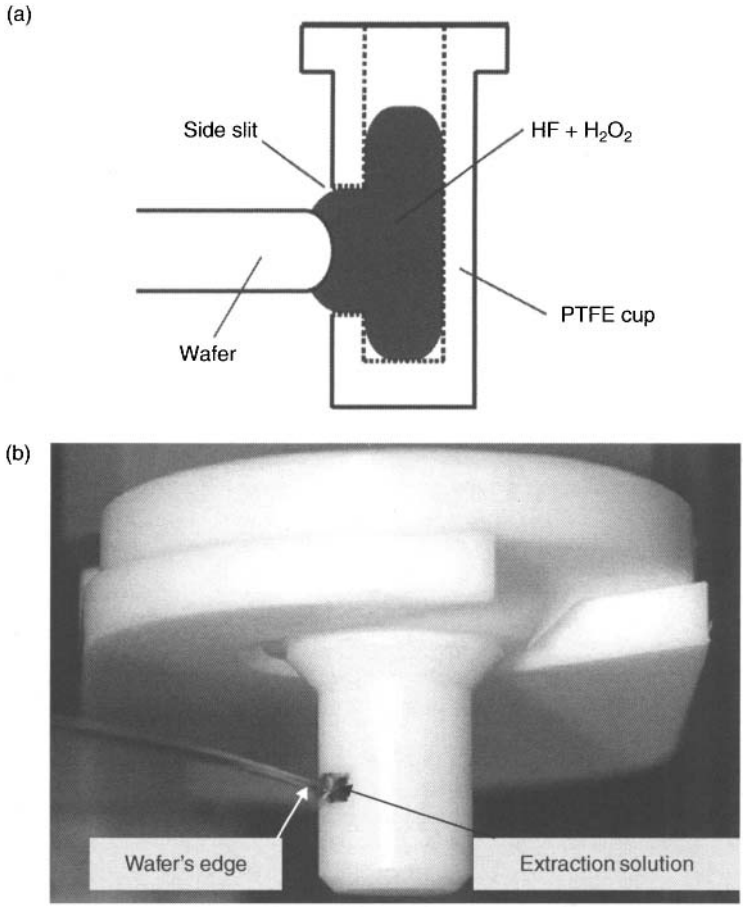


**Figure 15.11.** (a) Schematic of wafer horizontally supported and rotated through extraction solution and (b) image of sample collection in progress [48]. Reprinted with permission from the *Proceedings of the 65th Autumn Meeting of the Japanese Society Applied Physics*, Sakurai, Y., Mori, Y., and Uemura, K., Page 3p-B-17 (2004).

## 15.7 Novel Applications of Electron Spectroscopy Techniques

The basic principles of X-ray photoelectron spectroscopy (XPS) are covered in [2]. Angle-resolved XPS (ARXPS) is a method where surface and depth information can be obtained by collecting the spectra while varying the angle between the X-ray source and the sample, a simplified schematic is shown in Figure 15.14 and theoretical details can be found in reference [63].

Many other studies have been performed. Characterization of sidewall post-etch residue cleaning has been demonstrated with ARXPS [64, 65]. In these studies, the authors demonstrated they could quantitatively resolve the composition of the field, trenches, and sidewalls. The data suggested that there was incomplete removal of post-etched residue from the sidewalls, even after cleaned, due to the level of F detected [65]. Roughening of the surface of Si after HF etching

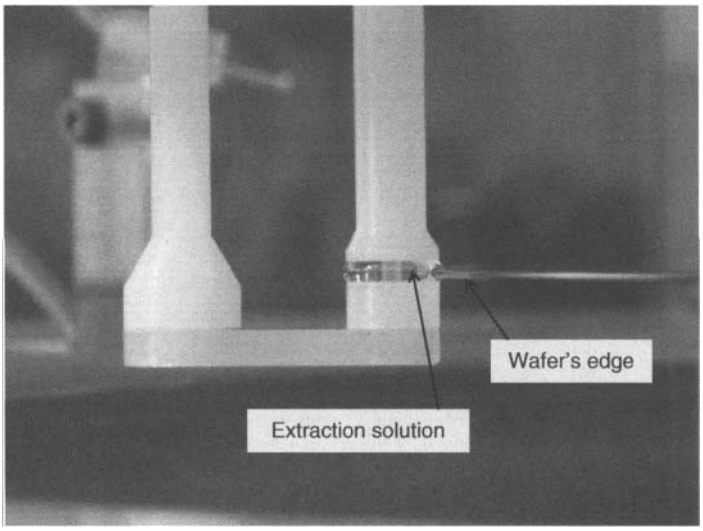


**Figure 15.12.** Automated bevel and edge analysis chemical extraction design from Technos International [24]. Used with permission from H. Takahara.

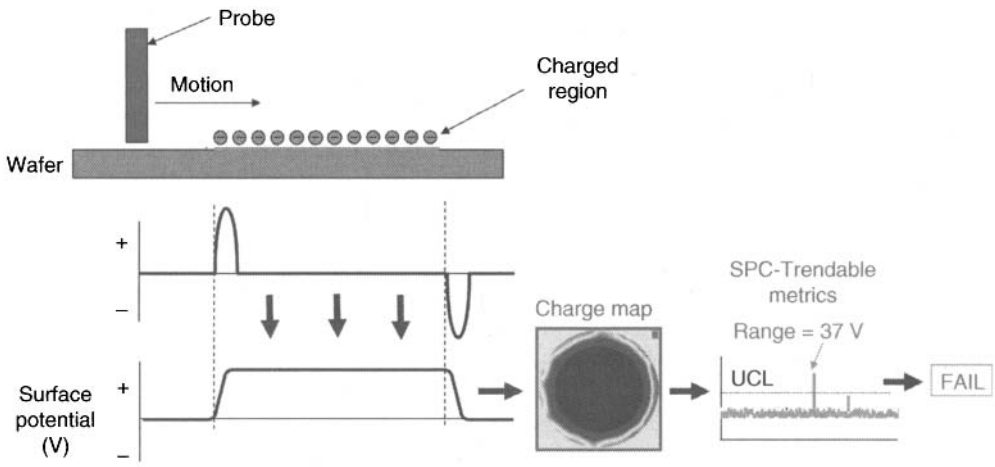


**Figure 15.13.** Schematic of surface potential difference imaging from Qcept [50]. Used with permission from Qcept Technologies.

was characterized with infrared (IR) spectroscopy and ARXPS, from this study they found a new bonding configuration (a reduced form) of Si [66]. The quality of chemical oxides formed on SiGe after wet cleans was investigated with ARXPS. A comparison of $H_2O_2$ cleaning processes showed less C contamination and improved oxide quality [67]. A post-CMP clean study of chemical oxides using a HF + $H_2O/O_3$-based clean on SiGe (20%, 50%, and 100% Ge) was performed with ARXPS [68]. Surface oxidation (and removal of the oxide) of W films deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD) was studied by ARXPS, for both as-deposited films and post-cleaning samples [69]. Angle

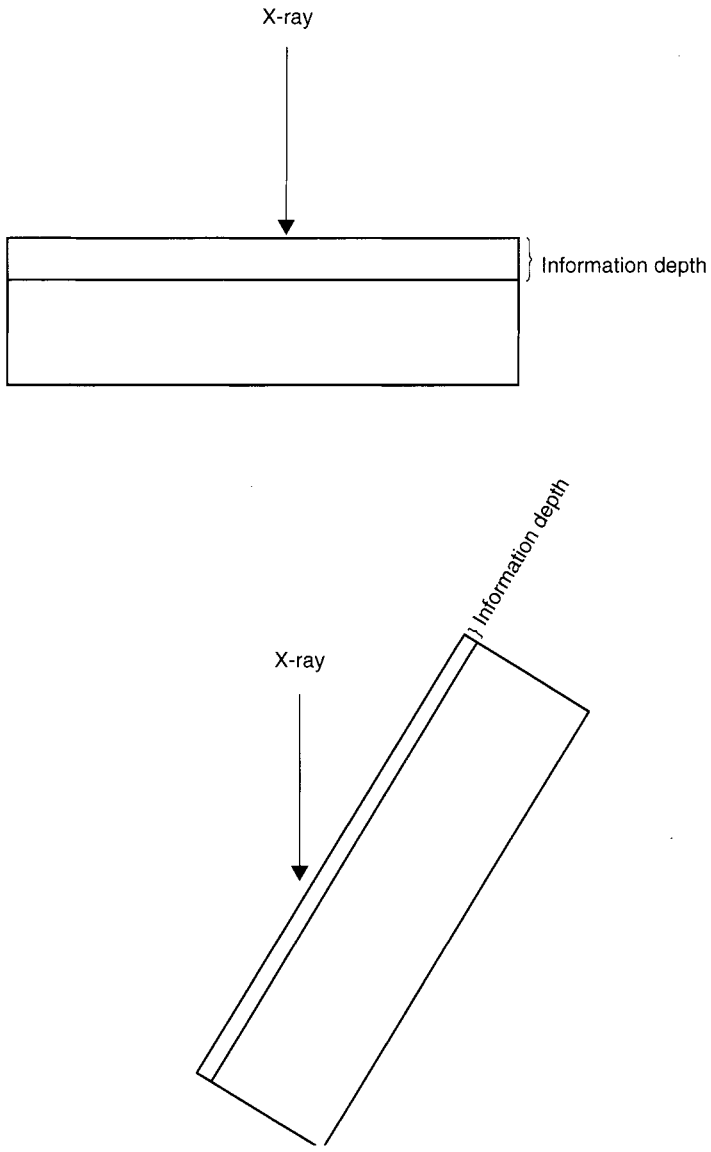


**Figure 15.14.** Schematic diagram of angle resolved-XPS where varying the X-ray's angle of incidence affects the information depth of the signal. Courtesy of Chris Sparks.

resolved XPS was also used to study the affect of different wet cleaning and storage conditions on the oxidation state of Cu films [70]. The surfaces of ultra low-κ films post-CMP cleaning processes were characterized with ARXPS, it was found that using an oxalic acid plus derivatives cleaning solutions changed the structure of the surface and damaged the films while using a citric acid plus derivatives clean cleaning solution did not [71]. The affect of the surface condition on the growth of high-κ dielectrics have also been characterized with ARXPS [72] and the results from ARXPS were compared to TOF-SIMS and RBS data and used to evaluate the authors' model for surface coverage.

## 15.8 Novel X-ray Spectroscopy Techniques

Some groups have utilized the capabilities of synchrotron facilities to further characterize the surface of semiconductor surfaces. For example, the group at the Physikalisch-Technische Bundesanstalt (PTB) has fully characterized their instrumentation to allow reference-free calibration with TXRF [73, 74]. Near edge X-ray absorption fine structure (NEXAFS) was used to analyze organic compounds on Si [75, 76] and to characterize self-assembled monolayers (SAM) on Ge [77]. X-ray reflectivity [78] has been adapted by the semiconductor metrology community for monitoring of film layers and interfaces. Using a high energy synchrotron source (HEXRR) has been used to characterize drying procedures in bonding SOI wafers [79, 80].

## 15.9 Electrochemical Sensors

To evaluate the rinsing step on patterned wafers, an electrochemical residue sensor (ECRS) has been developed for *in situ* monitoring of the ionic species [81]. These sensors show an improvement over the conventional method of bulk water conductivity for optimal determination of the rinsing endpoint. They are being used to test more efficient rinse recipes involving such parameters as wafer spin rate and water temperatures [82, 83].

## 15.10 Summary

Clearly progress in properly analyzing and characterizing semiconductor cleans processes has been made recently. A more complete picture of contamination on monitor wafers from the edges and bevels to covering the entire surface is now possible giving the process engineer valuable data with which to better understand their processes and troubleshoot excursions. Measurements that are *in situ* or on product wafers provide a real time snapshot for characterization of the process at that point. The challenge then lies in anticipating the future needs of characterization and to continue the work that has been presented in this chapter.

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# PART 3
# NEW DIRECTIONS

# 15

# Novel Analytical Methods for Cleaning Evaluation

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*Abstract*

A review of recent trends in analytical characterization of wafer cleaning methodologies is covered in this chapter. For the wafer fab, there have been several improvements in the capabilities of total refection X-ray fluorescence spectroscopy. These would include difference X-ray sources for improved selectivity of analysis and more complete coverage of the entire wafer's surface. Methodologies also have been developed for monitoring trace metal contamination on the bevel and edge of the wafer. Non-visual defects and wafer charging mechanisms have been characterized with Kelvin probe type technologies. While some new methodologies are still highly specialized, lab based techniques that require a synchrotron X-ray source, others are *in situ* monitoring at the wafer processing level, such as electrochemical sensors.

*Keywords:* wafer contamination, contamination monitoring, analysis, TXRF, vapor phase analysis – VPD, vapor phase treatments – VPT, Kelvin probe

## 15.1 Introduction

The fundamentals of wafer contamination [1] and trace contamination analysis on wafers [2] are well covered in these and other references. The purpose of this chapter is to report on recent advances in analytical methodology associated with cleaning and surface conditioning processing. It is useful to consider the various methods of contamination monitoring in terms of different applications:

1. Device and wafer fabrication for high volume manufacturing and research.
2. Pilot line development activities.

Device and wafer manufacturers require detailed analysis when monitoring contamination and surface condition. However, monitoring typically is done only

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for a selected set of wafers in volume manufacturing. This information is provided to the fabrication facility engineers and includes surface roughness, particle counts, surface and bulk metallic contamination [3]. These metrics are used to track the cleanliness of tool, the process stability, and other important items required for manufacturing high yielding devices and high-quality wafers.

The research and pilot line facilities often evaluate a variety of new materials and processes, some of which are selected for volume manufacturing. Research and pilot line facilities, where tools can be shared using different types of materials and processes, must prevent these materials from contaminating the entire process line. For example, hafnium oxide and metal gate (*i.e.* titanium, tungsten, and tantalum-based metals) are now used in volume manufacturing; however, next generation transistors require the introduction of new elements to the gate stack [4]. Elements such as lanthanum or aluminum are candidate materials, while other elements are under consideration. A variety of low dielectric constant (low-κ) and barrier metal materials are also under consideration [5]. These must be monitored to determine if any detrimental effects are contributed due to their introduction.

The Front End Processes Roadmap in the International Technology Roadmap for Semiconductors (ITRS) provides important information about the measurement requirements for contamination. The Surface Preparation Technology Requirements Table [6] lists the maximum allowable amount of metallic contamination for elements that are known to cause problems to the integrity of silicon dioxide and oxynitride gate dielectric layers; the gate oxide integrity (GOI). The Si wafers should have less than $5 \times 10^9$ atoms/cm$^2$ of these critical GOI metals such as Ca, Ba, and Sr. Other metals are known to dissolve in Si and form silicides including Ni, Cu, Cr, Co, Hf, and Pt. Of these, less than $1 \times 10^{10}$ atoms/cm$^2$ should be present on wafer surfaces. Finally, less than $2 \times 10^{10}$ atoms/cm$^2$ of mobile ions such as Na and K should be present on wafer surfaces. The ITRS targets for mobile ions are based on allowable shift in threshold voltage for a transistor. As stated in the ITRS, some metals may remain in the active Si layer while others diffuse through the buried oxide layer interface out of the device layer.

The introduction of high-κ gate dielectrics and silicon on insulator (SOI) wafers may change these targets; however, the necessary data is not available at this time. The ITRS roadmap takes a conservative approach by specifying contamination levels based on experience with bulk silicon wafers and traditional gate dielectrics.

## 15.2 Novel Analytical Methods

Because of the processing challenges of new materials introduced, as discussed in Chapter 16, it is necessary to measure new types of contamination and at a lower concentration level on Si surfaces. The continuous introduction of new materials, especially, high-κ and low-κ dielectrics, metals for gate conductors, along with new patterning processes challenge analytical methods, such as total reflection X-ray fluorescence spectroscopy (TXRF), to increase their capabilities – detection sensitivity and ease of analysis. New methods are being introduced for monitoring surface contamination with the ultimate goal of measurements on patterned wafer surfaces that correlate to product yield.

## 15.3 Recent Advances in Total Reflection X-ray Fluorescence Spectroscopy Analysis

For many years the TXRF instrument used to monitor contamination in the fab has not fundamentally changed. There have been incremental improvements in detection limits with advances in optics, sources, and detectors, but the basic procedure has included the measurement of transition metals at a few locations on silicon wafers. See [2] for an overview of TXRF basics. Monitoring *via* TXRF is often done by running a test wafer upside down through a chamber, such as etching or deposition, and then measuring the contamination transferred to the wafer surface during processing [7]. With the switch to high-κ gate dielectrics and metal gate electrodes, the film must have the added contamination monitored and as well as the contamination from these new layers. Fairly recent innovations in TXRF capabilities have allowed the technique to remain relevant in modern semiconductor fabs. For a comprehensive review please refer to reference [8]. Described below are some of the significant advances.

### 15.3.1 Alternative X-ray Sources for TXRF

Early candidates for high-κ gate dielectrics included Hf and Zr based materials, Chapter 7 presents an in depth discussion of the metal gates and high-κ dielectric gate electrode. As research and development laboratories went through the initial learning process for successful manufacturing using these materials, there was a need to control cross contamination. Monitoring for Zr at $10^{10}$ atoms/cm$^2$ levels with a standard W-Lβ TXRF source was not possible because there is significant background noise from the Si-Kα peak at the Zr-Lα energy region causing poor detection limits. The other option was to have a high energy X-ray source that was greater than Zr's K absorption edge of 18.000 keV. Commercial TXRF instruments have taken two main routes to achieve this; one is to select a portion of the Bremsstrahlung radiation (for example, 24 keV) for an excitation source, and the other is to use characteristic radiation from a tube anode. The Ag tube anode with a Kα line of 22.1 keV has become a popular choice for a characteristic radiation source [9]. Monitoring for Hf contamination on bare silicon wafers is more straightforward. A different source is not needed to observe the Hf-Lα line, but there can be overlaps between the Hf-Lα line (7.899 keV) and Cu-Kα contamination (8.042 keV) if either is present in significant amounts.

As large manufacturers in the semiconductor industry have settled on Hf-based gate dielectrics as a replacement for $SiO_2$-based gate dielectrics, the challenge is measuring trace contamination on the surface of the Hf films with the background in the 6–8 keV region introduced from the multiple Hf lines. Hellin, *et al.* proposed a TXRF method using the W-Lα radiation [10] which at 8.398 keV is below the Hf absorption edge of 9.56 keV resulting in a low background for most of the transition elements. Unfortunately, the W-Lα incident radiation is below the absorption edge for Cu (8.979 keV), limiting the usefulness of monitoring for this important element. Commercial instruments have now been introduced that utilize either an Ir or Pt anode with fluorescence lines at 9.175 keV and 9.443 keV respectively [11, 12]. These

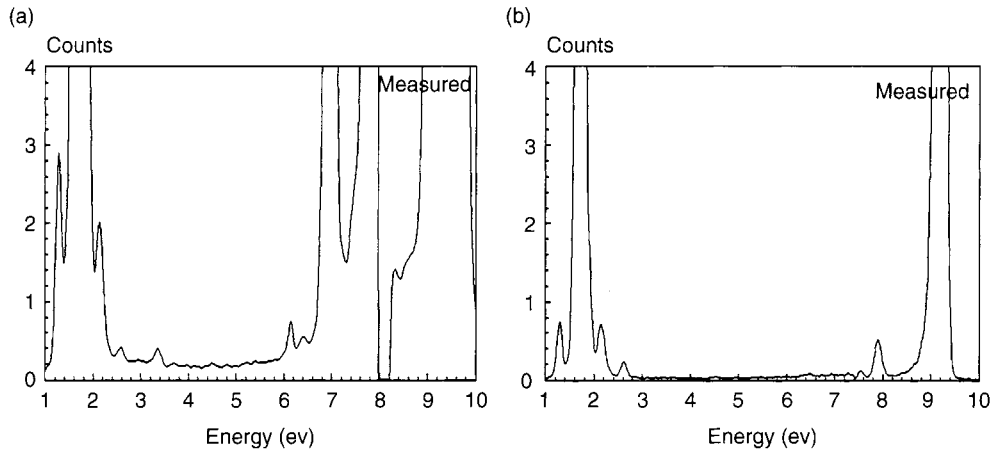


**Figure 15.1.** Total reflection X-ray fluorescence spectra of a 2-nm HfSiO film measured with (a) a W anode and (b) an Ir anode, showing that the Ir anode spectrum has less background noise. Used with permission from the authors.

sources minimize the background from the Hf substrate while allowing for trace level measurements of the transition metals. For example, Figure 15.1 compares the background spectra of a 2-nm HfSiO film collected by both a TXRF equipped with a) a standard W-Lβ source and b) an Ir-Lα source. There is a small peak at the Hf-Lα in the Ir collected spectra as well background from Raman scatter and the Ir escape peak [12], but otherwise the spectra is much cleaner for quantifying low levels of trace metal contamination. Recently work has been published describing methods for measuring trace metal contamination on a high-κ gate dielectric surface for evaluating wet etching of CMOS duel metal gates [11].

Monitoring contamination from light (low Z – atomic number) elements like Na, Mg, and Al are difficult with TXRF with a standard W-Lβ source. Reasons for this include low fluorescent yield of the elements due to a preferred relaxation mechanism that emits an Auger electron instead of a photon, re-absorption of the low energy photons, and a higher background from the Si matrix. Research into the measurement of low Z elements by Streli *et al.* [13–15] thoroughly investigated different sources for more efficient coupling of the photoelectric mass absorption coefficient and has led to improvements in detection limits. For example, using a windowless Si X-ray source Streli was able to achieve detection limits of $9 \times 10^{11}$ atoms/cm$^2$ for Na using only TXRF analysis extrapolating to a VPD-TXRF (vapor phase decomposition-TXRF) detection limit of $3 \times 10^9$ atoms/cm$^2$ on a 200-mm wafer [15]. Commercial TXRF systems have now implemented sources for more efficient excitation of the low Z elements. These systems have multiple X-ray sources that can converge at the same location on a wafer for more complete characterization. The system designed by Rigaku uses a monochromator to select the W-Mα line (1.776 keV) from the rotating W anode [16] while the system Technos International builds uses a multi-tube system (see Figure 15.2) that incorporates a Cr tube (Kα of 5.412 keV). Both manufacturers indicate they can reach detection limits in the low $10^{11}$ atoms/cm$^2$ range for Al with these sources.

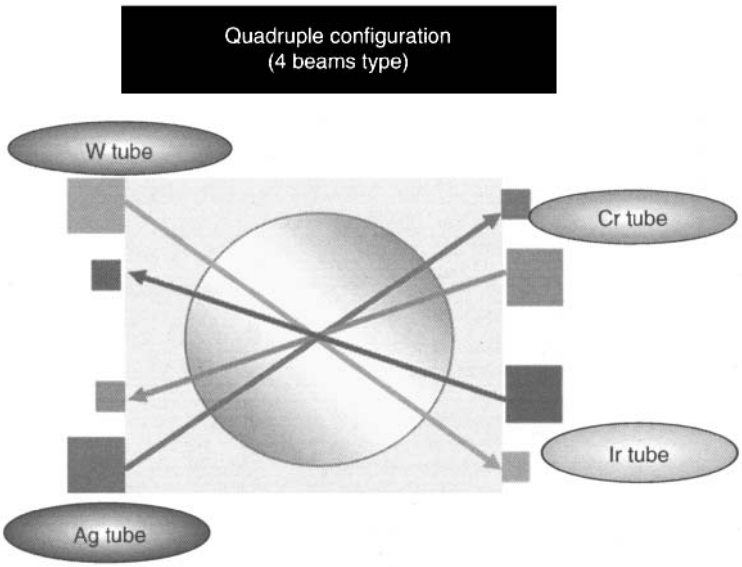


**Figure 15.2.** Example of a 4 beam TXRF system available from Technos International [17]. Used with permission from Technos International.

### 15.3.2 Surface Coverage of the Wafer

One of the advantages of TXRF is its ability to map contamination across the wafer. A standard recipe for a 300-mm wafer may be five points scattered across the surface which takes approximately one hour for the data acquisition. Assuming a quantitative spot size of 1 cm in that hour's time data is collected from about 0.6% of the surface area. To increase surface coverage, the data acquisition time will increase, and thus the throughput will decrease. In contrast, one of the reasons for the widespread use of VPD-based analysis is that contamination from the entire wafer surface is collected and analyzed. This along with the pre-concentration effect discussed by Hues and Lovejoy [2] are the primary advantages of VPD. Some disadvantages to using VPD are the loss of spatial resolution of the contamination, the dilution effect of averaging the contamination such that localized contamination may be lost, and the dependence of the efficiency of the metal collection on the scanning chemistry. To achieve complete surface analysis by TXRF in a reasonable amount of time, Mori recently developed sweeping TXRF [18, 19]. He showed by analyzing hundreds of points across a wafer for a very short integration time (10 sec or less) data could be collected from the entire wafer in approximately the same amount of time as a standard analysis. The accuracy error obtained by not rigidly controlling the incident angle was shown to be negligible if all the spectra are accumulated and summarized into a single spectrum. Additionally, a wafer map showing hot spots of localized contamination can be obtained whereas the detection limits only are about one order of magnitude worse than standard TXRF. The accumulated spectra can achieve good signal to noise averaging achieving approximately $10^9$ atoms/cm$^2$ detection limits for uniform contamination. Figure 15.3 shows an example of the sweeping TXRF – a localized hot spot of Fe

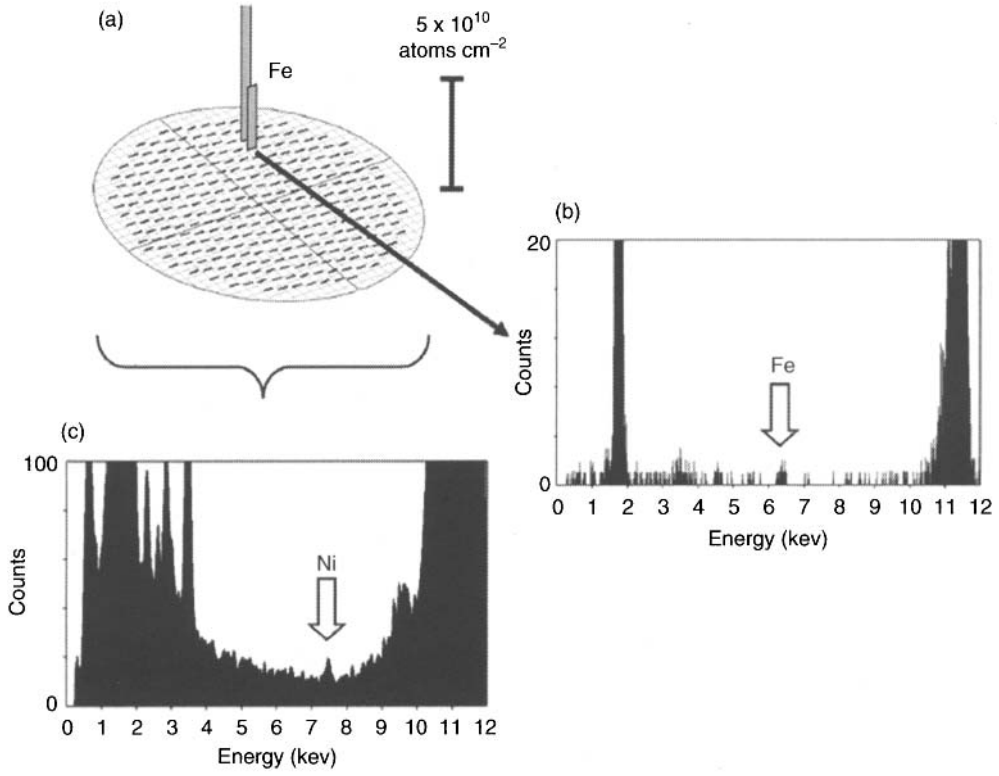


**Figure 15.3.** Result of the test of sweeping-TXRF for a 300-mm wafer, with uniform Ni and localized Fe contamination; (a) Fe is detected at a spot, (b) Fe-Kα peak can be seen at the spot, and (c) the accumulated spectra showed the presence of relatively uniform Ni at ca. $3 \times 10^9$ atoms $cm^{-2}$ [18]. Reprinted from *Spectrochimica Acta Part B*, Volume 59, Mori, Y., Uemura, K., Kohno, H., Yamagami, M., Yamada, T., Shimizu, K., Onizuka, Y., and Iizuka, Y., "Detection of unknown localized contamination on silicon wafer surface by sweeping total reflection X-ray fluorescence analysis", page 1277. Copyright (2004) with permission from Elsevier.

is detected in one area of the wafer while the accumulated spectra shows uniform contamination from Ni.

The major suppliers of TXRF tools designed for device fabrication analysis were quick to incorporate this method of mapping the surface of the wafer as an option on their instruments, and it was embraced by the analytical community. Investigations into contamination control [20], precision and accuracy [11], optimization [21, 22], and a holistic comparison of TXRF based analytical methods [23] soon followed. Figure 15.4 is an example of a 200-mm wafer that had been processed through a wet cleaning step that highlights the value of mapping TXRF. The data was collected from 109 points across the wafer surface; shown is a two dimensional map of the Cu contamination where the dark locations indicate Cu hot spots of about $2.5 \times 10^{10}$ atoms/$cm^2$. The x's represent where a standard TXRF measurement would have taken place and no Cu was detected at those locations. An analysis of this wafer by VPD-ICP-MS (VPD-inductively coupled plasma mass spectrometry) measured $1.3 \times 10^{10}$ atoms/$cm^2$ of copper

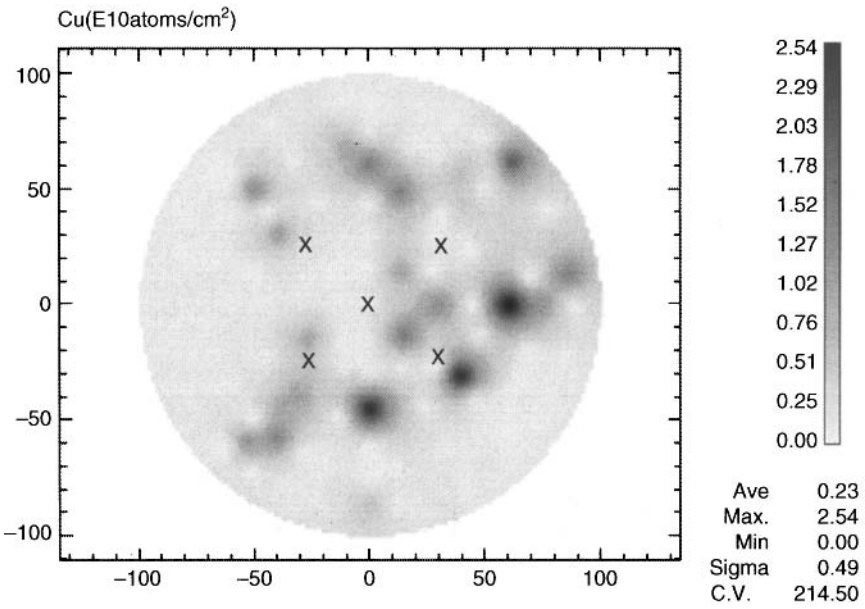


**Figure 15.4.** Two dimensional map of copper contamination, the X's represent coordinates for a standard 5-point map where no copper was measured [11]. Used with permission from the author.

contamination. This example shows the value of increasing the TXRF data density on a wet clean monitor even though the typical contamination from a wet cleaning tool is uniform coverage.

### 15.3.3 Edge Contamination Monitoring of the Wafer

Most TXRF systems have a built-in edge exclusion of ~10 mm to ensure that the incident radiation striking the edge and bevel of the wafer does not scatter into the detector. The edge region significantly contributes to contamination due to transfer of abraded material from edge grip handlers and cassette rails, for example. A recent innovation allowed for rotating the wafer 180° in the analysis chamber so the incident radiation approaches the edge of the wafer from the center [24], having a much lower background than the conventional geometry. As the incident X-ray beam travels nearly parallel to the surface of the wafer, if measurements near the edge of the wafer are attempted by conventional analysis, there will be scatter of the incident beam from the edge and the bevel region of the wafer into the detector. Figure 15.5 shows a schematic of the approach for a conventional incident beam and the approach of a beam that allows for measurement with no edge exclusion. Figure 15.6 shows the intensity dependence on the radius measured for Si and for Fe background counts. There is a drop in Si intensity past the 90-mm radius because the detector has a 10-mm diameter acceptance spot size, so a portion of the detector is over the edge of the wafer and not collecting signal from the wafer.

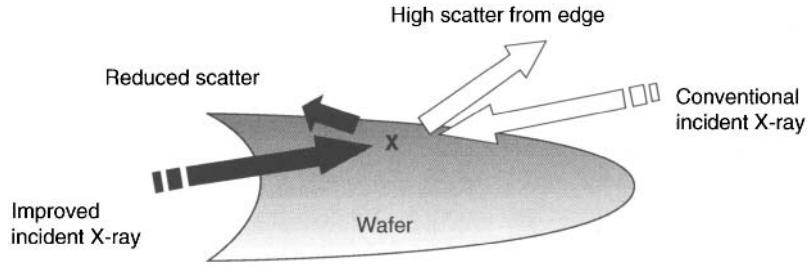


**Figure 15.5.** Example of edge contamination detection by TXRF [24]. Used with permission from H. Takahara.

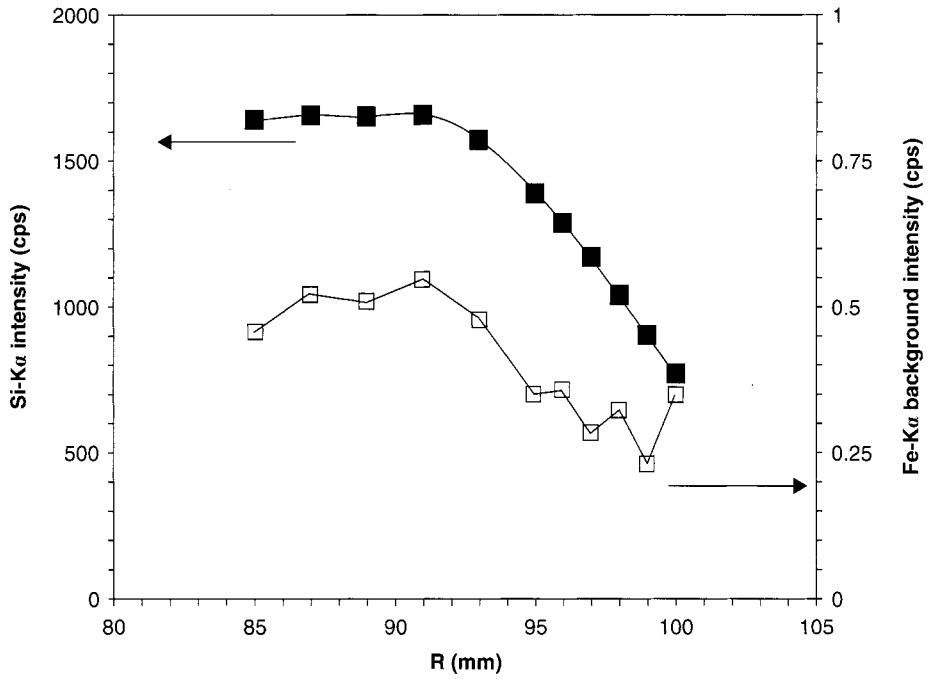


**Figure 15.6.** Intensity dependence on radius, *R*, in measurement coordinates for Si-Kα and Fe-Kα backgrounds for a 200-mm silicon wafer [24]. Used with permission from H. Takahara.

### 15.3.4 Front and Back Surface Monitoring of the Wafer

Measurement of contamination on the backside of a wafer due to the handling components of the tool typically has been accomplished on single-side polished 200-mm wafers by reversing the wafer in the wafer carrier, cycling the wafer upside down through the tool, and then reversing the wafer in the carrier to the polished side face-up for analysis. For 200 and 300-mm DSP (double sided polished) wafers, the contamination monitor wafer can be cycled through the tool and then flipped for standard TXRF analysis. In the interest of conserving monitor wafers, a TXRF tool has recently been developed that allows monitoring of contamination on both the front and back surface of the same wafer provided the wafer is DSP [25]. There

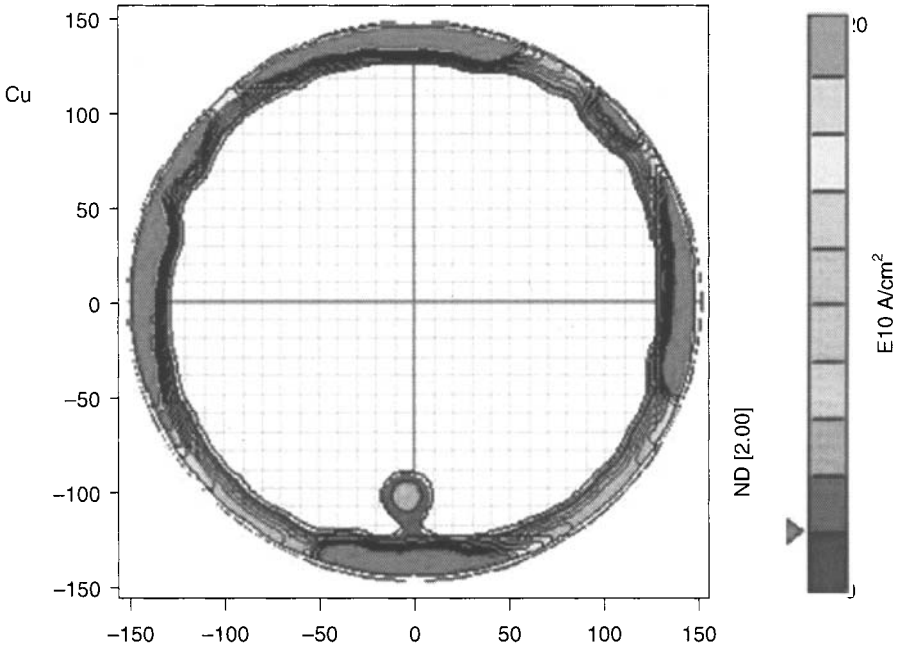


**Figure 15.7.** Copper contamination detected on the back surface of a 300-mm wafer, near the edge [24]. Reprinted with permission from Kohno, H., Yamagami, M., Formica, J., and Shen, L., *Abstracts of Frontiers of Characterization and Metrology for Nanoelectronics*. Copyright 2009, American Institute of Physics.

is a possibility for observing some cross contamination from the TXRF's handling robots and stage, but this tool was primarily developed to monitor contamination on the backside near the edge of the wafer. Figure 15.7 shows a Cu contamination map of the backside of a 300-mm wafer after a sputtering process where the contamination is concentrated close to the edge of the wafer.

### 15.3.5 Contamination Analysis on New Materials

The primary application of TXRF analysis is trace metal monitoring on silicon surfaces. With the rise of new materials, TXRF is also being used to characterize them as well. Earlier in Section 15.3.1, measuring Hf-based films for high-κ gate dielectrics was discussed. Other surfaces such as Ge [26–28], $Al_2O_3$ [29–31], Ru [30, 31], and CoWP [28] have also been characterized by TXRF.

## 15.4 Advances in Vapor Phase Analysis

There have been several reviews of the VPD TXRF technique [8, 32, 33] in recent years. The instrumentation has become automated to the point of "push-button analysis." Recent studies have investigated saturation effects that limit the linearity of the VPD TXRF signal and remediation of these effects [34–36]. Novel ways of depositing nanoliter and picoliter droplets and drying the VPD-residues have recently been studied [31, 37–41]. Some of the benefits found with the nanoliter and

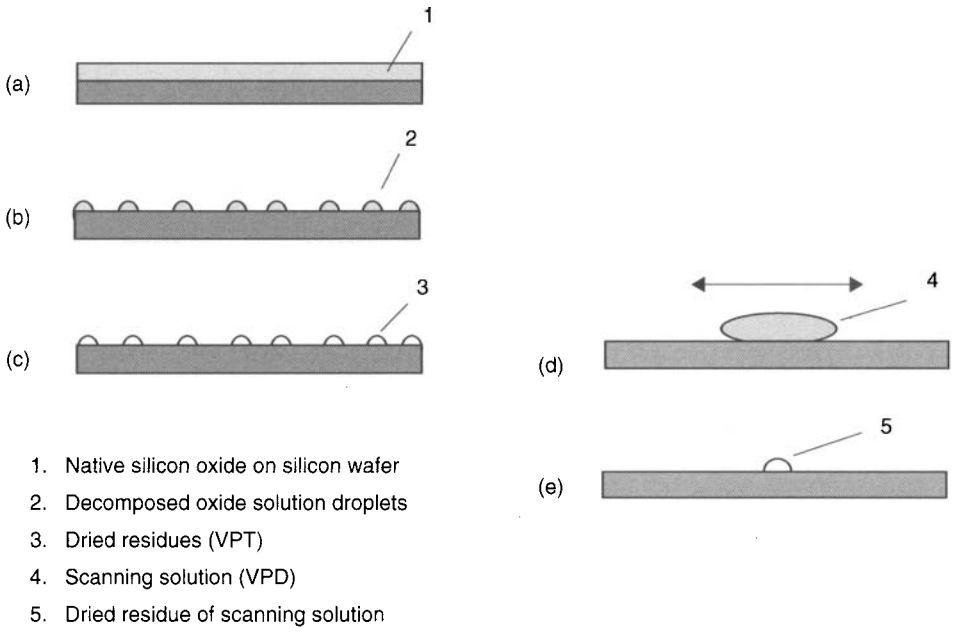


**Figure 15.8.** Flow schematic diagram of VPT-TXRF method compared with conventional VPD-TXRF method [44]:

- VPT-TXRF: (a) → (b) HF vapor decomposition of native silicon oxide → (c) natural drying of decomposed solution droplets → TXRF.
- VPD-TXRF: (a) → (b) HF vapor decomposition of native silicon oxide → (d) collection of decomposed solution droplets → (e) drying of collected scanning solution →TXRF.

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picoliter deposition are improved linearity of the TXRF signal and less signal suppression from additional matrices. An alternative method for decomposing thick (for example, 500-nm) $SiO_2$ films for VPD analysis use purging of the VPD chamber with nitrogen gas [42]. This reduces the water accumulation on the wafer surface from the byproduct of the reaction of HF with $SiO_2$ to an amount that is manageable for automated scanning. An interesting benefit of this process is that the Si concentration, measured by ICP-MS, of the sample from the oxide wafer is only a factor of two greater than the Si concentration from a wafer with a native oxide. This has potential benefits in the ability to quantitatively measure samples by ICP-MS and TXRF that would normally have matrix induced suppression [43]. This suppression is a reduction of the true analyte signal due to energy that would ideally go into creating the signal being absorbed by the matrix (for example, Si or $SiO_2$).

An interesting new sub-set of the VPD process called vapor phase treatment (VPT) TXRF has been recently introduced [44]. In this case, the wafer is exposed to HF vapor similar to the VPD process, but the collection solution from the wafer is not scanned. The condensate is allowed to dry in place allowing the spatial information of the contamination to remain (schematic in Figure 15.8). The premise is that low levels of contamination present on the wafer in plated contamination are converted to residue contamination (see Figure 15.9). This reportedly enhances

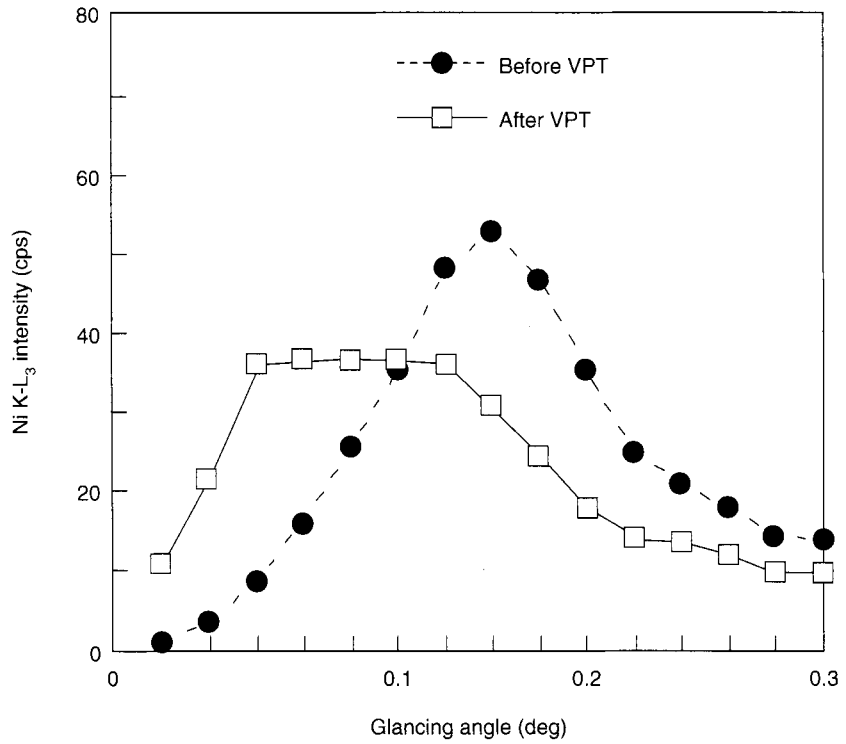


**Figure 15.9.** Angular dependence of fluorescent X-rays before and after VPT for $2 \times 10^{13}$ atoms/cm$^2$–Ni-contaminated standard wafer [44]. Reprinted with permission from the *Japanese Journal of Applied Physics*, Shimazaki, A., Miyazaki, K., Matsumura, T., and Ito, S., Volume 45(12), Page 9037 (2006).

the signal from the contamination at low incident angles of radiation by factors of 4–7 times, depending on the element, enabling quantification down in the low $10^9$ atoms/cm$^2$ range [44]. The VPT procedure combined with the mapping capabilities of TXRF has the potential to be a powerful technique for monitoring low level metallic contamination with spatial information. The Japanese ISO (international standards organization) working group ISO/TC201/WG2 implemented a round robin study of the VPT TXRF technique which resulted in a wide and inconclusive range of VPT signal enhancement factors; hence, work is being continued on this question [45].

## 15.5 Trace Metal Contamination on the Edge and Bevel of a Wafer

In section 15.3.2 the importance of measuring contamination on the whole wafer is discussed with respect to recent modifications to the TXRF system's ability to measure wafers with no edge exclusion. However, cross contamination of metallic contamination from the edge and bevel of the wafer can also occur and must be considered [46, 47]. Due to scattering of the incident radiation, TXRF cannot be used to measure the bevel or the edge of a wafer. One analytical technique that can be used to measure

on the bevel is time-of-flight secondary ion mass spectroscopy (TOF-SIMS); however, the angle on the bevel makes consistent analysis difficult, and the small analytical spot size would require many analyses for a representative sample set.

There have been methods of chemical extraction of the metallic contamination from the edge of the wafer that have been developed [24, 46, 48] where the extraction solution is subsequently analyzed by ICP-MS or TXRF. The extraction solution is usually similar to a VPD scanning solution being made up of HF, $H_2O_2$, and $H_2O$. In this case though, the concentration of HF is higher because the wafer may not have gone through a VPD-type step and there would be an oxide (native, chemical, or thermal) on the Si wafer. The higher concentration of HF allows for the surface to be converted from hydrophilic to hydrophobic as the wafer slowly rotates through the extraction solution. This prevents streaking or running of the extraction solution and allows for control over the area of the bevel and edge that is analyzed.

Figures 15.10a and 15.10b show a wafer vertically supported with the extraction solution in the sample boat [46]. The sample collection and wafer loading are manual procedures in this case. Another manual version of this type of analysis has the wafer horizontally supported, rotating through a sample cup, where the extraction solution is held in place by surface tension as shown in Figures 15.11a and 15.11b [48]. A fully automated version of the bevel and edge analysis has been incorporated into an automated VPD system where the standard VPD scanning nozzle has been be replaced with a nozzle designed to scan the bevel and edge of the wafer as shown in Figure 15.12 [24]. In this case the scanning droplet can be programmed to be dried on a wafer support for TXRF measurement or deposited into a vial for measurement by ICP-MS.

## 15.6 Kelvin Probe Technologies

There has been an influx of recent publications on non-contact measurements where the surface of a wafer is scanned by a metal probe and variations in the difference between the work function of the probe and the wafer surface are measured [49]. This can be used as an in-line monitoring step to capture defects that are not detected by current optical defect inspection equipment. A data map of the wafer is shown in Figure 15.13 from a Qcept Technologies instrument. Analysis of these variations in contamination levels allows process monitoring. Figure 15.13 shows processed-induced charging that is caused from single wafer cleaning [50]. Statistical process control can be applied to the data; when the measured charge surpasses the upper control limit the wafer is flagged.

Characterizing wafer charging associated with cleaning process and the efforts to mitigate the charging have been reported in [51, 52]. Kelvin probe based measurements have also been applied to other non-visual defects including trace metallic contamination, ionic contamination, and organic contamination on the front side, backside, and edges of wafers on both patterned and un-patterned wafers [53–57]. Identification of the various types of contamination and the concentration are under investigation, but this technique has been shown to allow rapid screening that can supply coordinate information for more efficient supplemental analysis by other techniques (*i.e.* TXRF, Auger, XPS, or SIMS).

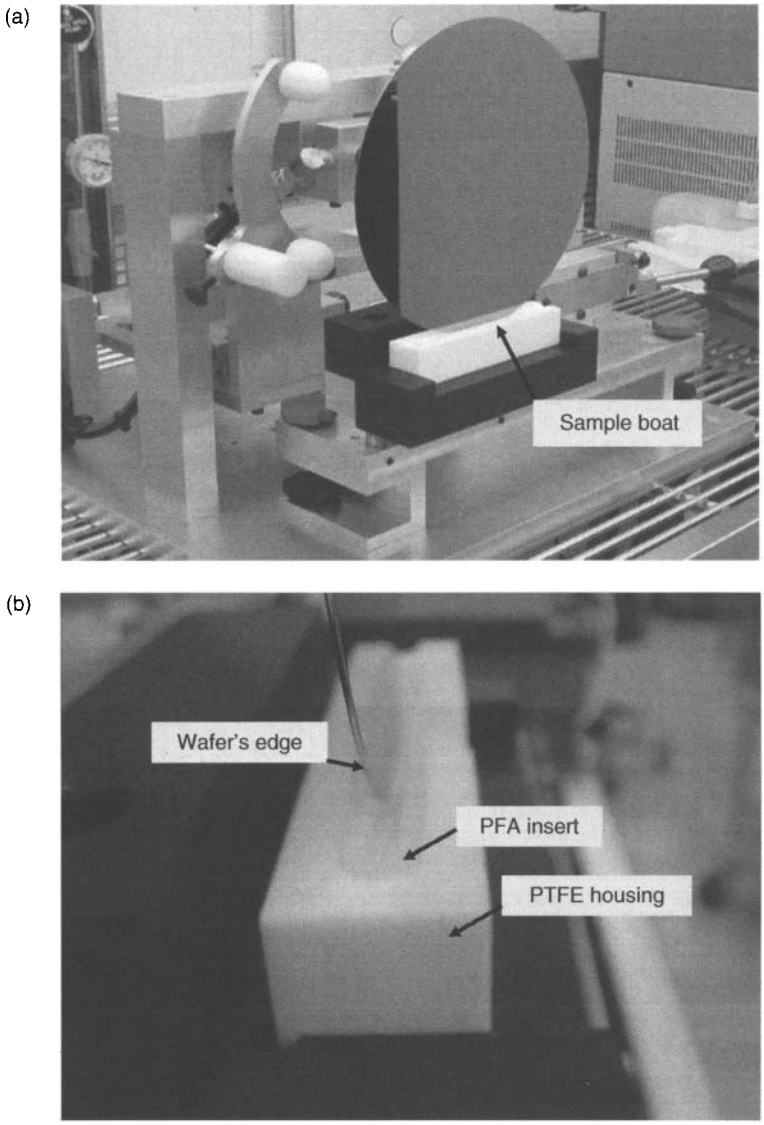


**Figure 15.10.** (a) Wafer vertically supported for analysis of the bevel and edge, and (b) side view of the wafer edge making contact with the extraction solution in the Teflon® perfluoroalkoxy (PFA) insert of the sample boat [46]. Used with permission from SPIE; Sparks, C., Gondran, C., Lysaght, P., and Donahue, J., "Novel Technique for Contamination Analysis Around the Bevel and Edge Exclusion Areas of 200 and 300 mm Silicon Wafers," *Process and Materials Characterization and Diagnostics in IC Manufacturing*, Volume 5041 (2003).

Other applications of Kelvin probe type technologies from KLA-Tencor Quantox™ have been used to extract electrical measurements; for example, current voltage and conductive voltage data, to evaluate pre-gate cleans [58]. The Quantox™ methodology can also be used to monitor surface charge, carrier, and generational lifetimes [59–62].

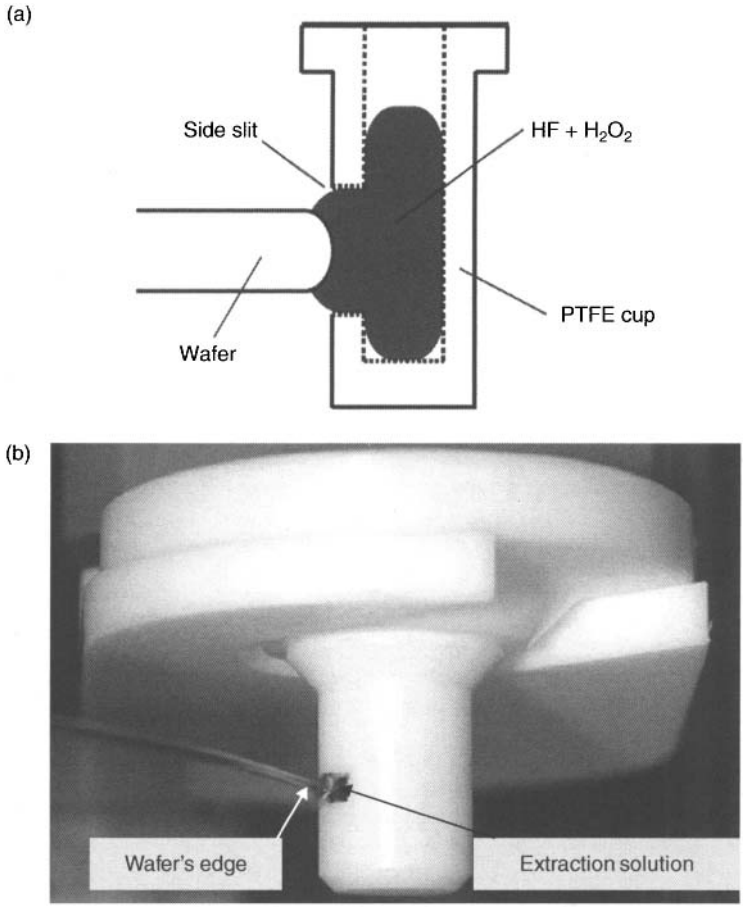


**Figure 15.11.** (a) Schematic of wafer horizontally supported and rotated through extraction solution and (b) image of sample collection in progress [48]. Reprinted with permission from the *Proceedings of the 65th Autumn Meeting of the Japanese Society Applied Physics*, Sakurai, Y., Mori, Y., and Uemura, K., Page 3p-B-17 (2004).

## 15.7 Novel Applications of Electron Spectroscopy Techniques

The basic principles of X-ray photoelectron spectroscopy (XPS) are covered in [2]. Angle-resolved XPS (ARXPS) is a method where surface and depth information can be obtained by collecting the spectra while varying the angle between the X-ray source and the sample, a simplified schematic is shown in Figure 15.14 and theoretical details can be found in reference [63].

Many other studies have been performed. Characterization of sidewall post-etch residue cleaning has been demonstrated with ARXPS [64, 65]. In these studies, the authors demonstrated they could quantitatively resolve the composition of the field, trenches, and sidewalls. The data suggested that there was incomplete removal of post-etched residue from the sidewalls, even after cleaned, due to the level of F detected [65]. Roughening of the surface of Si after HF etching

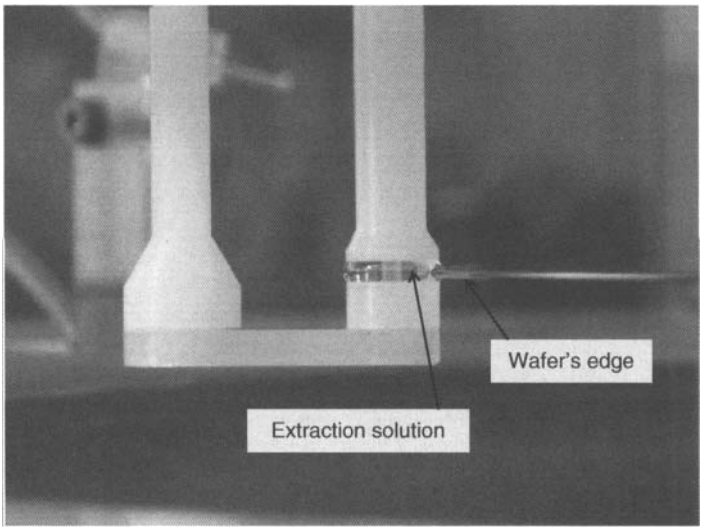


**Figure 15.12.** Automated bevel and edge analysis chemical extraction design from Technos International [24]. Used with permission from H. Takahara.

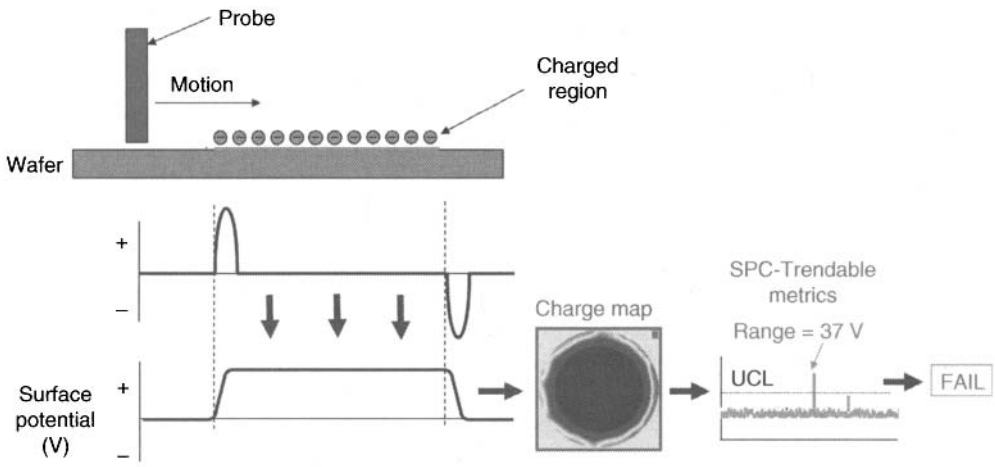


**Figure 15.13.** Schematic of surface potential difference imaging from Qcept [50]. Used with permission from Qcept Technologies.

was characterized with infrared (IR) spectroscopy and ARXPS, from this study they found a new bonding configuration (a reduced form) of Si [66]. The quality of chemical oxides formed on SiGe after wet cleans was investigated with ARXPS. A comparison of $H_2O_2$ cleaning processes showed less C contamination and improved oxide quality [67]. A post-CMP clean study of chemical oxides using a HF + $H_2O/O_3$-based clean on SiGe (20%, 50%, and 100% Ge) was performed with ARXPS [68]. Surface oxidation (and removal of the oxide) of W films deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD) was studied by ARXPS, for both as-deposited films and post-cleaning samples [69]. Angle

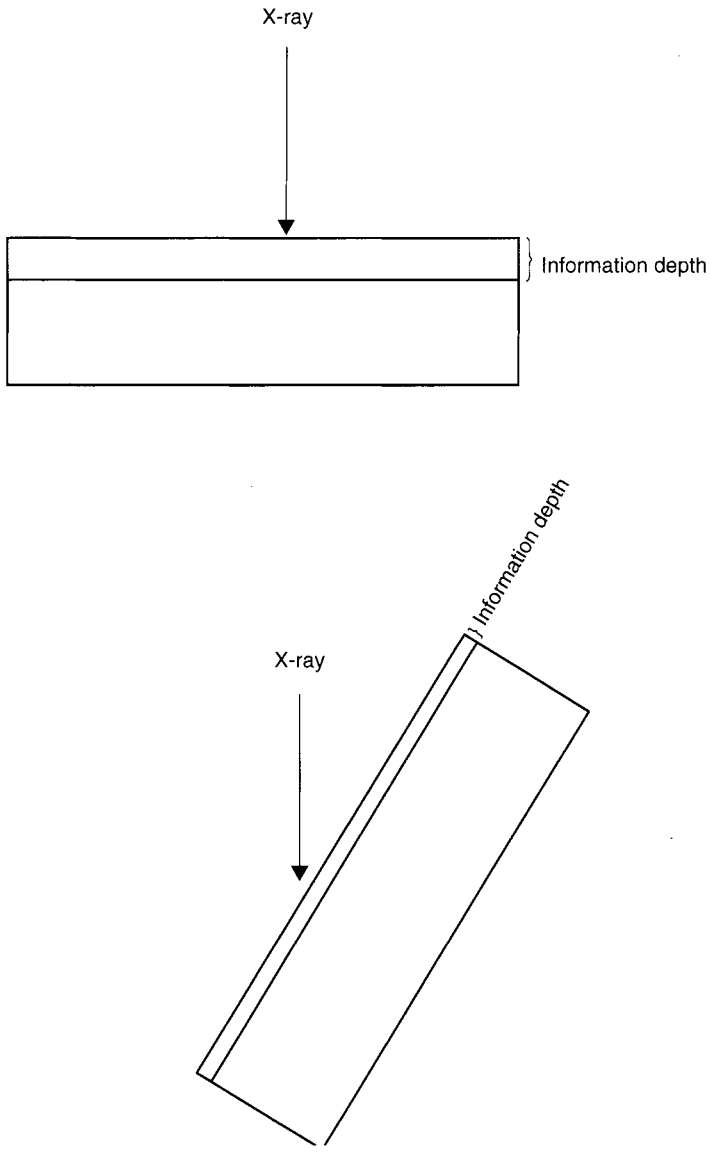


**Figure 15.14.** Schematic diagram of angle resolved-XPS where varying the X-ray's angle of incidence affects the information depth of the signal. Courtesy of Chris Sparks.

resolved XPS was also used to study the affect of different wet cleaning and storage conditions on the oxidation state of Cu films [70]. The surfaces of ultra low-κ films post-CMP cleaning processes were characterized with ARXPS, it was found that using an oxalic acid plus derivatives cleaning solutions changed the structure of the surface and damaged the films while using a citric acid plus derivatives clean cleaning solution did not [71]. The affect of the surface condition on the growth of high-κ dielectrics have also been characterized with ARXPS [72] and the results from ARXPS were compared to TOF-SIMS and RBS data and used to evaluate the authors' model for surface coverage.

## 15.8 Novel X-ray Spectroscopy Techniques

Some groups have utilized the capabilities of synchrotron facilities to further characterize the surface of semiconductor surfaces. For example, the group at the Physikalisch-Technische Bundesanstalt (PTB) has fully characterized their instrumentation to allow reference-free calibration with TXRF [73, 74]. Near edge X-ray absorption fine structure (NEXAFS) was used to analyze organic compounds on Si [75, 76] and to characterize self-assembled monolayers (SAM) on Ge [77]. X-ray reflectivity [78] has been adapted by the semiconductor metrology community for monitoring of film layers and interfaces. Using a high energy synchrotron source (HEXRR) has been used to characterize drying procedures in bonding SOI wafers [79, 80].

## 15.9 Electrochemical Sensors

To evaluate the rinsing step on patterned wafers, an electrochemical residue sensor (ECRS) has been developed for *in situ* monitoring of the ionic species [81]. These sensors show an improvement over the conventional method of bulk water conductivity for optimal determination of the rinsing endpoint. They are being used to test more efficient rinse recipes involving such parameters as wafer spin rate and water temperatures [82, 83].

## 15.10 Summary

Clearly progress in properly analyzing and characterizing semiconductor cleans processes has been made recently. A more complete picture of contamination on monitor wafers from the edges and bevels to covering the entire surface is now possible giving the process engineer valuable data with which to better understand their processes and troubleshoot excursions. Measurements that are *in situ* or on product wafers provide a real time snapshot for characterization of the process at that point. The challenge then lies in anticipating the future needs of characterization and to continue the work that has been presented in this chapter.

## Acknowledgments

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# 16

# Stripping and Cleaning for Advanced Photolithography Applications

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*Abstract*
This chapter discusses the processes and chemistry related to photoresist stripping and cleaning. Suppliers of these products are increasingly challenged to adapt to the new demands introduced by advanced integrated circuit designs and by increasingly difficult business conditions. Meeting these demands requires attention to cost, materials compatibility issues, and concerns about toxicity and environmental persistence of chemicals used in manufacturing. Maintaining a specialty mind-set in a commodities environment will be a continuing challenge in the industry. The specialized requirements of formulating products to address the multitude of new materials used for advanced chip manufacturing will severely test the "specialty" *vs.* "commodity" paradox, and stripper suppliers will increasingly face challenges that have already impacted other segments of the wet chemical supply chain.

***Keywords:*** high dose implant stripping, high-κ metal gate stripping, advanced low-κ stripping, photoresist removers, solvents, pattern collapse, surface wetting

## 16.1 Introduction to Advance Stripping Applications

As with all operations dealing with current semiconductor manufacturing, the processes and chemistry related to photoresist stripping and cleaning are continually being challenged to adapt to the new demands introduced by advanced integrated circuit (IC) designs and by the increasingly difficult business conditions. Meeting these demands requires attention to cost, materials compatibility issues, and concerns about toxicity and environmental persistence of chemicals used in manufacturing. Among the driving forces affecting the formulation of photoresist strippers and removers are:

1. The move to new materials, such as porous low-κ and metallic-based high-κ dielectrics. (κ = dielectric constant)

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2. Special requirements introduced by narrow features and high aspect ratios.
3. Increasingly complex process steps.
4. Strippers designed to work with bi-layer and tri-layer resists.
5. The move to single wafer processing tools.

In the front end line (FEOL), higher implant doses combined with new gate metals and dielectrics are particularly challenging. Adding to future stripping and clean challenges, manufacturers are contemplating completely different memory construction techniques including phase-change and spin-active materials for non-volatile memory applications. The sum of these issues substantiates an observation made in the early days of VLSI (very large scale integration) manufacturing: "...no single resist stripping chemical or technique is suitable for all applications..." [1].

Many of the issues related to new materials are addressed extensively in other chapters in the Handbook; however, they will be briefly discussed here to give readers a full understanding of the requirements of photolithography cleaning as the industry moves forward.

## 16.2 Historical Background

While this chapter addresses new challenges introduced by advanced processes, to appreciate how strippers and removers evolved to address the task at hand, a historic prospective is provided. Photoresist strippers (as the name might imply) are related to "paint strippers" formulated with strong, polar organic solvents, such as N-methyl pyrrolidone, also known as 2-methyl pyrrolidone (NMP). A good review of the evolution of photoresist cleaning products can be found in an article by Peters *et al.* [2].

### 16.2.1 Solvent-Based Strippers

In the early days of the semiconductor industry, photoresist strippers were not formulated as such. Engineers probably used what was on hand in the fab to remove resist, such as RCA cleans [3], acetone, or photoresist thinner (a solvent sold by resist vendors to allow users to reduce resist viscosity as a means to adjust coating thickness and for cleaning of the photoresist coater spinner bowls). These cleaning methods were supplanted by more purposefully formulated products as processing became more challenging to meet design rules; for example, post exposure hard baking to stabilize resist images and introduction of dry etching to avoid lateral etching. Implementation of hard baking led to organic films that were resistant to many solvents (*e.g.* acetone, thinners) resulting in particulate contamination due to partial or non-removal of resist. As feature size diminished, care was needed to avoid loss of metal due to corrosion, because a few percent of material loss during stripping was no longer viable. Reactive ion etching of resist introduced new trials. In addition to the bulk resist, so called "dry etching" must remove the highly cross-linked surface layer and the etch residue – a complicated mixture of inorganic,

organic and fluorocarbon materials. This residue does not differ greatly from the underlying substrate; therefore, the stripping process must be controlled to prevent damage to the film beneath the resist. Obeng and Raghavan proposed that penetration, swelling, and dissolution are the steps involved in resist removal [4]. If the rate of swelling exceeds the dissolution rate or the solvating power, the typical result is adhesion failure resulting in the generation of particles across the wafer surface – an unhappy result. Hence, the history of stripper technology outlined below is comprised of a series of attempts by formulators to match the three factors – penetration, swelling, and dissolution. It is relevant to note etching processes significantly differ among semiconductor manufacturers. No place is this more evident than in dry etching. The amount of residue generated during the etching process and the degree of difficulty in removing that residue can vary considerably among chipmakers and, in some cases, even among fabs running the "same" process for the same manufacturer.

Initial resist stripper formulations were fairly noxious compositions from both environmental and health perspectives. Exemplary is an often referenced material; Indust-Ri-Chem J-100, which contained perchloroethylene, *o*-dichlorobenzene, phenol, and alkylaryl sulfonic acids and was developed for resist removal in the printed circuit board industry. One of the first products in response to environmental and health issues was a product called NoPhenol 922 (EKC Technology), which contained a sulfonic acid, a solvent, and catechol [5, 6]. While these types of products were marginally better from an environmental perspective, they required the use of a solvent rinse after stripping to remove the chemical. This additional step was seen to add cost due to additional processing time and expense as well as necessitating disposal of the rinse solvent. Hence, the next advancement in stripper development was the advent of water miscible strippers permitting water rinses.

The mid-1980's were dominated by the use of a variety of strong, polar organic solvent-based formulations. Popular primary solvents included NMP, tetrahydrothiophene-1,1-dioxide (sulfolane), and dimethylsulfoxide (DMSO). A variety of co-solvents or additives were used including glycol ethers such as diethylene glycol mono-(m)ethyl ether.

The next incremental improvement in strippers came with the addition of basic ingredients such as amines or tetraalkyammonium hydroxides [7] to formulations containing polar solvents. One issue with these water-miscible strippers was that during the water rinse, corrosion caused significant damage to exposed metal (Al/Cu). This issue lead to two innovations that are still being employed in formulations used today – the inclusion of corrosion inhibitors and formulations with controlled pH. It is worth pointing out that specifying pH in predominately solvent-based formulations is somewhat problematic. In fact, what is being controlled is the pH at some high dilution; what the wafer "sees" when being rinsed, as described by Lin *et al.* [8]. The Lin patent also introduced the use of solvent parameters as a means of designing "stripping power" and as a way to show novelty to patent offices. The inclusion of amines led to the addition of hydroxylamine providing, arguably, the most powerful and successful stripping products of the 1990's.

### 16.2.2 Hydroxylamine Photoresist Residue Removers

The first mention of hydroxylamine (HA) as a stripper component is in a patent by Lee [9] that claims the use of hydroxylamine ($HO\text{-}NH_2$) in mixture with alkanolamines ($HO\text{-}R\text{-}NH_2$, where R is a hydrocarbon fragment). This initial disclosure led to a shower of patents, primarily from EKC Technology (now a business of DuPont) and ACT (now a business of Air Products), that claimed improvements for stripping and residue removal based on using additional solvents, corrosion inhibitors, and other functional additives.

Each of these companies launched very successful product lines based on initial offerings EKC 265® and ACT 935® that came to dominate the photoresist stripper market. The predominance of HA-based products began to plateau with the introduction of Cu interconnect technology. Hydroxylamine in these formulations represents the addition of a more "active" component in stripper formulations that can deleteriously affect metal features. It has been postulated by Lee that HA is able to reduce metals in the etch residue to a lower oxidation state and hence render them more soluble [10].

Hydroxylamine is a powerful Cu etchant and, despite considerable research efforts, no suitable corrosion inhibitor has been found for this formulation, Chapter 11 outlines the progress of corrosion inhibitors. Indeed, EKC even developed a line of CMP (chemical mechanical polishing) products based on HA [11]. Nevertheless, for the removal of dry etching residue and cross-linked photoresist on Al interconnect technology, such as used in DRAM (dynamic random access memory); these products remain unchallenged for their effective cleaning capability.

### 16.2.3 Fluoride-containing Strippers

One of the first-mentioned uses of fluoride in stripper compositions is in a patent to ACSI [12] (now owned by ATMI) that detailed a formulation containing anhydrous ammonium fluoride salts and a glycol. Both ACT (NE-series products) and EKC produced fluoride-containing products in short order, and ATMI subsequently marketed a semi-aqueous version [13]. These products quickly became ubiquitous and began to penetrate production due to their "semi-aqueous" nature, and because HA was in short supply due to a series of tragic accidents related to its production.

The mechanism of action is not well understood, but it is likely that trace amounts of HF or $HF_2^-$ allow for the removal of underlying $SiO_2$ and allow the other components of the formulation to penetrate and swell the residue. The chemistry of HF etching is discussed in Chapter 3. Controlled etching of $SiO_2$ by $HF/HF_2^-$ in purely aqueous systems is a well-studied area, but still elicits comments and analysis [14]. When considering the added complications from introducing solvents into semi-aqueous media, it is no wonder that these formulations can be modified and tuned for specific applications.

One other factor that can be attributed to the increased use of fluoride-containing strippers was the introduction of Cu interconnects. While HA-containing products

attack Cu, fluoride-containing products can be inhibited from attacking Cu by the introduction of corrosion inhibitors and by controlling pH through buffers or other suitable means.

## 16.3 Recent Trends for Photoresist Stripping and Post-etch Residue Removal

### 16.3.1 New Materials and Compatibility Issues

The challenges introduced by new materials cannot be underestimated; consequently, the variety and permutations of potential material combinations could make this section extensive indeed. For brevity, select areas will be covered.

### 16.3.2 Germanium

Because of its higher mobility and also its ability to induce strain in the Si lattice that enhances the properties of Si-based devices, germanium is increasingly being exploited in new semiconductor applications. Historically, of course, it has suffered from the lack of a robust oxide, which is one of the factors that have enabled the Si-based semiconductor industry. The quest for a suitable passivation methodology for germanium has been long and arduous. For wet chemical applications, strategies using sulfur-based and halide passivating agents have so far given limited, but not sufficient success. Chapter 12 discussed the passivation of germanium surfaces in detail. Passivation of germanium surfaces continues to be one of the unmet needs for full utilization of germanium as a semiconducting material in commercial devices [15, 16], and these issues are expected to apply to FEOL photoresist stripping applications as well.

### 16.3.3 Phase-change Memory Material

Germanium also makes an appearance in the leading phase change technology. Germanium selenium telluride (GST) is aggressively being developed for use in these applications. The FEOL stripping and cleaning processing for this material will require removal of photoresist residues. Although the cleaning of these materials is not typically a subject of discussion in current publications, some work has been done on wet-etching of GST. While not directly related to cleaning, the peculiar behavior of these "microcrystalline" films in nitric acid etches suggests a multitude of opportunities for surprising results with aggressive chemical treatments. In particular, Figure 16.1 shows that heat annealed crystalline GST films are most vulnerable to attack by nitric acid at the thermal boundaries caused by the heating coil of the hotplate. In addition, amorphous films were found to etch much more uniformly [17]. This phenomenon, coupled with the selective dissolution of the components by the acid [18], indicates that cleaning GST features after patterning may offer interesting challenges.

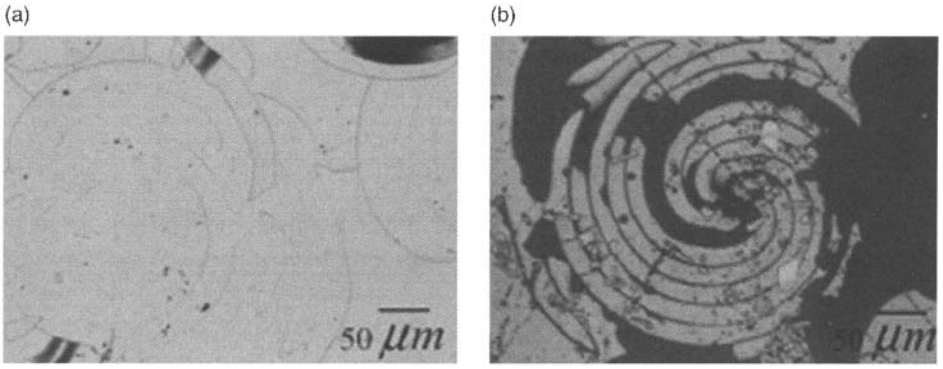


**Figure 16.1.** Selective attack of 20 wt% nitric acid at the thermal boundaries of a crystalline GST film; a) 10 sec and b) 50 sec [17]. Used with permission of Cheng, H.-Y., Jong, C.-A., Lee, C.-M., and Chin, T.-S. *IEEE Transactions on Magnetics*. © 2005 IEEE.

### 16.3.4 Porous Low-κ Materials

Another area receiving a great deal of attention is low-κ porous dielectrics and the damage to these materials caused by the cleaning process. An example is post-CMP cleaning and plasma photoresist removal over low-κ dielectrics, where, as with stripping, a primary goal is to either prevent an increase in dielectric constant on cleaning or, alternatively, to recover the dielectric properties after cleaning, perhaps with use of a recovery fluid [19]. An elegant technique for determining the amount of penetration into porous low-κ films by solvents and other components of cleaning formulations is with the use of ellipsometric porosimetry (EP) [20]. Rao and coworkers have recently used this technique to derive diffusion information of certain molecular probes into porous films and have related diffusion rates to the molecular size of the probe molecules [21]. Figure 16.2 shows penetration rates derived for a surfactant probe into plasma enhanced chemical vapor deposition ortho-silicate glass (PECVD OSG). In this case, there is a simple trend observed based on probe concentration; however, the use of this technique to screen formulation components for pore penetration is a useful extension of this work.

Additionally, moisture uptake into porous low-κ dielectric films from various processes cause concerns. Reidy *et al.* used $D_2O$ to monitor moisture and water adsorption into post-stripped damaged low-κ materials [22]. They have shown that deuterium uptake is a potentially useful technique for characterization of the moisture uptake properties of low-κ materials.

### 16.3.5 High-κ Materials

The complexities of modern day cleaning processes can be seen in the use of a combined dry and wet processes needed to selectively etch $HfO_2$ in the presence of a variety of other FEOL materials. Wet etching is enabled by post-deposition annealing and plasma induced damage of the $HfO_2$. Chapter 7 outlines the issues and options for removing the high-κ materials. The cleaning chemistries were dilute acid solutions. The choice of specific formulation depended on the other materials present and on whether single wafer or batch processing was used [23].

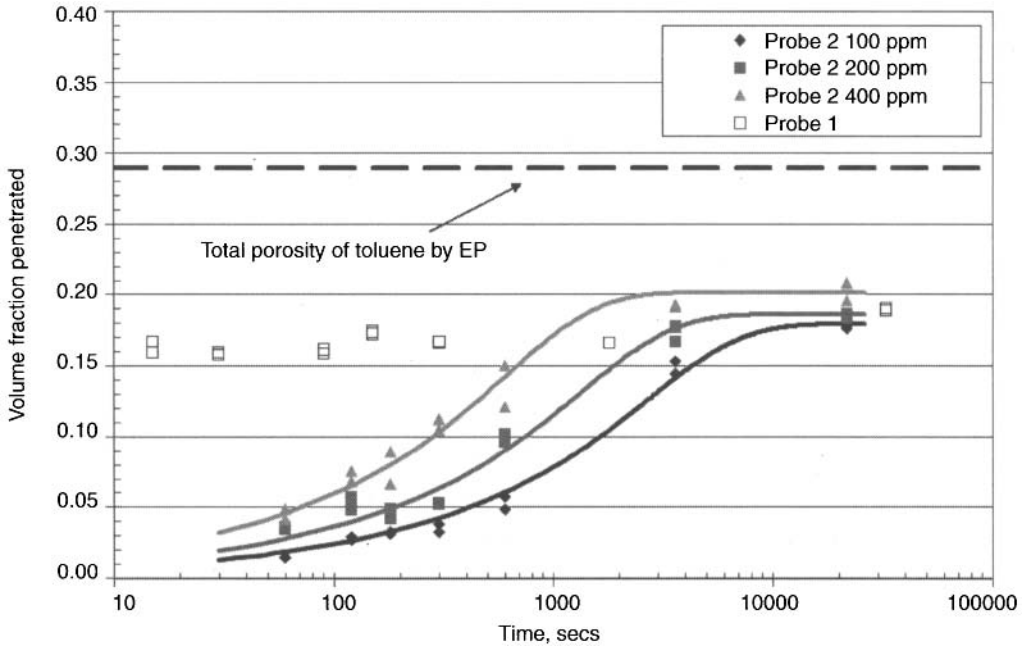


**Figure 16.2.** Results of ellipsometric porosimetry to show the penetration rates of a molecular probe that measures their diffusion into porous low-κ dielectrics [21]. Used with permission of Air Products and Chemicals.

### 16.3.6 High Dose Ion Implanted Photoresist

In addition to new materials challenges encountered in FEOL cleaning, perhaps the greatest current challenge in this area is the removal of implant-hardened resists. High dose implant stripping (HDIS) is addressed in more detail in Chapter 8 of this book; however, it is worth mentioning with respect to the overall context of photoresist stripping.

It is well-known that the ion-implant process leads to dehydrogenation and cross-linking of organic photoresist. Traditionally, strongly oxidizing cleaners such as $H_2SO_4/H_2O_2$ (sulfuric acid hydrogen peroxide mixture – SPM) or very aggressive oxidizing plasma stripping have been employed to address this issue. Continued scaling of features, however, has lead to stringent reductions in the allowable amount of silicon removal during the cleaning process. The increasing use of metal gates also complicates the issue since these metals are typically susceptible to oxidation. Further, dosing levels continue to increase exacerbating the problem [24].

These challenges have forced providers of equipment and chemical cleaning solutions to change their approach. One approach has been to use reducing or "forming" gas mixtures to strip the hardened resist. In addition to preventing oxidation of metal or silicon substrates, this technique avoids the loss of nitrogen from high-κ dielectric materials such as HfSiON. Stripping rates under the reductive conditions, however, are slow [25].

Very recently, a steam-based process has been advocated for removal of high-dose implanted resists. According to researchers at FSI, the introduction of steam to SPM cleans increases the efficacy of removing the carbonized resist [26]. It was proposed that high temperature steam serves to enhance the radical content of the peroxide mixture. Substrate oxidation remains to be an issue with this method, although the increased etching rate of photoresist minimizes the exposure of the underlying materials to the aggressive environment [27–29].

## 16.4 Single Wafer Tools

For 300-mm wafer processing and sub-45 nm geometries, attention has been paid to the tools being used and the associated processing. The cost of a 300-mm wafer by the time it reaches the back end is many thousands of dollars and any processing issues that may impede high yield must be thoroughly evaluated. Batch wafer processing raises the concern that the misprocessing of an entire lot of wafers is an expensive proposition. The added concern of particle generation and contamination from the front side of one wafer to the backside of other wafers in a cassette has led to a search for alternatives to batch processing.

Single wafer processing (SWP) addresses these concerns. Additionally, single wafer tools (SWT) provide better control of the processing parameters. Single wafer processing has been used in the semiconductor industry for nearly two decades following Texas Instrument's demonstration of a 100% SWP line under sponsorship by DARPA [30]. The aim of this work was to demonstrate SWP for "dry" processing, but specialized applications using SWP for wet applications, such as backside cleaning, emerged [31]. These benefits were soon realized in mainstream manufacturing applications with the implementation of SWT processing for back end of line (BEOL) processes and, more recently, for FEOL processing. The cleaning product choices for a SWT process depend on the substrates exposed, the critical dimension of the devices, the residue type (*i.e.* plasma stripped, with or without polymer), and the overall cost of ownership.

Single wafer tool manufacturers have become numerous as well. The SWT manufacturer with longest tenure is SEZ (now owned by Lam Research), but tool offerings are now possible from Akrion, Applied Materials, Dai Nippon Screen (DNS), FSI International, Lam Research, Semitool (now owned by Applied Materials), SCP Global Technologies (now owned by Applied Materials), Solid State Equipment Corporation (SSEC), Tokyo Electron (TEL), and other companies. Single wafer platforms are sold with multiple processing chambers to provide higher wafer throughput. Each SWT manufacturer offers their own unique twist to wafer processing, but all offer some method of chemical delivery *via* spraying (except for the AMAT Emersion and a tool offered by SCP Global Technologies which are immersion SWT platforms), a drain system that segregates the process chemical waste from the DIW (deionized water) rinse, and a method of wafer drying either by $N_2$/spin, isopropyl alcohol (IPA) vapor, or combinations thereof.

Because SWP necessarily requires short process times for each individual wafer, manufacturers have devised specific designs to physically enhance the cleaning process. Examples include the use of:

1. A non-contact, megasonic wand on the Akrion Goldfinger. This feature is claimed to offer enhanced cleaning with increased particle reduction;
2. The ability to deliver chemical to either the front side, back side, or both in a nitrogen-purged chamber with Advanced Rinse Dry (ARD) using a DIW-wetted, IPA vapor dry, offered on the Semitool Raider platform;
3. A vertical-moving wafer chuck within a process chamber with vertically-arranged process levels and multiple chemical dispenses offered on the SEZ DaVinci® platform;
4. A combination immersion/single wafer spray that can use either a megasonics or atomized spray nozzle offered by Solid State Equipment Corporation.
5. The C3™ technology on the Lam Research 2300® Serene™ tool combining linear wafer motion with chemically-driven, single-wafer cleaning to remove residues with chemical exposure times of a few seconds.
6. SCP Global Technologies has a single wafer immersion tool that makes use of megasonic transducers in a single wafer immersion chamber.

### 16.4.1 Back End of the Line Processing

Equipment used for BEOL batch processing (*i.e.* post-etch residue removers) and their related processes are quite mature having been in use for many decades. The processing parameters for these products are typically in the 60–80°C range with processing times of 10–30 min. These operating temperatures and times are not acceptable for SWT processing because of their limitations for obtaining high wafer throughput. Whereas batch tools have throughputs approaching 500 wafers per hour, single wafer tools require much shorter process times to achieve the same throughput and to provide an acceptable cost of ownership (CoO) [32]. Processing times on the order of 30–120 sec per wafer are required, including the DIW rinsing and drying steps, with operating temperatures in the 25–55°C range. Because of their higher processing temperatures, the post-etch residue (PER) stripper products used for batch processing are not acceptable for SWT processing. Additionally, batch processing PER products generally have a high pH and contain organic solvents and amines that require an IPA or NMP intermediate rinse for corrosion protection. The added intermediate rinsing step adds to the overall processing time, thus making the CoO of single wafer tools unattractive. Therefore, entirely new chemical formulations have been developed to accommodate the demands of SWT processing, especially the requirement of low process temperatures, short processing times, no intermediate rinse, and the ability of the chemical to be removed with DIW rinses without substrate corrosion.

Single wafer products targeting BEOL PER applications are generally semi-aqueous, fluoride (SAF) chemistries comprised of a fluoride source, an organic solvent, water, and a pH buffer. Some of the more popular products included Air Products ACT®NE-Series and ACT®EZSTRIP®500 series, ATMI ST-250, Baker REZI™-series and CLκ™-series, CuSolve™ EKC520™, and SAC™ EKC 600™

series. These SAF products typically operate at 25–40°C with processing times of 30–90 sec and do not require an intermediate rinse.

In addition to blended formulated stripper products, SWT platforms take advantage of the low CoO of dilute acids, such as dilute HF (DHF) at ratios of 300:1 to 1000:1 and dilute sulfuric acid hydrogen peroxide (DSP) mixtures [33]. Unlike the SAF chemistries that are recirculated within the SWT system, dilute acid (DA) strippers are single-use products. Typical process parameters for these products are 25°C for 60 sec or less.

As a further example, Tsang *et al.* compared amine-based and fluoride-based cleaners using a Verteq Goldfinger Mach II™ tool which is equipped with a megasonic wand. In this study, the F-based cleaning chemistry outperformed the amine cleaner in post-etch wet cleaning of a Cu/low κ interconnection application; the amine cleaner led to lift-off of the copper structures, as shown in Figure 16.3 [34].

### 16.4.2 Front End of the Line Processing

More recently, SWT platforms have been used for FEOL applications, such as pre-diffusion cleans that use SC-1 and SC-2 chemistries and removing high dose implanted resist. The latter generally uses SPM chemistry at high processing temperatures of 150–220°C. A challenge for the SWT manufacturers and the chemical suppliers for HDIS applications are providing products and processes that can completely dissolve the highly carbonized photoresist crust formed during the ion implantation process within the time constraints of a SWT process. The chemical products also must be compatible with metal gate materials and minimally attack silicon to preserve the ultra-shallow junctions and their near-surface doping levels. Chemical suppliers are currently pursuing alternatives to high temperature DSP chemistries that will achieve the above mentioned goals within the times required for SWT processing.

Single wafer processing is providing the needed alternative to batch processing required by advanced technology. Continued advancements in single wafer

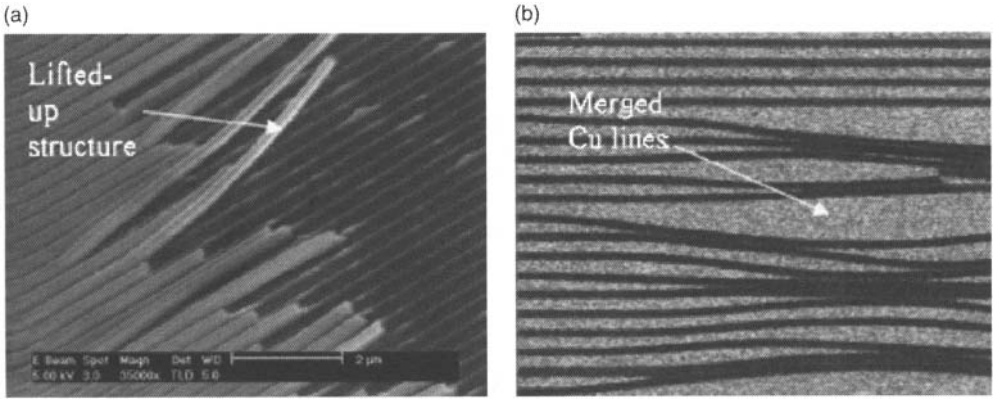


**Figure 16.3.** Comb structures of copper in a low-κ structure; a) after processing in SWT with amine-based cleaning and b) after CMP [34]. Reprinted from *Microelectronics Reliability*, Vol. 45, Tsang, C. F., Chang, C. K., Krishnamoorthy, A., Ee, K. J., Su, Y. J., Li, H. Y., Li, W. H., and Wong, L. Y., "A study of post-etch wet clean on electrical and reliability performance of Cu/low k interconnections", page 517. Copyright (2005) with permission from Elsevier.

tool design and chemical products designed specifically for these tools are making this a popular method of wafer processing. A variant of the high temperature SPM chemistry for SWT has been developed by SEZ [35]. In this "enhanced sulfuric acid" (ESA) stripping process, patterned arsenic-implanted deep ultraviolet (DUV) resist was successfully cleaned without a stripping process. Chapter 8 discusses the details of this process.

### 16.4.3 Photoresist Rework

The increasing complexity of wafer processing quite naturally leads to a high occurrence of misprocessing and defects. Photoresist imaging is one of very few steps of the manufacturing process where rework can be performed without being concerned with catastrophic fouling and particle redeposition. This challenge particularly is evident in bi-layer and tri-layer resist applications since a diversity of resist types are likely to be present [36]. Proper selection of cleaning formulations and process parameters can lead to efficient and effective reprocessing of expensive wafers [37]. Figure 16.4 shows one example, a reworked BEOL trench after photoresist coating, where the photoresist is removed. In this case, the photoresist is observed being dissolved over the time period studied and not being lifted off of the substrate. The photoresist removal uses ACT® EZSTRIP® 527 at 60°C in single-wafer tool. The cross section is of a Si-containing top imaging

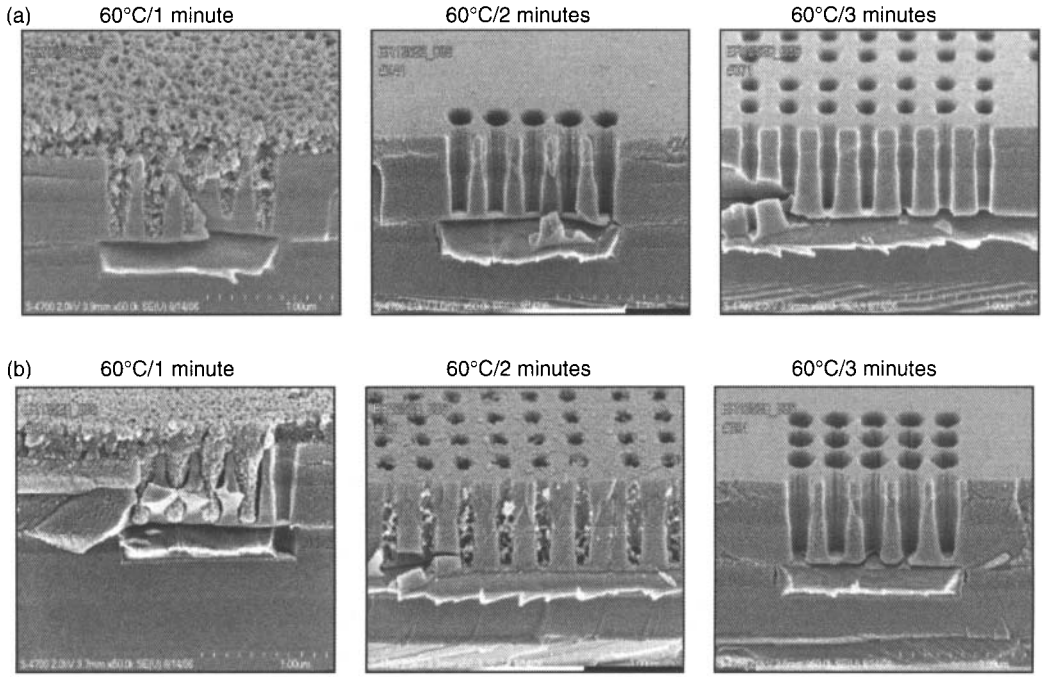


**Figure 16.4.** Scanning electron microscope image for the removal of photoresist at the BEOL trench level, used for reworking the lithography layer; a) center location and b) edge location [37]. Reproduced with permission of ECS – The Electrochemical Society from Wu, A., Baryschpolec, E., Molnar, L., Henry, S.-A., Detterbeck, S., Brilz, L., Bartsch, C., Sulzer, G., and Ott, A., *ECS Transactions*.

layer and organic planarization layer over interlayer dielectric and copper interconnect layer.

## 16.5 Wetting in Small Dimensions and Cleaning Challenges

As the IC industry continues its quest for smaller and smaller dimensions, there are specific applications where the aspect ratio of the features on patterned surfaces becomes an issue. In particular, pattern collapse can be a concern for a critical photoresist process rinse step immediately after photoresist development. The photoresist pattern is subjected to capillary forces due to the wetting of the small features, and this creates stress on the lines that can cause collapse, as depicted in Figure 16.5. Chapters 1 and 4 discuss surface tension and wetting associated with cleaning, rinsing, and drying. Two approaches to determine the force on small features – one based on force acting on the top of a line and one based on stress induced at the base of a patterned line – are outlined below.

In the first approach, the emphasis is on the capillary force acting on a structured surface and the force pushing features from the top. Using this approach, Cao *et al.* considered a variety of scenarios whereby capillary forces act on photoresist lines [39]. Referring to Figure 16.6, Equation 16.1 defines the force acting on equally spaced lines where one of the trenches is partially filled. Equation 16.2 defines a case where a line is present between two fully filled gaps of significantly different spacing. In both cases, it can be seen by inspection that the force ($F$) acting on a photoresist line is directly proportional to both surface tension of the liquid ($\gamma$) and $\cos\theta$ ($\theta$ = contact angle between liquid wetting fluid and solid resist surface). Where $S_A$ is the spacing between the lines, $H_B$ is the height of the feature, and $D$ is the length of the feature.

$$F_1 = \left( \frac{2\gamma\cos\theta}{S_A} \right) * H_A \tag{16.1}$$

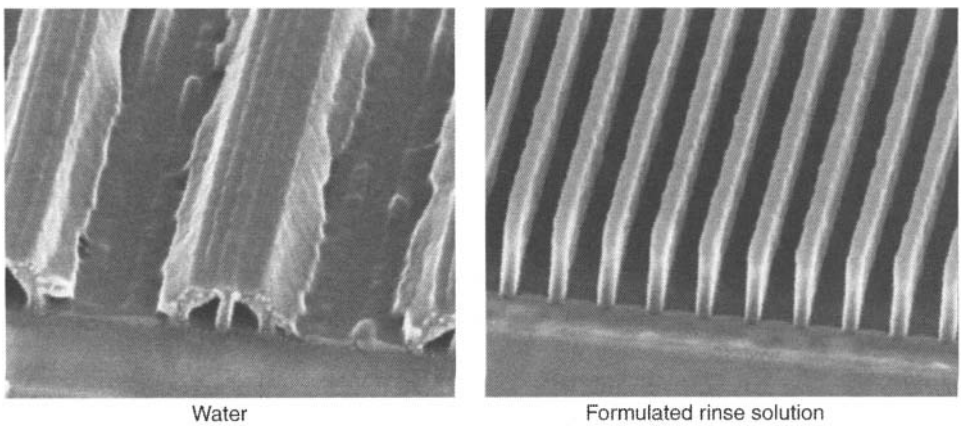


**Figure 16.5.** Pattern collapse of high aspect ratio features with water and its elimination with a formulated rinse solution [38].

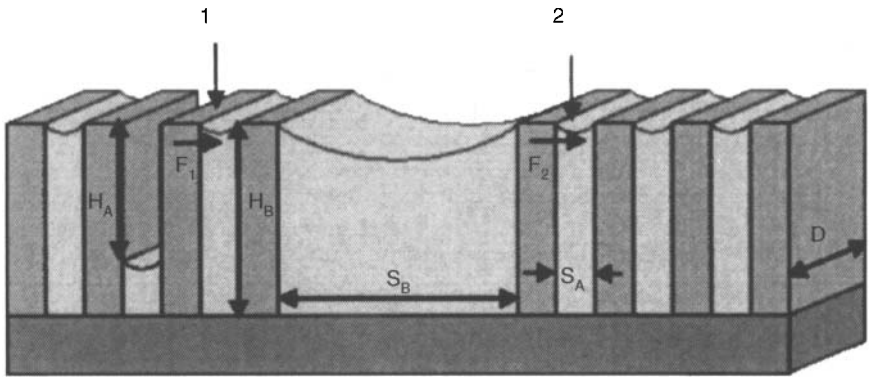


**Figure 16.6.** Physics of photoresist collapse, force model [39]. Reprinted with permission from *J. Vac. Sci. Technol., B*18(6):3303. Copyright 2000, American Vacuum Society

$$F_2 = 2\gamma\cos\theta\left(\frac{1}{S_A} - \frac{1}{S_B}\right) * H_B D \tag{16.2}$$

Thus, to minimize the capillary force acting on the line, the surface tension would have to be minimized, but without significantly decreasing the contact angle. Indeed, there would be a distinct advantage in increasing the contact angle if the sole focus is to minimize pattern collapse. Moreover, the term $\gamma\ cos\theta$ is merely the adhesion tension and easily relates to the Young's equation, as defined in Chapter 4. The adhesion tension is a useful and measurable quantity.

While Young's Equation is seemingly simple, surface energies at solid surfaces are difficult to study and adsorption phenomena lead to changes during the wetting process itself; however, the surface energy of the liquids ($\gamma_{sl}$) and contact angle are relatively easy to measure. Thus, it follows directly from the above discussion that the adhesion tension of the cleaning formulation/photoresist combination should be minimized in order to decrease the capillary forces acting on the photoresist line in order to avoid pattern collapse. Non-smooth surfaces will be addressed later in this section.

In a second approach, where the actual stress imposed at the base of the line itself is considered, the role of surface tension and contact angle is more complex. This was the approach taken by Petricich *et al.*, who calculated the stress at the foot of a photoresist line using Equation 16.3 [40]:

$$\sigma_{max} = 6 \cdot \gamma \cdot A \cdot \left(\frac{\sin\theta}{d} + A \cdot \frac{\cos\theta}{S}\right) \tag{16.3}$$

The terms are defined as shown in Figure 16.7, where A is the ratio, H/d and it is important to note that the symbols refer to slightly different quantities than in Figure 16.6 and Equations 16.1 and 16.2 (the conventions the original authors used).

Unlike Equations 16.1 and 16.2, it is not a simple matter to inspect Equation 16.3 to determine the trend in stress as it relates to $\theta$. In fact, if reasonable values are

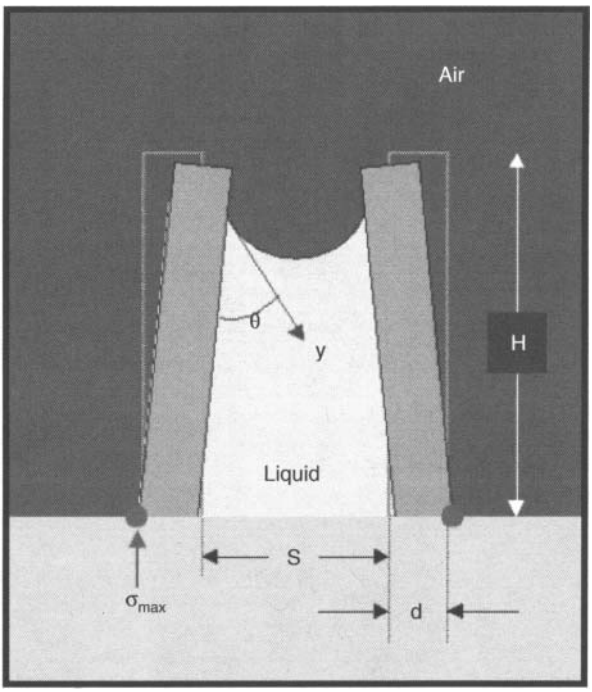


**Figure 16.7.** Physics of photoresist collapse, stress model [40]. Reproduced with permission from Petricich, G., Suzuki, K., Munemasa, J., Yoshikawa, T., Kawakami, N., Shimizu, S., and Watanabe, M., "Supercritical Resist Dry Technique for Electron-Beam Projection Lithography (EPL)" *Proc. SPIE, Emerging Lithographic Technologies VII*, 5037:917 (2003).

inserted for the variables in Equation 16.3 (where $A = 5$ and d = s), the maximum stress at the base of the line occurs at approximately $\theta = 10°$, and does not fall below the stress observed at complete wetting ($\theta = 0°$) until $\theta \sim 25°$. The challenge involved in minimizing pattern collapse therefore lies in providing a low surface tension liquid that does not completely wet the photoresist.

In other words, a cleaning agent should penetrate the resist lines without pulling them together. Because of the general relationship between $\theta$ and $\gamma$ inherent in Young's equation, this can only be achieved by designing the photoresist so it has a suitable surface energy or by formulating the cleaning agent with suitable additives to affect the surface energies of the photoresist surface. Adsorption phenomena involving surface-active agents to impart these types of properties are well-known [41]. The complex interplay between surface tension, contact angle, and adsorption phenomena leads to observations that surfactants can have varying effects on resist collapse [42].

As with pattern collapse, surface tension and solid surface energies play a key role in wetting and actual cleaning of fine features themselves. Facile movement of liquids in and out of fine patterns is obviously necessary. Unfortunately, many wetting studies on patterned surfaces are performed on features larger than relevant to current IC designs.

A recent exception is an elegant study on patterned surfaces with feature sizes of about 150 nm [43]. In this study, using water droplets, it was found that even hydrophilic surfaces constructed from hydrogenated silicon oxycarbide (SiCOH)

become hydrophobic after patterning. There were slight differences due to orientation relative to the pattern that relate to whether drop advancement is occurring parallel to the patterned lines or perpendicular, but the predominant effect observed is that the surface became hydrophobic. In this particular study, the authors were mainly interested in the impact of the wetting of such surfaces and the potential effect on the movement of stepper or scanner components in immersion lithography applications, but the study raises important questions with regard to wetting of fine patterns in cleaning as well. Indeed, in immersion lithography, bubble entrainment within the line (the Cassie-Baxter region, described in Chapter 4) was viewed as advantageous since this can aid in the liquid "slipping" over the surface; however, this situation should be avoided in cleaning. In particular, attempts to make more "green" formulations by increasing water content (and thereby the surface tension of the formulation) will have to be considered with regard to wetting of fine features. The use of surfactants may be required if higher water content is chosen as a formulating tool in order to address cost and EH&S issues.

The above study shows that inherently hydrophilic nanopatterned surface can be made hydrophobic simply as a consequence of the nanopatterning. This issue will continue to become more pronounced as feature sizes decrease. As stated above, this is typically not the case in larger scaled features, as the surface roughness of a hydrophilic surface tends to enhance the hydrophilicity. Indeed, such roughness can often lead to hemi-wicking or perhaps a better term, superwetting [44]. A study on similar nanopatterned scales, but using pillars and pits instead of lines showed complex behavior depending on spacing and specific shapes of features [45], but in this case, generally, hydrophobic surfaces remained hydrophobic when patterned. The impact of patterning on wetting and the issues involved in cleaning deep trenches and fine patterns remains complex and merits further study.

## 16.6 Environmental Health and Safety

### 16.6.1 Challenges to the Semiconductor Industry

As with the other unit operations involved in the complex process of semiconductor manufacturing, cleaning and stripping operations involve the use of hazardous substances. In some cases, specific segregation schemes to keep the chemical waste stream separate from simple rinse water might be warranted when the substances are both toxic and highly reactive, such as hydroxylamine. However, in most cases, chemical cleaning waste streams are treated in conjunction with other waste streams in the semiconductor fab that generally consist of "solvent" and "wastewater" streams [46], sometimes segmented further into acid and base wastewater streams. Furthermore, fluoride, metal residues [47], and even trace additives such as perfluorinated materials [48] must be considered in these waste streams. Semiconductor manufacturers always seek to minimize dealing with these hazardous materials, but as with other substances, trade-offs are made with regard to manufacturing requirements and dealing with the subsequent waste streams.

The greatest added burden from photolithography cleaners and strippers relates to the organic solvents used in the cleaners. Technologies have been developed to

treat the organic components of the aqueous waste streams, usually through oxidative techniques [49]. Recycling of the organic solvents used in photoresist stripping processes is of continuing interest [50], but is not yet a widespread practice. Chapter 6 addresses recycling and reuse of chemicals used in IC manufacturing.

### 16.6.2 Solvents

Needless to say, one of the primary environmental health and safety (EH&S) drivers to modify photoresist strippers and removers has been the use of solvents in these formulations and the requirement for safe disposal. From the earliest days of phenol-based strippers to today's relatively benign products based on organic amides and ether alcohols, there has been a desire to minimize their environmental impact. In addition to the exposure of these chemical to workers in the fab, strict regulatory limits based on flammability, inclusion on regulatory lists such as the US HAPS (United States hazardous air pollutants) inventory, or even concerns about ozone depletion weigh on decisions involving solvent selection.

Their progression can be very easily demonstrated by examination of the cases of NMP, DMAC (N,N-dimethylacetamide), and glycol ethers based on ethylene oxide or propylene oxide. A shift from NMP to DMAC occurred in the 1990's as studies emerged showing that NMP is a reproductive toxin. In 2001, California officially declared NMP to be in this category and subsequently set workplace exposure limits [51]. As industries shifted to DMAC as a replacement, it too became the subject of intense toxicology studies and was shown to have some of the same hazardous properties as NMP. A third solvent, DMSO, is being marketed as a replacement, and is touted as having low toxicity. Historically, DMSO has suffered from an issue with odor although it has been claimed that the odor is due to low levels of dimethylsulfide and not due to DMSO itself. An additional issue with DMSO is that it has readily accessible oxidized and reduced forms that can lead to complications when formulated with other materials. In addition, DMSO is perceived as being very effective for transporting materials through the skin, which is of great concern in industrial applications where solvents are used to dissolve other materials. In fact, DMSO is no more effective a transport agent than NMP [52], but its past history as a highly publicized medical adjuvant has perhaps tainted it more than other solvents.

An additional example of evolving solvent selection driven by EH&S issues is the switch from ethylene glycol (EG) ethers and esters to the propylene glycol (PG) versions. Ethylene glycol derivatives are associated with increased levels of reproductive problems in female workers [53]. For photoresist solvent applications, esters such as propylene glycol methyl ether acetate (PGMEA) and ethyl lactate have found wide spread use, but, under the harsher environment encountered by strippers and removers, the PG ether alcohols are more appropriate since they do not contain groups prone to thermal or hydrolytic cleaving.

A useful approach for formulating with alternative solvents to address EH&S issues is the use of Solubility Parameters. Large databases of these values have been tabulated for hundreds of solvents [54], and recently, $CO_2$ has been added [55]. Chapter 5 discusses the formulation design with an in-depth overview of Solubility Parameters. Solubility Parameters have been used for identifying candidates as "drop-in" replacements for older solvents, but they have an even more

powerful role in determining properties of solvent mixtures as values for mixtures are easily calculated. There are at least two computer programs available for comparing Solubility Parameters for individual solvents and for calculating values for mixtures [56, 57].

## 16.7 The Future of Advanced Photoresist Stripping and Cleaning

Over the past decade or so, there have been several efforts to drastically change the formulation medium for cleaning photoresist residues. Supercritical or liquid $CO_2$ is perhaps the best known of these proposed alternatives, and this area has been thoroughly reviewed [58, 59]. Other novel techniques including foam cleaning [60] and, more recently, the use of room temperature ionic liquids [61] have been proposed. These novel techniques would eliminate or mitigate many of the issues with current cleaning formulations including corrosivity, toxicity, volatility, and perhaps pattern collapse, and other issues related to wetting; however, none have been adopted by the semiconductor industry. Processes using dense-fluid $CO_2$ require significant capital investment and entail high energy costs due to extensive pressurization/depressurization cycling; foam cleaning requires a paradigm shift in how wafers are handled; ionic liquids are very expensive and require extensive recovery and recycling efforts – all of these issues are difficult to surmount as semiconductor manufacturers struggle with cost and increasingly complex processing in the other unit operations of the IC manufacturing process. The field of photoresist stripping and residue removal has always been evolutionary rather than revolutionary, and in the coming decade as manufacturers seek to minimize their risk in this unit operation, it may remain so.

Like all segments of the semiconductor supply chain, photoresist stripper and cleaner suppliers will face continuing cost-containment pressures. As mentioned earlier, maintaining a specialty mind-set in a commodities environment will be a continuing challenge in the industry. The specialized requirements of formulating products to address the multitude of new materials used for advanced chip manufacturing will severely test the "specialty" *vs.* "commodity" paradox, and stripper suppliers will increasingly face challenges that have already impacted the other segments of the wet chemical supply chain [62].

## Acknowledgements

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# INDEX


| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| **A** | | | | | | |
| Activation Energy | | | | | | |
| ammonia evaporation | 49 | 54 | | | | |
| decomposition of $H_2O_2$ in SC-1 | 51 | 61 | | | | |
| decomposition of $H_2O_2$ in SC-2 | 68 | | | | | |
| etching of Si | 120 | | | | | |
| etching of $Si_3N_4$ | 132 | 139 | | | | |
| etching of $SiO_2$ | 120 | | | | | |
| surface activation | 97 | | | | | |
| Adsorption | 3 | 9 | 17 | 19 | 26 | 31 |
| | 32 | 217 | 220 | 336 | 368 | 370 |
| | 376 | 378 | 382 | 384 | | |
| hydrogen | 453 | | | | | |
| metal | 17 | 19 | 434 | 437 | 448 | 496 |
| | 497 | 527 | | | | |
| moisture | 518 | 530 | 531 | 532 | 570 | 577 |
| surfactant | 9 | 22 | 26 | | | |
| Aluminum | | | | | | |
| etching | 331 | | | | | |
| metal | 328 | | | | | |
| passivation | 348 | | | | | |
| reactivity | 334 | | | | | |
| residues | 329 | | | | | |
| stripping of photoresist | 331 | | | | | |
| Amine-based Chemistry | 169 | 171 | 184 | | | |
| Ammonium Bifluoride | 341 | | | | | |
| Ammonium Hydroxide | 336 | | | | | |
| Ammonium Hydroxide Hydrogen Peroxide Mixture (APM) | 42 | 331 | 514 | | | |


This page has been reformatted by Knovel to provide easier navigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Angle Resolved X-ray Photoelectron Spectroscopy (ARXPS) | 558 | 560 | 561 | | | |
| Anneal, Annealing | 503 | 519 | | | | |
| Atomic Force Microscopy (AFM) | 505 | | | | | |
| Auger Analysis | 333 | 340 | | | | |
| Azole Corrosion Inhibitors | | | | | | |
| azole compounds | 404 | | | | | |
| benzotriazole (BTA) | 381 | 387 | 414 | 420 | 421 | |
| triazole (TAZ) | 401 | 405 | 416 | | | |
| **B** | | | | | | |
| Bath Life | 178 | 180 | 188 | 344 | 347 | |
| Bath Stability | 341 | | | | | |
| Bevel Edge Contamination Analysis | 555 | | | | | |
| Bond Strength | 47 | 98 | 112 | 120 | 126 | 131 |
| | 337 | 520 | 536 | | | |
| Bonding | | | | | | |
| bonding energy | 516 | 531 | | | | |
| conductive bonding | 530 | | | | | |
| direct bonding | 501 | 512 | 514 | 517 | 519 | 526 |
| | 528 | | | | | |
| wafer bonding | 501 | 505 | 507 | 509 | 511 | 512 |
| | 515 | 525 | 529 | 532 | 536 | |
| Boron Diffusion into Gate Oxide | 240 | 242 | 247 | 249 | | |
| Brush Scrubbing | 386 | 501 | 515 | 517 | | |
| Buffered Oxide Etch (BOE) and Buffered Hydrofluoric Acid (BHF) | 9 | 99 | 101 | 222 | 263 | 341 |
| Buffering Agents | 171 | 175 | | | | |
| **C** | | | | | | |
| Carboxylic Acid Corrosion Inhibitors | 397 | 399 | 411 | 413 | | |
| Caro's acid | 71 | | | | | |
| Cascade Rinser | 142 | | | | | |
| Charge Damage | 300 | | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Chelating Agents | 168 | 174 | 178 | 180 | 345 | |
| Chemical | | | | | | |
| blending | 193 | 202 | 206 | 230 | | |
| delivery systems | 193 | 210 | 214 | 234 | | |
| distribution | 193 | 202 | 210 | 215 | 228 | 234 |
| management | 193 | | | | | |
| recycling | 193 | 195 | 230 | 232 | | |
| reprocessing | 232 | | | | | |
| reuse | 193 | 230 | 232 | | | |
| waste | 230 | 232 | | | | |
| Chemical Contamination | | | | | | |
| inorganic | 210 | | | | | |
| metallic ion | 194 | 200 | 213 | 215 | 233 | |
| organic | 201 | 204 | 213 | 215 | 225 | 229 |
| | 232 | | | | | |
| particulate | 193 | 197 | 203 | 206 | 210 | 213 |
| | 215 | 218 | 228 | | | |
| Chemical Formulation | 167 | 178 | | | | |
| Chemical Mechanical Planarization (CMP) | 330 | 502 | 511 | 526 | 528 | 532 |
| Chemical Oxide | | | | | | |
| chemical oxide formation | 253 | 264 | | | | |
| ozonated water oxide formation | 256 | | | | | |
| SC-1 oxide formation | 253 | 255 | | | | |
| Chemical Purity | 175 | 186 | | | | |
| Cleaning | | | | | | |
| RCA cleaning | 469 | | | | | |
| standard clean 1 (SC-1) | 478 | 483 | 493 | | | |
| standard clean 2 (SC-2) | 478 | 483 | 488 | | | |
| Concentration Control | 86 | 129 | | | | |
| Conductivity | | | | | | |
| ionic | 336 | | | | | |
| metallic | 328 | | | | | |
| Conductivity Measurement | 53 | | | | | |
| Contact Angle | 22 | 148 | 157 | 161 | 378 | 576 |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Contamination Control | 193 | 206 | 327 | 547 | 550 | |
| Copper Cleaning Formulations | 392 | 394 | 397 | 400 | 410 | 415 |
| Copper Corrosion | | | | | | |
| acceleration | 397 | | | | | |
| causes | 391 | 394 | 406 | 411 | | |
| galvanic corrosion | 396 | 400 | | | | |
| photo-induced corrosion | 396 | | | | | |
| Copper Corrosion Inhibitor | 392 | 397 | 399 | 405 | 408 | 411 |
| Copper Passivating Agent | 393 | 400 | | | | |
| Corrosion | 373 | 376 | 387 | | | |
| Corrosion Inhibitor Efficiency | 398 | 400 | 410 | | | |
| Crevice Corrosion | 58 | 374 | | | | |
| Cross Linked Photoresist | 281 | 284 | 286 | 291 | 297 | 303 |
| | 316 | | | | | |
| Crust Breakthrough | 296 | 299 | 316 | | | |
| Cryoaerosol | 320 | | | | | |
| Crystal Growing | 471 | | | | | |
| Czochralski | 470 | 472 | 474 | | | |

## D

| | | | | | | |
|---|---|---|---|---|---|---|
| Degassing | 157 | 507 | 530 | | | |
| Dielectric Material | | | | | | |
| low- κ, carbon doped oxide (CDO) | 356 | 361 | 364 | 366 | 378 | 488 |
| low- κ, porous | 100 | 356 | 361 | 379 | 384 | 565 |
| | 570 | | | | | |
| high- κ | 240 | 297 | 309 | 430 | 442 | 452 |
| | 460 | 546 | 553 | 560 | 570 | 577 |
| Dilute Sulfuric Peroxide | | | | | | |
| Solution (DSP DSP+) | 341 | 344 | 350 | | | |
| Diluted Dynamic Clean | 40 | | | | | |
| Dimethylacetamide (DMAc) | 339 | 341 | | | | |
| Dimethylsulfoxide (DMSO) | 339 | 341 | 348 | | | |
| Diol/Triol Corrosion Inhibitors | 403 | 415 | 418 | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Dissolved Oxygen (DO) | 85 | 155 | 157 | 234 | 272 | 401 |
| | 432 | 498 | 517 | | | |
| Dry Etching | 96 | | | | | |
| Drying | 34 | 30 | 499 | 509 | 512 | 526 |
| | 528 | 531 | | | | |
| Dual Damascene | 402 | 421 | | | | |
| Dual Metal Gate | 242 | 246 | 263 | | | |
| **E** | | | | | | |
| Electrical Double Layer | 3 | 7 | 8 | 11 | 15 | |
| Electrochemical Residue Sensors (ECRS) | 561 | | | | | |
| Electrohydrodynamic Spray | 350 | | | | | |
| Electromigration | 327 | 331 | 336 | 343 | | |
| Enhanced Sulfuric Acid (ESA) | 307 | | | | | |
| EPA Regulations | 187 | | | | | |
| Equivalent Oxide Thickness | 240 | 247 | 251 | 253 | 258 | |
| Etch Mechanism | | | | | | |
| Si in $HF/HNO_3$ | 113 | | | | | |
| Si in KOH | 116 | | | | | |
| Si in TMAH | 120 | | | | | |
| $Si_3N_4$ in $H_2O$ | 127 | | | | | |
| $Si_3N_4$ in $H_3PO_4$ | 127 | | | | | |
| $Si_3N_4$ in HF | 124 | | | | | |
| $SiO_2$ in $H_2O$ | 109 | | | | | |
| $SiO_2$ in HF | 102 | | | | | |
| Etch Selectivity | 98 | | | | | |
| Si/Al | 121 | | | | | |
| $Si/Si_3N_4$ | 112 | 116 | | | | |
| $Si/SiO_2$ | 83 | 112 | 116 | 119 | | |
| $SiO_2/Si_3N_4$ | 110 | 125 | 131 | | | |
| Etching | | | | | | |
| Si | 43 | 98 | 111 | | | |
| $Si_3N_4$ | 98 | 122 | | | | |
| $SiO_2$ | 44 | 80 | 98 | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| **F** | | | | | | |
| Filters | 197 | 203 | 205 | 217 | 222 | 225 |
| | 229 | | | | | |
| Filtration | | | | | | |
| capsules | 221 | 225 | 230 | | | |
| design | 220 | | | | | |
| log reduction value (LRV) | 227 | | | | | |
| materials | 217 | 220 | 222 | 224 | 227 | 229 |
| mechanisms | 193 | 217 | 227 | | | |
| membrane | 223 | 228 | 230 | 234 | | |
| performance | 194 | 196 | 198 | 204 | 208 | 220 |
| | 224 | 229 | | | | |
| rating | 226 | 227 | | | | |
| Fluoride-based Chemistry | 169 | 172 | | | | |
| Forming Gas Plasma | 290 | 300 | | | | |
| Formulation Modeling | 178 | 180 | | | | |
| Formulation Specifications | 178 | | | | | |
| Fourier Transfer Infrared (FTIR) | | | | | | |
| Spectroscopy | 514 | 528 | 530 | | | |
| Fully Silicided (FUSI) Process | 242 | 251 | | | | |
| **G** | | | | | | |
| Galvanic Corrosion | 262 | 272 | 277 | | | |
| Gate-first Process | 243 | | | | | |
| Gate-last Process | 244 | 248 | 261 | 277 | | |
| Generation of Strippers | 168 | | | | | |
| first generation | 169 | | | | | |
| second generation | 170 | | | | | |
| third generation | 171 | | | | | |
| Germanium | 569 | | | | | |
| carbon contamination | 444 | 450 | 456 | 459 | 460 | 463 |
| | 466 | | | | | |
| crystal structure | 430 | | | | | |
| metal contamination | 434 | 437 | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Germanium (*Cont.*) | | | | | | |
| particulate contamination | 440 | 442 | | | | |
| use in integrated circuits | 429 | | | | | |
| Germanium Etching Rates | | | | | | |
| in cleaning chemicals | 433 | 441 | | | | |
| in water | 432 | | | | | |
| Germanium on Insulator, GeOI | 502 | 507 | 516 | | | |
| Germanium Oxide | 431 | 443 | 447 | 458 | 463 | |
| Germanium Passivation | | | | | | |
| chlorine passivation | 462 | | | | | |
| hydrogen passivation | | | | | | |
| (also Hydrogenation) | 453 | 460 | | | | |
| nitride passivation | 448 | 452 | 461 | | | |
| oxide passivation | 442 | | | | | |
| oxynitride passivation | 448 | 451 | | | | |
| sulfur Passivation | 464 | | | | | |
| **H** | | | | | | |
| Hydrofluoric Acid, HF (liquid, vapor) | 59 | 80 | 85 | 89 | 100 | 508 |
| | 510 | 513 | 530 | 531 | 537 | |
| High Aspect Ratio (HAR) Features | 3 | 26 | 146 | 148 | 156 | 160 |
| | 566 | 576 | | | | |
| High Dose Implant | 282 | 284 | 292 | 294 | | |
| High Dose Implant Stripping (HDIS) | 281 | 289 | 291 | 294 | 298 | |
| | 300 | 303 | 305 | 313 | 571 | 574 |
| High Dose Implant Stripping (HDIS) Tools | 297 | 301 | | | | |
| High Energy X-ray Reflectivity (HEXRR) | 514 | 528 | 561 | | | |
| High- κ Metal Gate | 297 | 312 | 316 | | | |
| High- κ Anneal | | | | | | |
| ammonia anneal | 258 | 261 | | | | |
| anneal | 247 | 251 | 254 | 260 | 265 | 270 |
| cleanliness prior to anneal | 278 | | | | | |
| nitrogen anneal | 270 | | | | | |
| Oxygen Anneal | 260 | | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| High- κ Dielectric Material | 239 | 243 | 253 | | | |
| High- κ Dielectric on Germanium | 253 | 260 | 430 | 442 | 447 | 452 |
| | 460 | 463 | 466 | | | |
| High- κ Removal | | | | | | |
| dry removal | 266 | | | | | |
| requirements | 264 | | | | | |
| wet and dry removal | 272 | | | | | |
| wet removal | 269 | | | | | |
| High- κ /Metal Gate Devices | 239 | | | | | |
| High- κ /Metal Gate Resist Stripping | | | | | | |
| plasma stripping | 273 | | | | | |
| wet stripping | 273 | 276 | | | | |
| Huang-l | 42 | | | | | |
| Huang-2 | 67 | | | | | |
| Hydrochloric Acid Hydrogen Peroxide | | | | | | |
| Mixture (HPM) | 67 | 509 | 511 | | | |
| Hydrogen ($H_2$) Plasma | 301 | 304 | 306 | | | |
| Hydrogen Passivation | 80 | | | | | |
| hydrogen peroxide | 331 | 335 | 341 | | | |
| hydrogen plasma treatment | 328 | 338 | | | | |
| Hydrogenation | 453 | 460 | | | | |
| Hydrogen-terminated Surfaces | 141 | 152 | 253 | 259 | | |
| Hydrophilic Surface | 141 | 144 | 146 | 149 | 152 | 159 |
| | 162 | 497 | 503 | 507 | 513 | 516 |
| | 518 | 520 | 524 | 528 | 530 | 532 |
| | 578 | | | | | |
| Hydrophobic Surface | 141 | 145 | 149 | 151 | 156 | 159 |
| | 497 | 502 | 507 | 510 | 513 | 524 |
| | 531 | 579 | | | | |
| Hydroxylamine-based Chemistry | 171 | 178 | 180 | 184 | 327 | 332 |
| | 337 | 340 | 343 | 351 | 567 | 579 |
| Hydroxyl-terminated Surface | 241 | 253 | 258 | 261 | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| **I** | | | | | | |
| IMEC-clean | 42 | | | | | |
| In Situ Steam Generation Oxidation | 259 | | | | | |
| Inductively Coupled Plasma Mass Spectrometry (ICP-MS) | 550 | 554 | 556 | | | |
| In-situ Characterization | 561 | | | | | |
| Interaction Forces | 13 | 15 | 18 | | | |
| Interfacial Oxide | 240 | 253 | 258 | | | |
| Isoelectric point (IEP) | 6 | 8 | 10 | 21 | 102 | |
| Isopropyl Alcohol (IPA) | 30 | 378 | | | | |
| **J** | | | | | | |
| Junction Loss | 298 | | | | | |
| **K** | | | | | | |
| Kelvin Probe | 557 | | | | | |
| Kinetic Salt Effects | 183 | | | | | |
| **L** | | | | | | |
| Lapping | 469 | 471 | 473 | 481 | 484 | 488 |
| | 490 | | | | | |
| Layer Transfer | 498 | | | | | |
| Leakage Current | 239 | 256 | 258 | 261 | | |
| Localized Contamination | 549 | 550 | | | | |
| Low Gamma Solvent, LGS | 513 | | | | | |
| Low K cracks | 379 | | | | | |
| **M** | | | | | | |
| Marangoni Dryer and Drying | 31 | 34 | 71 | 156 | 158 | 349 |
| | 378 | | | | | |
| Material Stacking | 501 | | | | | |
| Megasonic | 350 | 385 | 386 | | | |
| Mercapitan Corrosion Inhibitors | 403 | 420 | | | | |
| Mercury | 336 | | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Metal Gate Electrode | | | | | | |
| metal gate material | 241 | | | | | |
| work function | 242 | | | | | |
| Metal Halides, Properties | 334 | | | | | |
| Metal Induced Pitting (MIP) | 491 | | | | | |
| Metal Ion Contamination | 52 | 61 | 377 | | | |
| Metal Reclaim | 488 | | | | | |
| Monoethanolamine (MEA) | 339 | 342 | | | | |
| Mouse Bites | 335 | | | | | |
| **N** | | | | | | |
| Near Edge X-ray Absorption Fine Structure (NEXAFS) | 561 | | | | | |
| Near Infrared | 83 | 87 | 90 | | | |
| Nitrided Gate | 240 | 250 | 254 | 259 | 261 | |
| N-methyl Pyrrolidone (NMP) | 169 | 173 | 175 | 188 | 339 | 341 |
| | 348 | | | | | |
| Non-Metal Reclaim | 484 | | | | | |
| Nucleophile | 341 | 343 | | | | |
| **O** | | | | | | |
| Overflow Rinser | 142 | | | | | |
| Oxidation-Reduction Potential (ORP) | 491 | | | | | |
| Oximes | 346 | | | | | |
| Oxygen ($O_2$) Plasma | 305 | 328 | 331 | 338 | 340 | 346 |
| Oxygen Scavengers | 175 | 178 | 403 | 414 | | |
| Oxynitride Gate | 240 | 255 | 258 | | | |
| Ozone | 79 | 497 | 499 | 508 | 522 | |
| **P** | | | | | | |
| Packaging | 500 | 522 | | | | |
| Particle Adhesion | 376 | | | | | |
| Particle Counting | 194 | 206 | 212 | 225 | | |
| Particle lift Off | 381 | 387 | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Particle Removal | 377 | 381 | 387 | 514 | | |
| Particle Removal Efficiency | 43 | 49 | 59 | 66 | 67 | 164 |
| | 203 | 211 | 227 | 377 | 384 | 424 |
| | 441 | 512 | 515 | | | |
| Particles in $H_3PO_4$ | 134 | | | | | |
| Passivating Agents | 172 | 175 | 178 | 180 | | |
| Pattern Collapse | 576 | 581 | | | | |
| Performance Specifications | | | | | | |
| final thickness | 478 | | | | | |
| particle | 469 | 473 | 477 | 486 | 491 | |
| surface defects | 474 | 478 | 481 | | | |
| surface roughness | 478 | 491 | | | | |
| total thickness variation (TTV) | 478 | | | | | |
| trace metal contamination | 478 | | | | | |
| Phase-change Memory | 566 | 569 | | | | |
| Phenol-based Strippers | 169 | 170 | | | | |
| Photoresist Crust | 288 | 295 | 300 | 306 | 311 | 313 |
| | 316 | 320 | | | | |
| Photoresist Modification | 288 | 303 | 320 | | | |
| Photoresist Popping | 299 | 301 | 305 | 307 | | |
| Photoresist Rework | 575 | | | | | |
| Photoresist Strippers | | | | | | |
| fluoride-based | 568 | | | | | |
| future of | 581 | | | | | |
| historical background | 566 | | | | | |
| Photoresist Stripping | 73 | 167 | 179 | 181 | 184 | |
| Physical Vapor Deposition (PVD) | | | | | | |
| aluminum | 331 | | | | | |
| tungsten | 330 | | | | | |
| Piranha | 71 | | | | | |
| Planarization | 501 | 505 | 538 | | | |
| Plasma activation | 501 | 503 | 519 | 524 | 530 | |
| Point of Zero Charge (PZC) | 5 | 6 | 8 | | | |
| Point-of-use | 193 | 205 | 211 | 216 | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Polishing | 469 | 473 | 478 | 481 | 484 | 488 |
| | 490 | 493 | | | | |
| Polystyrene Latex Spheres (PSL) | 209 | 226 | 229 | | | |
| Pore Size | 219 | | | | | |
| Post-CMP (chemical mechanical polishing) | | | | | | |
| Cleaning | 167 | 168 | 172 | 175 | 373 | 380 |
| | 387 | 398 | 401 | 409 | 419 | |
| Post-etch Clean | 374 | 396 | 398 | 402 | 404 | 411 |
| | 420 | | | | | |
| Post-etch Residue (PER)- | | | | | | |
| composition | 377 | 396 | 591 | | | |
| Post-etch Residue Removal (PERR) | 169 | 174 | 180 | 183 | 376 | 336 |
| | 351 | 359 | 569 | 573 | | |
| Potassium Hydroxide | 336 | | | | | |
| Pourbaix Diagram | 215 | 355 | 396 | 402 | 431 | 496 |
| Process Tools | | | | | | |
| immersion | 193 | 202 | 228 | 230 | 234 | |
| single wafer | 193 | 202 | 204 | 228 | 230 | |
| Pumps | 194 | 196 | 198 | 201 | 203 | 206 |
| | 212 | | | | | |

## Q

| | | | | | | |
|---|---|---|---|---|---|---|
| Quick Dump Rinsers (QDR) | 142 | 145 | | | | |

## R

| | | | | | | |
|---|---|---|---|---|---|---|
| RCA Clean | 41 | 42 | 511 | 515 | 518 | 519 |
| | 520 | 524 | 528 | | | |
| REACH Regulations | 190 | | | | | |
| Recirculation | 193 | 197 | 202 | 222 | 227 | 235 |
| Reclaiming | 469 | 476 | 480 | 482 | 488 | |
| Recycling | 477 | 480 | 483 | 488 | 494 | |
| Replacement Gate | 242 | 244 | 251 | 264 | | |
| Replacement Gate Removal | 264 | | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| **S** | | | | | | |
| Selective Passivation | 313 | | | | | |
| Selective Solvency | 182 | | | | | |
| Self-assembled Monolayers (SAM) | 313 | | | | | |
| Semi-aqueous Chemistry (SAC) | 169 | 172 | 176 | 184 | 187 | 312 |
| Shelf Life | 186 | | | | | |
| Silanol | 510 | 520 | | | | |
| Silica | | | | | | |
| dissolved silica | 77 | 109 | 135 | 145 | 152 | 154 |
| | 157 | | | | | |
| precipitated silica | 154 | 161 | 378 | | | |
| silica particles | 10 | 12 | 21 | 144 | 162 | 219 |
| | 226 | 377 | 383 | 386 | 425 | 440 |
| | 510 | | | | | |
| solubility in water | 153 | 156 | | | | |
| silicic acid | 153 | 157 | 378 | | | |
| Silicon | | | | | | |
| metallurgical-grade silicon | 470 | | | | | |
| mono-crystalline silicon | 471 | | | | | |
| polycrystalline | 470 | | | | | |
| Silicon Damage | 295 | | | | | |
| Silicon Germanium Passivation | 467 | | | | | |
| Silicon Loss | 295 | 299 | 307 | 312 | 316 | |
| Silicon on insulator (SOI) | 500 | 507 | 516 | | | |
| Siloxane | 499 | 508 | 520 | | | |
| Single Chemistry Clean | 43 | | | | | |
| Single Wafer Tool (SWT) | | | | | | |
| back end of line (BEOL) | 573 | | | | | |
| front end of line (FEOL) | 572 | 574 | | | | |
| Slurry | 100 | 165 | 231 | 373 | 376 | 379 |
| | 383 | 387 | 397 | 406 | 421 | 424 |
| | 477 | 510 | 515 | | | |
| Smart-Cut | 500 | 508 | | | | |
| Smoothing | 497 | 500 | 503 | 521 | 526 | 528 |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Sodium Carbonate | 336 | | | | | |
| Solubility Parameters | 180 | 182 | 580 | | | |
| Solvent Recycling | 189 | | | | | |
| Solvent-based Strippers | 170 | 177 | 182 | 188 | 190 | |
| Solvents | 566 | 570 | 573 | 579 | 580 | |
| Spin Rinse Dryer (SRD) | 142 | 144 | 157 | 162 | 349 | |
| Standard Clean-1 (SC-l) | 41 | 230 | 253 | 262 | 512 | 527 |
| | 574 | | | | | |
| chelating agent addition | 497 | | | | | |
| concentration | 49 | 206 | 434 | | | |
| concentration monitoring | 53 | | | | | |
| diluted | 66 | | | | | |
| electrochemistry | 42 | | | | | |
| etch rate | 45 | 48 | 63 | | | |
| galvanic etching | 55 | | | | | |
| gas bubbles | 55 | | | | | |
| molecular mechanism | 46 | | | | | |
| particle removal | 514 | | | | | |
| passivation | 47 | 506 | | | | |
| Standard Clean-2, SC-2 | 42 | 67 | 204 | 230 | 253 | 276 |
| | 502 | 509 | 511 | 515 | 527 | |
| concentration | 67 | 206 | 434 | | | |
| HCl fumes | 70 | | | | | |
| ionic strenght | 71 | | | | | |
| metal-ion adsorption | 67 | | | | | |
| particle deposition | 68 | | | | | |
| Stiction | 160 | | | | | |
| Stripping Mechanism | 173 | 175 | 177 | | | |
| Substrate Loss | 265 | | | | | |
| Sulfate Residue | 308 | | | | | |
| Sulfur Trioxide ($SO_3$) | 78 | | | | | |
| Sulfuric Acid Hydrogen Peroxide Mixture (SPM) | 41 | 67 | 71 | 77 | 285 | 293 |
| | 297 | 300 | 308 | 508 | 527 | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Sulfuric Acid Ozone Mixture (SOM) | 79 | | | | | |
| Supercritical $CO_2$ ($SCCO_2$) | 313 | 317 | 328 | 348 | 351 | |
| Surface Charge | | | | | | |
| caused by drying | 146 | | | | | |
| caused by spinning | 146 | 149 | | | | |
| charge particles | 146 | 165 | | | | |
| pH Dependence | 5 | | | | | |
| $SiO_2$ | 4 | | | | | |
| $Si_3N_4$ | 4 | 6 | | | | |
| Surface Energy | 148 | 150 | 159 | 164 | 577 | 578 |
| Surface Roughening | 55 | 61 | 497 | 499 | 503 | 505 |
| | 512 | 520 | 525 | 528 | 531 | |
| Surface Smoothing | 509 | | | | | |
| Surface Tension | 4 | 22 | 27 | 148 | 158 | 163 |
| | 576 | | | | | |
| Surface Tension Gradient (STG) | 4 | 30 | | | | |
| Surface Tension Gradient (STG) Dryers | 144 | 158 | 161 | 166 | 349 | |
| Surface Wetting | | | | | | |
| capillary action | 150 | 163 | | | | |
| Cassie-Baxter wetting | 152 | 579 | | | | |
| general surface wetting | 144 | 148 | 565 | | | |
| Wenzel wetting | 152 | | | | | |
| wetting features | 150 | 577 | | | | |
| wetting rough surfaces | 151 | 163 | | | | |
| surfactant | 9 | 16 | 22 | 26 | 173 | 178 |
| | 182 | 380 | 384 | 486 | 492 | |

## T

| | | | | | | |
|---|---|---|---|---|---|---|
| Tetraethylorthosilicate (TEOS) Glass | 336 | | | | | |
| Three-dimensional (3D) Integration | 502 | 504 | | | | |
| Thermal Treatment | 503 | 507 | 519 | 524 | 529 | 532 |
| Time of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) | 76 | 556 | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Total Reflection X-ray Fluorescence (TXRF) | | | | | | |
| alternative sources | 547 | | | | | |
| analysis of non-silicon surfaces | 322 | 547 | 553 | | | |
| backside surface analysis | 552 | | | | | |
| edge exclusion | 551 | | | | | |
| high- κ films | 547 | | | | | |
| light elements | 322 | 484 | 548 | | | |
| reference free calibration | 561 | | | | | |
| wafer mapping | 549 | | | | | |
| Tungsten | | | | | | |
| metal | 328 | | | | | |
| plug corrosion | 162 | 176 | 336 | 343 | | |
| plug etchback | 330 | 342 | | | | |
| resistivity | 328 | | | | | |
| selectivity to | 111 | | | | | |
| Twelve Principles of Green Chemistry | 189 | | | | | |
| **U** | | | | | | |
| Ultraviolet-Ozone cleaning, (UV-$0_3$) | 73 | 79 | 90 | 234 | 256 | 258 |
| | 260 | 350 | 367 | 431 | 445 | 501 |
| | 503 | 519 | 526 | 529 | | |
| **V** | | | | | | |
| Van der Waals Force | 11 | 15 | 68 | 163 | 213 | 376 |
| | 384 | 387 | 440 | 503 | 507 | 512 |
| | 535 | | | | | |
| Vapor Phase Decomposition Analysis (VPD) | 484 | 548 | 553 | | | |
| Vapor Phase Treatment Analysis (VPT) | 554 | | | | | |
| **W** | | | | | | |
| Wafer Edge Contamination | 147 | 160 | 226 | 295 | 386 | 462 |
| | 477 | 488 | 494 | 555 | | |
| Wafer Manufacturing | 474 | 487 | | | | |


This page has been reformatted by Knovel to provide easier avigation.

| Index Terms | Links | | | | | |
|---|---|---|---|---|---|---|
| Wafer Reclamation | 474 | 485 | 492 | 494 | | |
| Water Droplet | 159 | 162 | 166 | 378 | | |
| Watermark(s) | 157 | 378 | | | | |
| Wet Etching | | | | | | |
| Anisotropy | 97 | | | | | |
| Definition | 96 | | | | | |
| Wettability | 22 | 26 | 1 | 143 | 148 | 150 |
| | 170 | 177 | 179 | 341 | 351 | 378 |
| | 490 | 528 | 576 | | | |
| **Y** | | | | | | |
| Young's Equation | 150 | 577 | 578 | | | |
| **Z** | | | | | | |
| Zeta Potential | 6 | 8 | 21 | 382 | | |


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